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EXTENDED ABSTRACTS

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An Ultralow Noise Amplifier for Superconductive Detectors#

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Abstract. The design and construction of an ac-coupled, ultralow noise amplifier (equivalent input noise voltage E_n= 0.33 nV/$\sqrt{Hz}$, optimum source impedance 1kΩ at 100kHz) is presented. The amplifier employs nine Sony 2SK152-4 JFETs in parallel to yield the low noise result. Measurements were taken to characterize the amplifier's bandwidth, the additive voltage noise vs. frequency, and the current noise vs. frequency. SPICE modeling parameters for the JFETs used will also be discussed. Finally, we will review the performance of the amplifier in a flux-locked SQUID application.

1. Introduction

Superconductive detectors, such as SQUIDs and Josephson junction particle detectors, often have very low intrinsic noise (10-100 pV/$\sqrt{Hz}$ for a dc SQUID). The noise of the following amplifier must be significantly smaller than the output noise of the superconductive detector to realize the full system performance. As the performance of superconducting detectors improves so must that of the room temperature amplifier.

In this paper we describe the theory, implementation and characterization of a very low noise amplifier which we have used to directly measure the output signal of a dc SQUID. The basic form of the amplifier is similar to that published by Hallgren[1]. Other similar amplifiers have been presented by VanVechten, *et al.*[2] and Pallottino, *et al.*[3]. Modifications were made to these designs to optimize an amplifier for our purposes.

2. Amplifier Theory

The total noise density observed at the input to an amplifier (E_{nt}) can be modeled in the following form:

$$E_{nt}^2 = E_d^2 + E_n^2 + I_n^2 Z_{eff}^2 \ (V^2/Hz) \qquad (1)$$

where E_d is the output noise density of the detector in units of V/$\sqrt{Hz}$, E_n and I_n are the voltage and current noise densities of the amplifier with units of V/$\sqrt{Hz}$ and A/$\sqrt{Hz}$ respectively, and Z_{eff} is the net impedance at the amplifier input (consisting of the source impedance Z_s in parallel with the amplifier's input impedance). For many applications Z_s dominates the Z_{eff} term, in the following discussion we approximate Z_{eff}=Z_s. In this paper we assume that E_n and I_n are uncorrelated and that E_d is fixed.

For a fixed source impedance, Motchenbacher and Fitchen have shown that when K identical amplifiers are placed in parallel, E_n is reduced by a factor of $\sqrt{K}$ while I_n is increased by the same factor[4]. For a given source impedance Z_s one finds that the amplifier's contribution to the total noise E_{nt} of equation (1) is minimized when

$$K=E_n/(I_n Z_s) \qquad (2)$$

Alternatively, for a fixed amplifier configuration and source impedance, one may use a transformer to modify the effective impedance of the source. Within certain limits, a transformer increases the effective impedance of a source by the square of the turns ratio $(N2/N1)^2$ where N2 and N1 are the number of turns on the secondary and primary of the transformer respectively. In general, the optimum turns ratio occurs when:

$$(N2/N1)^2=E_n/(I_n Z_s) \qquad (3)$$

Caveats- Both impedance matching techniques described above have their shortcomings. In practice, physical size, input capacitance and power consumption limit the number of amplifiers one can place in parallel. Large step-up transformers have limited bandwidth and self resonances caused by parasitic capacitances.

By making an attempt to optimize the noise impedance of an amplifier ($E_n/(KI_n)=Z_s$ equation 2), the construction of an impedance matching transformer is greatly simplified, and sometimes unnecessary. For the remainder of this paper we will concentrate on amplifier optimization for low impedance sources.

3. Implementation

Our amplifier, shown in Figure 1, was constructed on a single ground-plane 4" X 5" prototype board. The design is essentially that of a two-stage cascode amplifier with an op-amp follower. The input stage consists of nine Sony 2SK152-4 JFETs in parallel (Q1-Q9). The noise of a single 2SK152-4 was measured to be: E_n=1.3 nV/$\sqrt{Hz}$ and I_n=65fA/$\sqrt{Hz}$ at 10kHz with a drain current of 10mA (E_n of the 2SK152-4 is approximately a factor of two larger with a 1mA drain current)[5]. The 10mA bias condition results in an optimum source impedance Z_{opt} (where $Z_{opt}=E_n/I_n$) of 20kΩ for a single device. Since the typical dynamic impedance of a SQUID is on the order of 5Ω, equation (2) suggests one would need 4000 stages to optimize this amplifier. Nine FETs seemed a practical limit, based on the bias current needed for each FET. The total current of the input stage (90mA) must flow through Q10 (Harris 2N5434) which is close to its upper limit of 100mA. To prevent nonlinearities in Q10 and thermal noise in R1 from degrading the amplifier's noise performance, both parts should be well heat sunk; R1 should also be rated for high power (5-10 Watts). All other resistors are 1% metal film and all non-polarized capacitors use mylar dielectric. Q10 and Q11 are 2N5434; all other FETs are 2SK152-4.

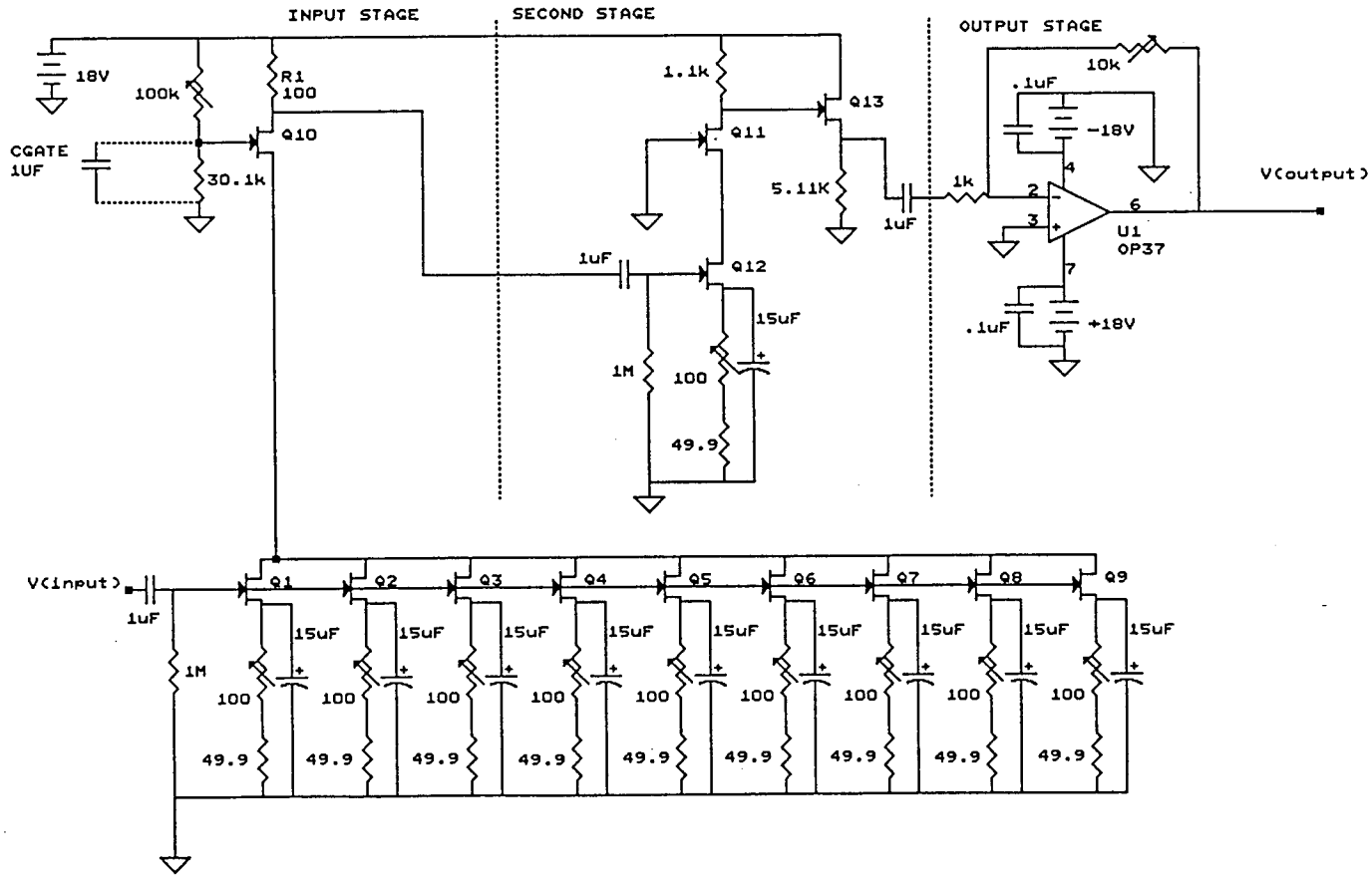

Figure 1: Schematic of Low Noise Amplifier

The first stage alone only afforded a voltage gain of 15 V/V so a second similar single FET stage was needed to prevent the noise of the OP-37 op-amp (3nV/$\sqrt{Hz}$ at 1kHz) from degrading the amplifier's noise performance. The total gain of the first two stages is 220V/V. The amplifier has poor power supply noise rejection. Therefore, to achieve the specified low noise result, large (6A-hour) lead acid batteries were used to provide quiet supply voltages. The need for large battery capacity is a result of the approximately 2W power dissipation in this circuit.

The gate capacitor labeled CGATE is needed for this configuration to give the best high-end frequency response. However, it was noted that with low source impedances (<50Ω) the amplifier would drift into harsh oscillations. All measurements discussed in the next section took place without this capacitor for maximum stability. It should be noted that for higher source impedances (100-1kΩ) the amplifier was quite stable (no oscillations were observed) with the capacitor inserted. In this situation the bandwidth can be increased by a factor 3-4 (reduction of the Miller effect).

The voltage on the gate of Q10 should be adjusted to approximately 5V. The individual drain currents should then be adjusted on Q1-Q9 and Q12 to 10mA (about 90Ω total drain resistance). The drain current can be easily monitored across the 49.9Ω fixed resistor in series with each drain. If the amplifier oscillates, small adjustments to the gate voltage of Q10 generally bring the amplifier into a stable and robust operating condition. Finally, the 10kΩ op-amp feedback resistor should be adjusted for the desired gain. If an OP-37 op-amp is used, the feedback resistor should be >5kΩ or the op-amp may become unstable[6]. Any high performance op-amp may be used, however, its noise should be less than $22nV/\sqrt{Hz}$.

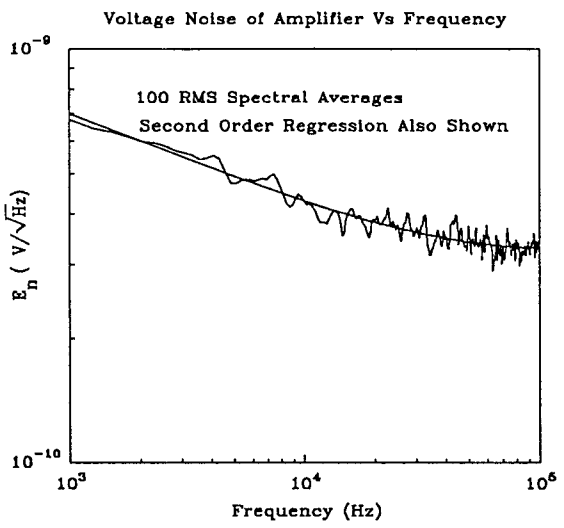

Figure 2a: E_n of Low Noise Amplifier

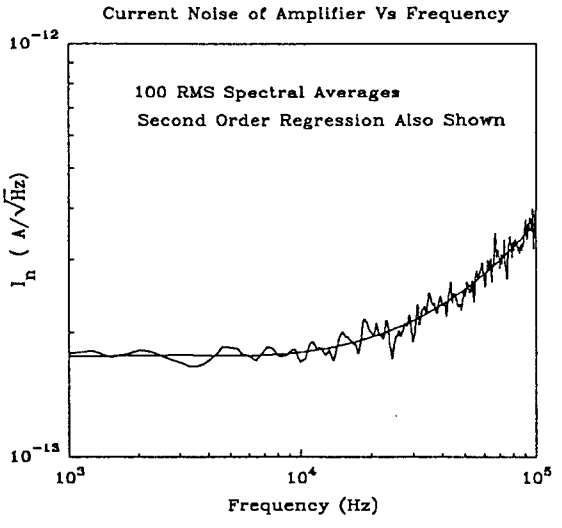

Figure 2b: I_n of Low Noise Amplifier

4. Measurements

Figures 2a and 2b show E_n and I_n for the amplifier described above. E_n was measured with the input to the amplifier shorted using a HP-35660 spectrum analyzer (Hanning window). 100 RMS averages were taken to reduce the variance. To prevent quantization error, a low noise commercial amplifier ($4nV/\sqrt{Hz}$) was used to make the total gain a calibrated 10^6 V/V. Finally, a second order regression was performed on the data.

I_n was measured by placing a mica capacitor across the input such that the I_n term of equation (1) dominated the expression. Several different capacitors were used (12pF,100pF,620pF). Since I_n is independent of source impedance, the input capacitance of the amplifier and I_n can be obtained (amplifier input capacitance=400pF). Z_{opt} is computed from E_n/I_n at each frequency of interest (4kΩ at 1kHz, 1kΩ at 100kHz). E_n and I_n measurements were made on individual FETs using an amplifier similar to the second stage shown in Figure 1.

The low frequency -3dB point for this amplifier occurs at 500Hz; it can be reduced by increasing the size of the three 1μF coupling capacitors. The high-end -3dB frequency depends greatly on the source impedance. Rolloff occurred at 1.3MHz for a 50Ω source and at 350kHz for 1kΩ source. The harmonic distortion of a 2kHz pure sinusoid was measured to be .02% (75dB down at the first harmonic).

This amplifier was modeled using SPICE with the FET model parameters shown below:

.MODEL J2N5434 NJF(VTO=-2.5,BETA=15E-3,LAMBDA=0.021,CGD=35PF,CGS=35PF)
.MODEL J2SK152 NJF(VTO=-2.0,BETA=8.5E-3,LAMBDA=0.046,CGS=9PF,CGD=4PF)

With these parameters, SPICE predicted the system gain within 10% and the -3dB points within a factor of two.

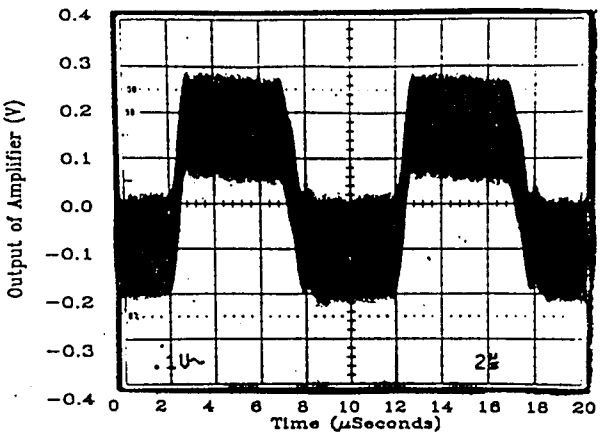

Figure 3a: Amplified SQUID Output
(Commercial Amplifier Gain=10,000 V/V)

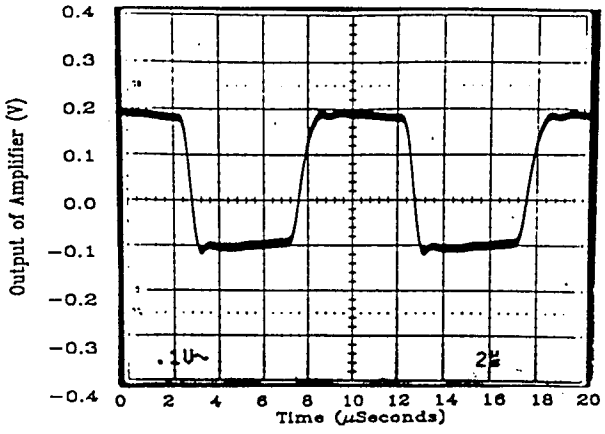

Figure 3b: Amplified SQUID Output
(Amplifier Presented Gain=10,000 V/V)

5. SQUID Application

Best results in a SQUID application are typically obtained by using a cryogenic transformer or tank circuit to couple a dc SQUID to the room temperature amplifier. However, in many cases it is useful to couple to the superconductive detector with little or no impedance transformation. We have employed the amplifier described above for measurements on dc SQUIDs with no impedance transformation.

The amplifier is used in two modes of operation. First, the intrinsic noise of a SQUID which has an output voltage noise density greater than 0.4nV/Hz can be measured. Second, a SQUID can be operated as a magnetometer using linearizing feedback electronics. In this mode of operation the low noise amplifier serves as the preamplifier.

In the feedback (flux-locked) mode of operation the SQUID is flux modulated at 100 kHz. This process up-converts the SQUID's output to 100 kHz where noise contributions from the electronics are smaller. Figure 3 shows the modulated SQUID signal (30μVpp typical SQUID output) using two different types of following amplifiers. The noise as seen in Figure 3a is dominated by the following amplifier (low noise commercial amplifier with $4nV/\sqrt{Hz}$). The noise as seen in Figure 3b (our design) is dominated by the intrinsic noise of the SQUID. Both situations used identical gain and filtering. The result of Figure 3b allows operation of this particular SQUID as a linear magnetometer at noise level of $5\mu\Phi_0/\sqrt{Hz}$ without a transformer. Additionally, the amplifier's dynamic range, bandwidth and slew rate are all adequate to follow the modulation signal as well as the expected input signal to the SQUID.

6. Conclusion

We have designed and built a low noise amplifier well suited to use with superconductive detectors. It yields a measured performance of E_n= 0.33 $nV/\sqrt{Hz}$, I_n = 335 $fA/\sqrt{Hz}$, a maximum bandwidth of 1.3MHz, and a noise impedance of 1kΩ at 100kHz. A flux-locked noise of $5\mu\Phi_0/\sqrt{Hz}$ was obtained using this amplifier with a thin-film dc SQUID.

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