Practical Operation of Cryogen-Free Programmable Josephson Voltage Standards

R. E. Schwall, *Senior Member, IEEE*, D. P. Zilz, J. Power, C. J. Burroughs, P. D. Dresselhaus, and S. P. Benz, *Fellow, IEEE*

***Abstract*—Cryogen-free operation is rapidly becoming the preferred implementation of most superconducting electronics systems including programmable Josephson voltage standard (PJVS) systems. There are strong operational incentives for using the smallest possible cryocooler in order to minimize acoustic noise, system footprint, and power consumption. In addition, $Nb/Nb_xSi_{1-x}/Nb$ junction technology, which operates near 4 K, offers better yield than $NbN/TiN_x/NbN$ technology, which can operate at 8.5 K, thus making lower temperature operation near 4 K desirable. As junction density increases, however, self-heating of the junctions can create significant thermal gradients between the arrays and coldhead. Thus careful design of the overall system is required to maintain acceptable operating margins. We have developed a calorimetric measurement technique to characterize the system variables and used it to evaluate several different PJVS configurations. This technique uses the PJVS subarrays as both heat sources and temperature sensors, in conjunction with a time gated measurement technique, to characterize the thermal response of the system. A passive thermal filter incorporating a Pb thermal mass is used to reduce the temperature oscillations of the cryocooler. Our results suggest that, with appropriate system design, operation of a practical 10 V PJVS on a small (nominally 100 mW capacity at 4.2 K) cryocooler may be possible.**

***Index Terms*—Josephson arrays, quantization, standards, superconducting device packaging, superconductor-normal-superconductor devices, voltage measurement.**

I. Introduction

JOSEPHSON voltage standards are by far the most widely used superconducting electronic systems with a significant number of Josephson junctions, having ∼100 systems deployed worldwide [1]. The increased cost and problematic availability of liquid helium have made cryogen-free operation of these systems more attractive at the same time that higher voltage (∼10 V) PJVS systems have increased the system thermal budget. While these issues can be addressed by the use of NbN-based circuits operating at higher temperatures [2] or higher capacity cryocoolers [3], cost, convenience, circuit yield, and laboratory environmental (noise, rejected heat) issues argue for the use of lower capacity refrigeration systems operating near 4 K.

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R. E. Schwall, C. J. Burroughs, P. D. Dresselhaus, and S. P. Benz are with the National Institute of Standards and Technology (NIST), Boulder, CO 80305 USA (e-mail: schwall@boulder.nist.gov).

D. P. Zilz is with Taylor University, Upland, IN 46989 USA.

J. Power is with California Polytechnic State University, San Luis Obispo, CA 93407 USA.

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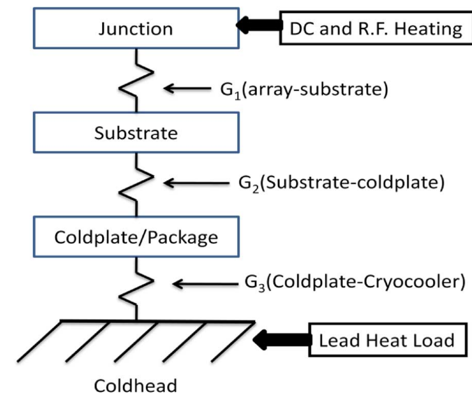

Fig. 1. Block diagram of thermal circuit with definition of thermal conductances.

The operation of a 10 V PJVS system on a small cryocooler presents a number of interrelated and often conflicting design requirements. We have attempted to address these in a systematic manner through the development of calorimetric measurement and analysis techniques that allow many of the thermal impedances in the system to be determined and controlled. The results of these measurements are used to suggest design rules for a cryocooled 10 V PJVS system utilizing a low power cryocooler.

II. Design Approach and Measurements

The thermal design constraints can be illustrated by use of the simple block diagram of Fig. 1. We address the items beginning at the bottom of the diagram.

A. Cryocooler

The cryocooler must provide sufficient cooling power at a temperature somewhat below the JVS operating temperature to remove heat from DC and microwave power dissipation on the chip plus parasitic loads. The superconducting material used for the junctions on the chip (e.g; Nb or NbN) determines the maximum practical operating temperature. The design of the junctions and the temperature gradients between the junctions and the coldhead in turn determine the required coldhead temperature. This can be compared with the published or measured cryocooler load curve (Fig. 2) to determine whether a particular cryocooler has sufficient capacity.

B. Temperature Stabilization (Coldplate)

The coldhead temperature of Gifford McMahon cycle coolers varies at the operational frequency, typically from 1 Hz to 1.5 Hz. For temperatures below ∼10 K, the amplitude of this

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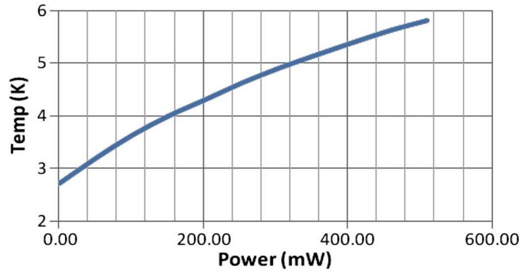

Fig. 2. Measured load Curve of Sumitomo RDK-101D cryocooler used in this study. First stage temperature of the cryocooler was ~ 35 K.

TABLE I
TEMPERATURE STABILIZER PERFORMANCE

Mean $T_{coldhead}$ (K)	$\Delta T_{coldhead}$ (mK p-p)	$\Delta T_{coldplate}$ (mK p-p)
3	250	46
4	400	50
6	686	61
8	1120	90

temperature variation increases with the load on the cryocooler (see Table I and [4]). This temperature oscillation produces a variation in the junction critical current and a corresponding reduction in the voltage step height, or the current range over which the step is constant. To minimize this effect, one normally uses a passive thermal filter consisting of the coldplate specific heat and a thermal impedance between the coldplate and the 4 K stage (coldhead) of the cryocooler. This reduces the amplitude of the temperature oscillations at the coldplate by the factor

$$\frac{\Delta T_p}{\Delta T_c} = \frac{1}{1 + \frac{\omega C}{G_3}}$$

where ΔT_p and ΔT_c are the amplitudes of temperature oscillations at the circuit package and coldhead, respectively, ω is the operating frequency of the cryocooler, C is the heat capacity of the coldplate, and G_3 is the thermal conductance between the coldplate and the cryocooler. For fixed ω, the best temperature stability is clearly obtained by maximizing C and minimizing G_3. However, there are limits to both quantities.

The most effective approaches to increasing C are incorporating a reservoir of liquid helium [4] or a rare earth alloy such as Er_3Ni [3], into the coldplate. These approaches, however, add some system cost and complexity. The use of Pb, which has a relatively high volumetric heat capacity even in the superconducting state [4], is somewhat less effective but simpler. The introduction of the thermal impedance $1/G_3$ increases the steady state temperature of the package to

$$T_p = T_c + \frac{Q}{G_3}$$

where Q is the heat dissipated by the chip plus the parasitic heat load. Thus the minimum useable G_3 is limited by the cryocooler load curve, the circuit operating temperature, and the total heat load.

We have constructed two versions of the passive filter. For measurements performed on a 5 V PJVS [5], C consists of a ~0.75 kg Pb block sandwiched between copper plates. (~0.36 kg of Cu.) G_3 is adjusted by varying the thickness of a stainless steel shim between the cold plate and cryocooler and, use of a 0.9 mm thick shim yields $G_3 \sim 0.15$ W/K at 4 K. In a prototype 10 V PJVS system, C is augmented by an additional 0.61 kg of Cu. The performance of the 5 V system is given in Table I where the ΔT values are the peak to peak temperature oscillations of the coldplate and coldhead.

Methodology for minimizing the heat input due to conduction-cooled leads was developed over 50 years ago [6] and has been revisited numerous times [7]–[12]. In the present system, two stainless steel coax leads and 24 phosphor bronze twisted pairs are thermally anchored on the first and second stage of the cryocooler. The heat load on the second stage is 7 mW per coax and 160 μW per DC pair, for a total lead heat load (I^2R plus conduction) of ~18 mW. The thermal anchor at the cryocooler second stage ensures that the leads conduct no heat to the chip itself.

C. Chip Packaging

NIST has developed and implemented a system of flexible cryo-packages for all of our Josephson systems. This "flip-chip on flex" technology has proven microwave performance, service life, and ability to withstand repeated thermal cycles [13]. We have maintained this packaging approach for the cryogen-free system in order to leverage these advantages and to allow the same circuit to be repeatedly mounted and measured on a cryocooled coldplate or in a cryoprobe operated in liquid helium. This approach requires, however, the use of a demountable high thermal conductance interface between the substrate and the coldplate. The design and evaluation of this interface is discussed below.

III. THERMAL IMPEDANCES

A. Overview

As seen from Fig. 1, the aggregate thermal conductance from the junction arrays to the coldplate, and hence the junction temperature, is determined by the combination of G_1, G_2 and an impedance dependent upon the bulk thermal conductivity k of the silicon substrate. The latter impedance can be thought of as a spreading resistance for heat distribution. In the following sections we characterize each of these.

B. Measurement

An aggregate thermal conductance, which includes G_1, G_2 and a contribution from the thermal conductivity of the substrate itself, has been determined by first calibrating the critical current versus temperature for each subarray, then using one subarray on the chip as a heater and measuring the critical current and hence temperature of the other subarrays.

Since the chip temperature, and thus the subarray critical current, varies at the cryocooler frequency due to the temperature oscillations, the critical current measurements must be gated to the temperature variation to obtain consistent results. This is accomplished by use of a signal from the coldhead thermometer readout to trigger the DMM measuring the critical current. When combined with extensive low-pass filtering on the dc bias lines and on most thermometer leads, as well as an external magnetic shield, this technique yields a critical current repeatability of ± 10 μA, which corresponds to a temperature repeatability of ~4 mK. In the thermal conductance determination, 120 mW is applied to one array and this increases the

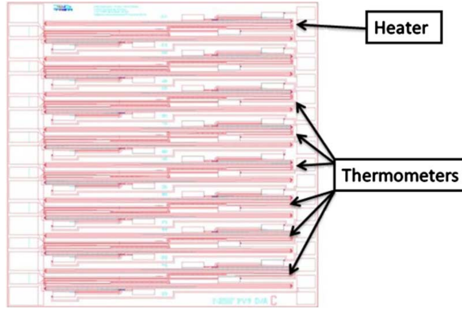

Fig. 3. Layout of 5 V chip. Size is 1 cm by 1 cm. In this example, heat is input through the top horizontal array, and the temperature across the chip is measured through the remaining arrays.

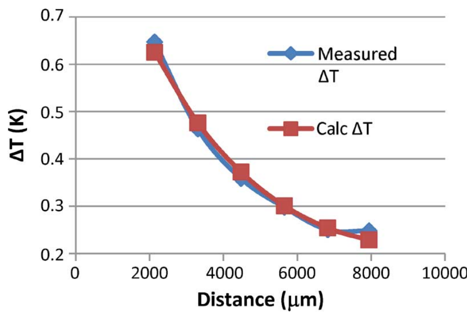

Fig. 4. Thermal gradients measured and calculated from ANSYS model. RMS temperature difference between data and calculations was usually <20 mK and always <60 mK.

temperature of the other arrays by ∼0.4 K to ∼1.2 K, so the temperature measurement precision is more than sufficient.

C. Analysis

Because a subarray cannot be used as a heater and thermometer simultaneously, it is not possible to directly measure G_1. Fortunately, sufficient information is available to allow optimization of the system design by use of a simple anisotropic thermal conductance model.

This model, which is implemented in the finite element program ANSYS, assumes that the arrays have perfect thermal conductance to the substrate, which, in turn, has a uniform isotropic thermal conductivity.[1] G_2 is modeled as a surface thermal impedance h times the area of the substrate and the coldplate temperature is measured directly. With heat applied to one array, as in Fig. 3, the temperatures of five to nine (depending on chip design) other arrays are measured and the curve of temperature versus distance from the heater is fit in the ANSYS model by varying G_2 and the Si thermal conductivity k as parameters in the model. Typical data and their resulting fit are shown in Fig. 4. The results are summarized in Table II. ΔT is the calculated temperature difference between the heated array and the coldplate.

[1]Commercial software and instruments are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the equipment identified are necessarily the best available for the purpose.

TABLE II
SUMMARY OF THERMAL CONDUCTANCE DATA

ρ_{Si} (Ω·cm)	Trench Depth (nm)	AuPd	k_{Si} (W/(m·K))	$h_{sub\text{-}CP}$ (kW/(m^2·K)	$\Delta T_{array\text{-}CP}$ (K)
2.4	167	No	60	1.35	0.90
46800	129	No	220	1.85	0.65
40000	125	No	220	2.70	0.45
~45000	182	Yes	125	2.55	0.47
2.7	173	No	86	1.6	0.76

D. G_1 (Array-Substrate)

Previous work [14] has demonstrated that G_1 depends critically on the interface between the Nb base electrode and the Si substrate. In particular, a layer of SiO_2 between the substrate and the Nb base electrode was found to degrade G_1. The substrates used in this study are thermally oxidized Si with a SiO_2 layer 150 nm thick on the surface. The Nb base electrode is deposited in a trench etched into this oxide to enhance the thermal contact. Although in some samples as much as 25 nm of oxide remains in the trench, this does not appear to significantly affect the measured conductivities. It is observed, however, that temperature measurements are somewhat more erratic on samples with shallow trenches.

E. Thermal Conductivity of the Substrate

Literature values for the thermal conductivity of Si at 4 K vary from ∼20 to ∼400 W/m K [15]. The devices tested here have been fabricated on two different classes of Si: p-type with a resistivity of 10 to 20 $\Omega \cdot \mathrm{cm}$, and "high-purity" Si with a resistivity of $\sim$ $45\ \mathrm{k}\Omega \cdot \mathrm{cm}$. Data in Table II indicate that the thermal conductivity values measured are consistent with the literature and that the use of high-purity Si significantly reduces the overall temperature gradient.

F. G_2 (Substrate-Coldplate)

As noted above, one of our design constraints is to retain the existing NIST packaging in a demountable configuration that allows testing of the same device in liquid He and on a cryocooler. This precludes soldering the chip directly to the coldplate, although this technique is known to provide good thermal contact [2], [16]. Materials such as vacuum grease or semiconductor heatsink thermal compound can provide adequate thermal contact at low temperature for interfaces of identical materials. However, they have a glass transition between room temperature and 85 K that yields a brittle interface, which is subject to disruption by shear forces when used between materials with different total thermal expansion, such as Si and Cu [17]. For this work, we have used a simple pressed indium bond as the interface. An indium foil, 0.127 mm thick, is cleaned with acetone and loaded above its yield stress (∼2.2 MPa) by use of a spring-loaded pressure foot employing a "ball to flat plate" arrangement, which precludes the application of moments or shear stress to the interface. Some variation in G_2 with pressure is observed, but this has not been systematically studied.

In order to assess the effect of the SiO_2 layer on the back of the substrate, the SiO_2 has been stripped from the back of one

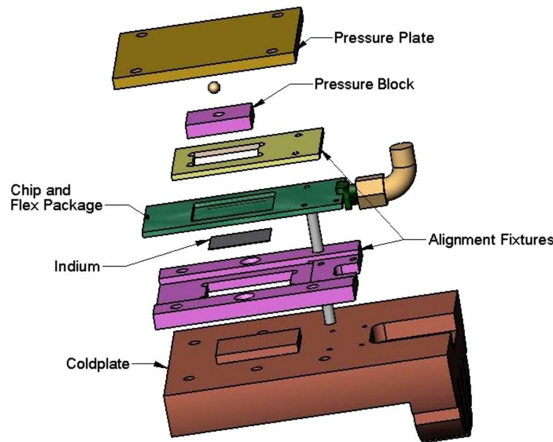

Fig. 5. Cryocooler fixture for 10 V JVS chip. The coldplate adds ~0.61 kg of Cu to the thermal mass of the temperature stabilizer. Alignment is maintained by 0–80 screws which pass through the alignment fixtures and flex package and are threaded into the coldplate. Applying pressure via the combination of the flat plate and ball ensures that only vertical force, i.e. no shear or moment is applied to the chip.

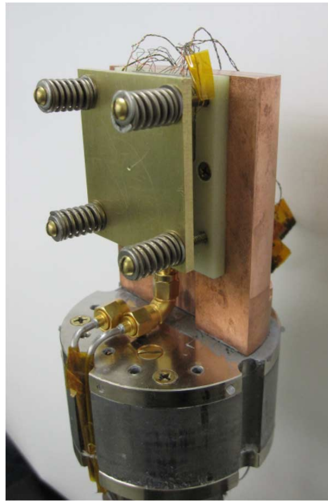

Fig. 6. 10 V JVS package mounted on RDK-101D cryocooler with Pb temperature stabilizer. Four sets of coaxial coil springs provide a total force of 440 N to the interface.

device and replaced by a layer of AuPd ~120 nm thick. This does not dramatically affect the thermal conductance.

G. 5 V PJVS

To verify the above results, two additional experiments have been performed using the 5 V chips. In the first, using a chip represented by the fourth line of Table II, a total of 120 mW is applied to three arrays at one end and two at the opposite end of the chip to simulate, as closely as possible, the uniform heating expected in actual operation. A center, unheated, array is used to measure ΔT. The result, 0.502 K, is in reasonable agreement with the predicted ΔT of 0.47 K from Table II as would be expected unless the "spreading resistance" of the silicon substrate was the dominant thermal impedance.

To demonstrate operation of a PJVS chip on the cryocooler, a 5 V chip, which has thermal properties equal to the first line of Table II has been measured. The chip operates successfully with the temperature stabilizer at 5 V and produces 1 mA margins at an estimated junction temperature of 4.7 K.

TABLE III
THERMAL BUDGET FOR 10 V PJVS

DC Load 10ma, 10V	0.1 W
RF load	0.1 W
Leads	0.017 W
Total	0.217 W
Cryocooler temperature	4.35 K
Delta T (array to coldhead)	0.432 K
Array Temperature w/o temperature stabilization	4.78K

H. 10 V PJVS

Figs. 5 and 6 show the mounting fixture for the NIST 10 V JVS package. This is a larger format (12 mm × 17 mm) chip, hence the heat flux, when operating at 10 V, is approximately the same as that of the 1 cm^2 chip operating at 5 V. Table III presents the thermal budget for this system using the RDK-101D cryocooler and the thermal properties of a chip employing deep trenches, high purity Si and AuPd backside coating.

IV. CONCLUSION

We have developed a sensitive calorimetric technique for measuring and modeling the thermal performance of PJVS systems operating on a cryocooler, and have demonstrated its accuracy by operating a 5 V PJVS system. This technique can be employed to optimize array dissipation and thermal interface design by providing a direct calorimetric determination of on-chip heat generation and individual thermal impedances. Predictions from the model indicate that it should be possible to operate a 10 V PJVS system on a small cryocooler with array temperatures near 5 K, although this may require modification of the temperature stabilization approach e.g. increasing C and G_3.

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