A Dual-Stage Low-Noise Amplifier for 24 GHz Using Packaged p-HEMTs

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***Abstract*--Few amplifier designs exist at 24 GHz which employ the use of inexpensive, packaged components. A design is presented which uses commonly available components and construction techniques to achieve a noise figure of 2.0 dB and 14 dB of gain.**

I. Introduction

Amateur Radio communications systems operating in the microwave region are typically used for narrowband (4 kHz FM or SSB) operation in a point-to-point arrangement. The challenge of these systems is to achieve radio communication over the greatest distance possible. Activity is emerging on the 1.2 cm (24 GHz) band. The majority of equipment being used at present consists of modified digital microwave radios.

A key problem with custom designed circuits at 24 GHz is the limited availability of off the shelf components. Most of the components available for 24 GHz operation are un-packaged dies. Without specialized, expensive equipment, the use of such devices is impractical.

The circuit presented in this paper employs the NEC NE32984D p-HEMT. This device is available from distributors such as Mouser and free samples can be obtained from California Eastern Laboratories (CEL), a division of NEC. Its usual function is that of the front end of a low noise amplifier in Ku band (14 GHz) digital satellite television systems.

A low noise amplifier (LNA) significantly improves the performance of most radio communications systems. To facilitate the construction of a transceiver at 24.192 GHz, a dual stage LNA has been designed using the NE32984D. This paper details the design, construction, and testing of that LNA as part of a senior design project at the University of California, San Diego (UCSD). Input and output matching networks were designed for optimal noise figure on the first stage, and optimal gain on the second stage. Bias circuit decoupling lines and DC blocks were also designed to complete the amplifier.

The circuit was constructed on a10 mil Duroid 5880 PTFE substrate. RF connections to the board were made using 3.5mm SMA coaxial connectors mounted on a custom test fixture.

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II. Design

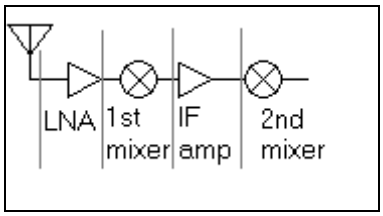

Figure 1. Downconverter Architecture

A. Specifications

The key figures of merit for a downconversion system are the system noise temperature and system gain. For the purposes of this circuit, the downconversion system consists of a low noise amplifier followed by a mixer, an IF amplifier, and another mixer (see Figure 1). This dual conversion architecture permits the use of widely available and high quality VHF single sideband receivers.

A low noise front end with high gain results in the reduction in noise contributed by the following stages. [1] Adding an amplifier is based on the need to increase G_1 and decrease F_1 in

$$F_{sys} = F_1 + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 \cdot G_2} + \cdots + \frac{(F_n - 1)}{G_1 \cdot G_2 \cdot G_3 \cdot \ldots \cdot G_{n-1}}$$

where

$$F_n = 10^{\frac{NF}{10}}$$

Based on typical device specifications and for simplicity, we set out to build at most a dual stage LNA. Our goal was 12 dB of gain and 2.0 dB noise figure. We found that by adding a low noise amplifier with the given specifications, we improve the system noise figure by approximately 10 dB.

Two systems are analyzed, on using a passive mixer, the other uses an active mixer.

Table 1 lists the figures of merit for the low noise amplifier, the passive and active mixers, the IF amplifier, and the 2nd mixer.

Item	G (dB)	G (mag)	NF (dB)	NT(K)	F
LNA	14 dB	25	2 dB	170 K	1.58
Active mixer	3.3 dB	2.13	13 dB	3705 K	19.9
Passive mixer	-12 dB	0.063	10.5 dB	2964 K	11.22
IF amp	14 dB	25	1 dB	75 K	1.26
2nd mixer	7.7 dB	5.9	12.7 dB	5110 K	18.6

Table 1. Figures of merit for system components.

The noise figures and gains in table 1 were either measured (in the case of the LNA) or taken from manufacturer data sheets. The rest of the figures were determined by the following

$$F_n = 10^{\frac{NF}{10}}$$
$$T = 290K \cdot [F - 1]$$
$$G(mag) = 10^{\frac{G(dB)}{10}}$$

For the passive mixer case, we have

$$F_{rcv} = 11.220 + \frac{(1.260-1)}{0.063} + \frac{(18.600-1)}{0.063 \cdot 25}$$
$$F_{rcv} = 26.524$$
$$T_{rcv} = 290 \cdot [26.524 - 1]$$
$$T_{rcv} = 7402K$$
$$NF = 10\log(F)$$
$$NF = 14.24dB$$

When a low noise amplifier is added, we obtain

$$F_{rcv} = 1.580 + \frac{(11.220-1)}{25} + \frac{(1.26-1)}{25 \cdot 0.063} + \frac{(18.600-1)}{0.063 \cdot 25 \cdot 25}$$
$$F_{rcv} = 2.6$$
$$T_{rcv} = 290 \cdot [26.6 - 1]$$
$$T_{rcv} = 464K$$
$$NF = 10\log(F)$$
$$NF = 4.15dB$$

The increased performance is significant. The noise temperature decreases by 6938K resulting in just under 10 dB of improvement in the noise figure (NF).

For the active mixer,

$$F_{rcv} = 19.9 + \frac{(1.26-1)}{2.14} + \frac{(18.6-1)}{2.14 \cdot 25}$$
$$F_{rcv} = 20.35$$
$$T_{rcv} = 290 \cdot [20.35 - 1]$$
$$T_{rcv} = 5612K$$
$$NF = 10\log(F)$$
$$NF = 13.085dB$$

Again, with the LNA we have

$$F_{rcv} = 1.580 + \frac{(19.9-1)}{25} + \frac{(1.26-1)}{25 \cdot 2.14} + \frac{(18.6-1)}{2.14 \cdot 25 \cdot 25}$$
$$F_{rcv} = 2.35$$
$$T_{rcv} = 290 \cdot [2.35 - 1]$$
$$T_{rcv} = 393K$$
$$NF = 10\log(F)$$
$$NF = 3.7dB$$

We improve the noise temperature dramatically, this time by 5219K. The noise figure also receives a nearly 10 dB improvement.

The minimum discernable signal (MDS) is one of the important factors used in determining the maximum range of the transceiver. In our system, we maintain that the minimum discernable signal is a signal which yields a 10 dB signal to noise ratio (SNR) after downconversion. A typical microwave contact is completed between two transceivers located on mountain peaks. The noise received by the system is chiefly ground noise. Since the antennas (typically a 0.3m diameter paraboloid) are pointed at the horizon, roughly half of the 'view' is that of ground noise. The contribution from ground noise is roughly half that of the temperature of the ground. Since the ground is roughly 300K, the ground noise contributes approximately 150 K of noise.

Since we already have the receiver additive noise temperature, we can simply add the antenna noise and receiver noise to arrive at the system noise temperature.

T_{sys}=150K + 392.6K. = 542.7K

The total received power is given by [2]

$$P_{noise} = kT_{sys}B$$

where k is Boltzman's constant, T_{sys} is 542.7K and B is 4000 (the bandwidth for an analog SSB voice channel). This gives us a noise power of -135 dBm. This yields an MDS of P_{noise}+10dB = -125 dBm.

A simple link budget calculation shows that with a 100 mW transmitter, 30% relative humidity, and 0.3m dishes, a link of 100 km is possible. With an effective radiated power ERP of +55 dBm (+20 dBm into a 35 dB gain parabolic antenna), a path loss of -180 dB (80 dB of atmospheric attenuation and 100 dB of free space loss), a signal of -125 dBm appears at the antenna of the receiving station [3]. This results in a 10 dB signal to noise ratio, plenty to sustain a Morse code contact, and on the verge of being able to hold a single sideband channel. On cooler, drier days, the 80 dB of atmospheric loss should drop considerably, possibly by 10 dB or more.

B. *Advanced Design System*

Agilent Technologies' *Advanced Design System 1.3* (ADS) was used to perform all computer calculations, simulations, optimizations, schematic capture, and layout. Dr. Asbeck and the UCSD High Speed Devices Group made ADS available to us for the duration of this project. ADS allowed us to import device S-parameter files and noise data in order to produce stability measures, noise and gain circles, matching networks, bias networks and other microstrip structures, schematics, and the final PC board layout. We were also able to import S-parameter data files from the HP 8510B during testing to quickly produce charts of our results. ADS was crucial to our success and utilized during every step of the design process.

C. *Transistor Selection*

The process of finding potential transistors and selecting the appropriate device for our LNA became much more time-consuming than expected. Our goal was to select a device with enough gain at 24 GHz to enable a single or dual stage amplifier design and meet our design requirements of 12dB gain with 2.5dB noise figure. Few packaged transistors are commercially available that have S-parameter and noise data published by the manufacturer past 18 GHz. Apparently packaged devices are difficult to reliably characterize above this frequency due to the varying parasitics of the ceramic or metal package and bond wires from one device sample to another. The particular type of transistor suitable for 24GHz operation is the psuedomorphic Hetero-Junction Field Effect Transistor (p-HJFET), a type of High Electron Mobility Transistor (HEMT). A survey of available packaged p-HEMT devices yielded four possibilities, the Fujitsu FMM5701LG, the Stanford Microdevices SPF-1576, the NEC NE32584C, and the NEC NE32984D.

In deciding whether a particular p-HEMT is right for an LNA design, many factors are important. For our design, we used the following: cost, availability of the device, availability of measured characteristics at 24GHz, gain, noise figure, package type, and stability. Cost was an important factor because our funding was limited and we were not positive we would not destroy a few devices in the construction and testing processes. The availability of free samples from the manufacturer was a strong selling point for a device. Device availability became a significant issue due to the short duration of the project and the long lead times in obtaining device samples from some manufacturers. To enable the use of computer simulations and hand calculations, tables of device characteristics, particularly S-parameters and noise data at 24 GHz, were necessary. A high gain and low noise figure were desirable, though not at the cost of significant instability. Packaged devices with wire leads were necessary for ease of hand construction. All of the devices considered came in similar ceramic or metal surface mount packages. Stability was an issue we did not expect at the time we began device selection, but quickly became one of the key factors we used to make our final FET choice.

The S-parameters of a particular device may be used to determine if it will be stable in a particular circuit. As derived by Gonzalez [4], the following stability measures are commonly used and are based on the S-parameters of a device at a particular frequency of interest.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11}S_{21}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

The necessary and sufficient conditions for stability are:

$$K > 1 \quad \text{or} \quad K > 1$$
$$|\Delta| < 1 \qquad\quad B > 0$$

In the following discussion the second set of conditions will be utilized. The Agilent Advanced Design System was used to find K and B for each transistor. If the conditions given are met, the device is "unconditionally stable" and will not oscillate for any input or output matching network that exhibits a reflection coefficient inside the Smith chart ($\Gamma < 1$). Otherwise the transistor is "conditionally stable" or "unstable" and may oscillate under some matching conditions. These conditions may be viewed graphically using stability circles [4]. These stability circles are circles on the Smith chart which represent regions for the input and output matching networks where the transistor will be unstable. A larger area of the Smith chart encompassed by these circles results in a less stable transistor which will be more difficult to match properly. We used ADS to plot the stability circles for each device. A device with K close to 1 and B greater than zero is fairly simple to match and therefore was a preferred candidate in our transistor selection.

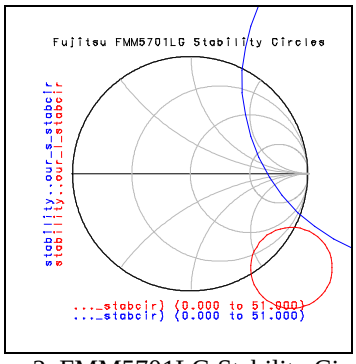

Figure 2. FMM5701LG Stability Circles

An ADS plot of the stability circles for the Fujitsu FMM5701LG are shown in Figure 2. The unstable regions of the Smith chart lie within these circles in this case, although this is not always the case. ADS has the facility to

determine which side of the circles are stable. The FMM5701LG is somewhat unstable (K = -0.096 and B = 0.481) resulting in a large portion of the Smith chart being unusable. This made the Fujitsu device a less attractive option.

The following table summarizes the key factors involved for each transistor studied.

Device	Cost/Avail.	Data?	G (dB)	NF (dB)	*K/B*
FMM5701LG	$25/Yes	Yes	16.8[1]	2.0	-0.096/0.481
SPF-1576	?/Yes	Yes	6.68[2]	1.25	1.636/1.125
NE32584C	$6/Yes	No	N/A	N/A	N/A
NE32984D	$0/Samples	Yes	13.8[1]	1.44	0.953/1.318

$MAG = \frac{|S_{21}|}{|S_{12}|}(K \pm \sqrt{K^2 - 1})$ when $K \geq 1$.

$MSG = \frac{|S_{21}|}{|S_{12}|}$ when $K < 1$.

Ultimately the NEC NE32984D was selected since it exhibits almost unconditional stability at 24GHz, enough gain to make a dual stage amplifier with over 12dB gain possible, a low noise figure, and can be sampled for free. California Eastern Labs (CEL) kindly donated several to our project and was extremely receptive to our requests for parts and specifications. A series of plots showing the stability circles, gain, noise figure, *K* and *B* factors for the NE32984D is included in this report (Figure 3).

D. Bias Circuitry

Biasing the depletion mode devices used in this project requires great care. The function of the bias circuitry is to provide a DC coupled connection between a voltage source for the gate, and a DC coupled connection to a current source for the drain. Another requirement is that the bias circuitry not interfere with the portion of the circuit operating at 24.192 GHz. The structure in Figure 4 illustrates the bias network used in the design. It consists of three 1/4 wavelength high impedance lines with two radial stubs. The 1/4 wavelength lines were initially calculated by hand, taking into account the effective dielectric constant of the 10 mil Duroid substrate. The effective dielectric constant of the circuit board was found [1] to be

$$\lambda_{eff} = \frac{c}{f \cdot \sqrt{\varepsilon_r}}$$

$$\varepsilon_r = \frac{\varepsilon_{eff}}{\varepsilon_0} = 1.96$$

$$\lambda_{eff} = 0.89cm$$

$$\frac{\lambda}{4} = 0.223cm$$

$$0.223cm \cdot \frac{1mil}{0.00254cm} = 88mils$$

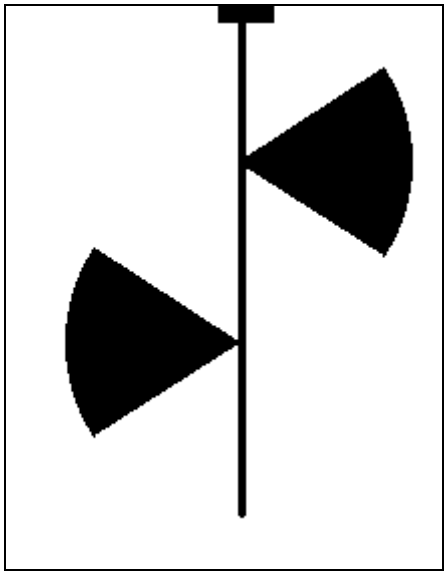

Figure 4. Bias network DC coupling segment

The radial stubs are actually radial transmission lines with a radius of a quarter wavelength. The values for the quarter wavelength line were adjusted slightly during the simulation process, although the optimum values were only two to three mils off from predicted. The bias DC coupling network functions as follows. The high impedance lower end of the structure is attached perpendicular to the 50Ω transmission line. A quarter wavelength up the high impedance line, the first radial transmission line branches off. At this point, the 24 GHz signal sees a short circuit to ground, thus reflections are minimized. At this point, lower frequency noise couples into the radial transmission line and is shorted to ground at the end. The radial transmission line acts as a capacitor at frequencies other than 24 GHz, at which it is a short. The same occurs with the next pair of quarter wave line and radial stub. At the end of the 3/4 wave line, the 24 GHz signal sees a short circuit to ground, keeping it away from bias circuitry.

At the end of the bias coupling networks is a shunt 1000pF capacitor and a series safety resistor. The resistor for the gate supply is 1kΩ, while the drain resistor is 100Ω. These resistors help to limit the maximum FET current, as well as help to dampen high frequency noise. The function of the capacitor is to AC couple the bias line to ground to reduce high frequency noise entering the bias circuits.

The DC bias supplies have been left for a future design, however there are a large number of very good designs available. For the purposes of testing we used current limited lab supplies.

A bias point of V_{DS} = 2V and I_{DS} = 20mA for each NE32984D was selected as a fair tradeoff between gain and noise figure.

E. DC Blocking Coupled Lines

In order to isolate the bias of one stage from the next stage as well as our test equipment, the transmission line must be AC coupled. Capacitors at 24 GHz are extraordinarily small, requiring wire bonding or silver epoxy. Additionally, they are difficult to find and somewhat expensive. Interstage coupling and DC isolation is accomplished through the use of a quarter wave coupled line structure. Figure 5 illustrates the coupled line element. Using Agilent Technologies' Advanced Design Suite, the dimensions of the element were optimized for 24.192 GHz. Limiting the performance is the capability of the printed circuit board manufacturer. We were limited in our design to a 4 mil separation and 6 mil wide lines.

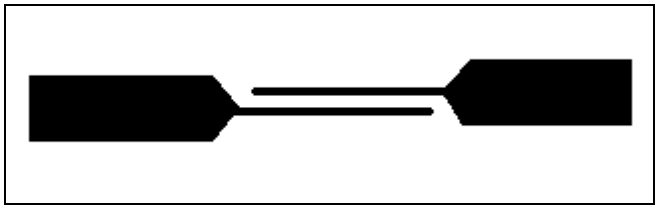

Figure 5. The coupled line element

ADS reported that the coupled line elements would have virtually no transmission loss, but that their S_{22} and S_{11} would be approximately 0.2. This was enough to effect the matching networks as described later.

Connecting the circuit to the network analyzer, as well as to other components in the radio system is accomplished using 3.5 mm SMA style connectors. Using an air dielectric, these connectors are suitable for use through 26.5 GHz. Other connectors were investigated, including Teflon dielectric SMA (good only through 18 GHz) and 2.92 mm 'K' connectors, good through 50 GHz. The decision to use 3.5 mm connectors was largely based on availability and ease of construction.

F. Matching Networks

The input and output matching networks of each stage of a low noise amplifier determine its overall gain, noise figure, and stability. Most amateur LNA designs at microwave frequencies contain little or no matching circuitry because simulation tools such as ADS are hard to come by at the hobby level. In most published amateur designs, small copper tabs referred to as “snowflakes” are moved around the microstrip lines of the amplifier until the desired gain/noise figure is achieved. They are then soldered into place. For this project, the sophistication of the design was increased in order to incorporate matching networks into fabricated PC board. We desired to take full advantage of the tools available to us by using them to assist us in designing custom matching networks for noise and gain performance.

The gain of a single stage transistor amplifier is a function of three variables. The first is the S-parameters of the transistor at each frequency of interest. The second and third are the source and load reflection coefficients, Γ_S and Γ_L, presented to the transistor by its matching networks. The purpose of a matching network is to transform the 50Ω characteristic impedance of the input and output of the amplifier to the desired Z_S and Z_L values for each transistor. These Z_S and Z_L values determine Γ_S and Γ_L through the relationship

$$\Gamma = \frac{Z - Z_O}{Z + Z_O}$$

As shown in Figure 6, there are four reflection coefficients and associated impedances involved in the matching circuit design. Γ_{IN} and Γ_{OUT} are the input and output impedances of the transistor, while Γ_S and Γ_L are the impedances looking into the matching networks on the source and load side of the amplifier. A full derivation of amplifier gain as a function of these parameters appears in the reference by Gonzalez[i].

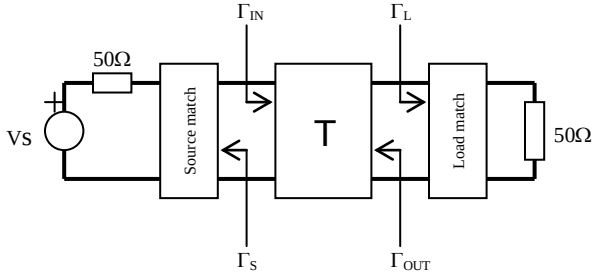

Figure 6. Reflection Coefficients

The particular impedances used in our design were been chosen using a systematic method detailed by Gonzalez[ii] and modified to take advantage of the S-parameter analysis and optimization features of ADS. A basic matching network at 24 GHz consists of a series and shunt microstrip stub along the transmission lines leading to the input (gate) and output (drain) of each transistor. The lengths of these stubs can be adjusted to match from 50Ω to any point on the Smith chart, and vice-versa. Figure 7, appended to this report, shows the positions of the matching stubs in a single stage amplifier. The basic procedure for determining the lengths of the stubs is as follows:

1. Plot the gain and noise circles for the device.
2. Pick the desired point on the Smith chart for each stage, based upon the gain/noise tradeoff.
3. Use the Smith chart to find the microstrip stub lengths L1s and L2s to match the chosen Γ_S to 50Ω. This forms the basis for the source matching network.
4. Optimize the chosen lengths L1s and L2s in ADS, taking into account the effects of the coupled lines and bias networks. ADS will return more corrected values for the lengths.

5. Using ADS, find Γ_{OUT} of the transistor with the source matching network in place.
6. Use the Smith chart to find the lengths L1l and L2l for the load matching network stubs that match Γ_{OUT}^{*} to 50Ω for a conjugate match. This becomes the load matching network.
7. Optimize the chosen L1l and L2l in ADS to find actual values.

A plot of the gain and noise circles for the NE32984D with V_{DS} = 2V and I_{DS} = 20mA is attached to this report (Figure 8). This plot shows the various possibilities for source matching on the Smith chart. The tradeoff between noise and gain performance is illustrated by the concentric circles which represent various gain and noise figure values. Two source matching points were chosen using this chart, one for high gain and one for low noise. The low noise match will be used in the first stage of our optimal dual stage amplifier, while the high gain match will be used in the second stage where noise is less critical. The points chosen are given below.

Match	**Gain (dB)**	**NF (dB)**	**Admittance (*Y_O = 1/50Ω)**
Gain	12.0	2.20	0.318 – j0.350
Noise	9.0	1.37	0.985 + j0.054

After following the procedures detailed above, the final results of the design process for both gain and noise matching are summarized below.

Match	**L1s (mils)**	**L2s (mils)**	**L1l (mils)**	**L2l (mils)**
Gain	99.9	45.1	151.7	38.0
Noise	28.2	7.7	197.1	7.7

Several variations of different stages with assorted matching networks are included in the final PCB artwork. These include three types of single stage amplifiers, utilizing a match for optimum noise figure, a match for high gain, and no match at all. These single stage amplifiers were intended to be used for troubleshooting purposes if the dual stage amplifiers did not work. To form a dual stage amplifier, two single stages were simply cascaded. Two variations of dual stage amplifiers are also included in the layout. The most important of these is a design utilizing a match for noise on the first stage and a match for gain on the second stage. This version is the most significant since it includes all of the design procedures we developed and was intended to have the best performance of all the designs. A dual stage amplifier with no matching is also included in the layout.

Our ADS simulations predicted the matched dual stage LNA to have a gain of 18.29dB and a noise figure of 1.96dB.

G. Layout

Layout of the circuit board was done using ADS as an export tool. The final layout is seen in Figure 9.

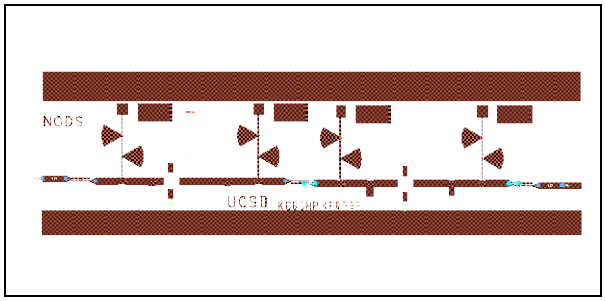

Figure 9. Final layout of the optimum dual stage amplifier.

III. CONSTRUCTION

Construction of the circuit board began with the transfer of the design to a local printed circuit board manufacturer. Approximately a week later the boards arrived. A photograph of the printed circuit board appears in Figure 10. Each sub-circuit was cut out of the main board with scissors. Since we were unable to obtain sufficient funding for a circuit board with plated vias, we drilled holes by hand for grounding. To ground the source leads of the transistor, the leads were bent such that when the device was mounted to the board, they would poke through slots in the substrate. Next they were soldered to the groundplane on the opposite side of the board. Figure 11 illustrates this arrangement.

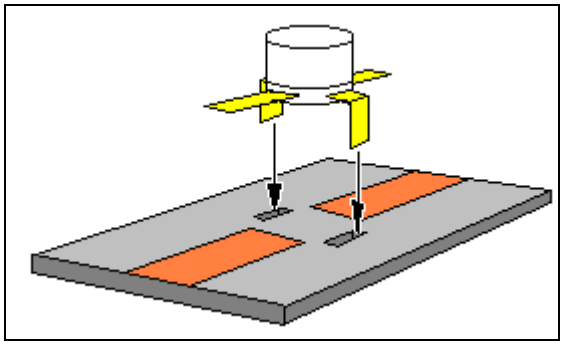
Figure 11. Device mounting detail.

Aluminum test fixtures were fabricated to hold the circuit boards in place and provide a mechanical support for the edge mounted coaxial connectors. Another benefit of the test fixtures was that it allowed for rapidly changing the circuit being tested. Figure 12, appended to this report, illustrates the test fixtures.

During testing we found that the source grounding was not adequate and the circuit began to oscillate. With the addition of small wires parallel to the source leads, this problem was eliminated.

IV. Testing

Testing was performed in the UCSD High Speed Devices Lab. The following amplifier boards were prepared for installation in the test fixtures for testing: single stage unmatched, single stage matched for gain, dual stage unmatched, and dual stage matched for gain. A straight 50Ω microstrip board was also prepared.

The test setup for all the amplifier boards tested can be divided into two sections, bias and RF. To set the bias for each transistor, two lab power supplies are used. One supplies a negative voltage V_{GS} to the gate of the transistor to be biased, while the other provides a positive drain voltage V_{DS}. The negative gate voltage is necessary because the NE32984D is a depletion mode device and requires a gate voltage of –1V to fully turn it off. The safety resistors on the gate and drain bias pads help to reduce the risk of destroying any FETs during bias setup and normal operation. The 1kΩ gate resistor presents an insignificant voltage drop to the gate bias since the gate of these FETs draws very little current. The 100Ω drain resistor, however, must be considered in our calculations. At I_{DS} = 20mA, there is a 2V drop across the drain safety resistor. Thus, for V_{DS} to be 2V, 4V must be supplied to the drain bias pad. However, this voltage may not be applied before sufficient current is flowing through the drain resistor, because the breakdown voltage of the NE32984D is on the order of 4V. Therefore, the drain voltage must be applied in steps and the gate voltage reduced during each step to careful arrive at the desired bias point without exceeding the transistor's ratings. The process of stepping bias voltages was quickly mastered during testing and presented little difficulty to us. Eventually we hope to design a circuit to bias the transistor automatically from a dual rail supply voltage.

The RF test setup consisted of a spectrum analyzer capable of 0 – 50 GHz, an HP 8510B network analyzer capable of 0 – 40 GHz, and associated cables, adapters, and 3.5 mm connectors. Calibrating the 8510B for 0.5 – 26.5 GHz testing proved to be a significant hassle and consumed most of our time in the lab.

The spectrum analyzer was used to check for oscillations in each amplifier before S-parameter testing. We found that some of our single and dual stage amplifiers oscillated at frequencies on the order of several GHz when powered up for the first time, while others did not. The oscillations could be eliminated by physically pressing down on the transistor, most likely indicating a poor ground connection to the source leads. To solve these oscillation problems, wires were inserted through the printed circuit board next to the two source leads of the transistors. These wires were then soldered to the source leads and the ground plane of the PCB. This made a better ground connection to the transistors and permanently eliminated the oscillations.

Each amplifier was then connected to the HP8510B network analyzer and S-parameter test set. The output power level of the 8510 was set to approximately–23dBm. A bias of V_{DS} = 2V and I_{DS} = 20mA was applied to each transistor. The gain and noise matched optimal dual stage amplifier was tested first and worked on the first attempt, producing 13dB gain at 24.2 GHz. This was later raised to 14dB by tweaking the mounting screws of the test fixture. Plots of the measured S-parameters for the matched dual stage amplifier appear in Figure 13, appended to this report. Figure 14 shows the simulated parameters for the same amplifier. The measured gain (S_{21}) at 24.2 GHz is 4dB lower than the simulated gain, but the overall shape of the each gain curve in the measured data is quite similar to our simulations. Many of the same resonances appear in both plots. We hope to perform a more detailed analysis of our results in the future.

By varying the applied bias from V_{DS} = 2V and I_{DS} = 20mA to V_{DS} = 3V and I_{DS} = 30mA, 1 dB additional gain was observed. Under normal bias conditions the amplifier has gain from 17 GHz to 25.5 GHz, so it is fairly broadband.

The measured S-parameters for the 50Ω line appear in Figure 15.

Unfortunately, we were unable to perform any noise figure tests. We do not presently have access to any noise figure measuring equipment capable of measurement above 18 GHz. In the future we hope to test the noise figure of the optimal dual stage amplifier with the help of the Amateur Radio community.

V. Conclusion

We accomplished our goal of designing a low noise amplifier for 24 GHz with a minimum 12dB gain and 2.0dB noise figure. The low noise amplifier presented in this paper exceeded our gain specification by 2dB. While we did not have the facilities to test the noise figure, we expect that it is likely within a dB of our predicted value. Future testing will involve a noise figure test, a two-tone linearity test, and fine tuning of the matching networks.

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VII. REFERENCES

[1] Paul Shuch et al., eds., The ARRL UHF/Microwave Experimenter's Manual, (Connecticut: ARRL press, 1991)

[2] Simon Ramo, John V. Whinnery, and Theodore Van Duzer, Fields and Waves in Communications Electronics (New York: John Wiley & Sons 1994)

[3] Rick Campbell et al., eds., The ARRL UHF/Microwave Projects Manual 1st ed., 1 vol. (Conecticut: ARRL press, 1994)

[4] Guillermo Gonzalez, Microwave Transistor Amplifiers (Upper Saddle River, NJ: Simon & Schuster 1997): pp. 217, 221-22, 257, 260.

[5] Al Ward, "Inexpensive Components for 24 GHz" Proceedings of the Microwave Update 1998, (1998): pp. 246-256

[6] Edwards, Marion Lee. “A Deterministic Approach for Designing Conditionally Stable Amplifiers.” IEEE Transactions on Microwave Theory and Techniques 43.7 (1995): pp. 1567-1575.