INTERSIL

ICL7650
CHOPPER STABILIZED OPERATIONAL AMPLIFIER

FEATURES

- **Extremely low input offset voltage — 1 μV over temperature range**
- **Low long term and temperature drift of input offset voltage**
- **Low D.C. input bias current — 10pA**
- **Extremely high gain, CMRR and PSRR — min 120dB**
- **High slew rate — 2.5V/μS**
- **Wide bandwidth — 2MHz GBW product**
- **Internally compensated for unity gain operation**
- **Very low intermodulation effects (phase shift <10°)**
- **Clamp circuit to avoid overload recovery problems, allow comparator use**
- **Extremely low chopping spikes at input and output**

GENERAL DESCRIPTION

The ICL7650 chopper stabilized amplifier is a high performance device designed to be used in a wide variety of applications. This amplifier offers exceptionally low offset voltage and input bias parameters combined with excellent bandwidth and speed characteristics. Intersil's unique approach to chopper stabilized amplifier design, using Intersil's well established CMOS process, yields a versatile precision component which can replace more expensive hybrid or modular parts, while out-performing them and other monolithic devices.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier that spends alternate clock phases nulling itself and the main amplifier. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs. These are the only external components necessary.

The clock oscillator and all of the other control circuitry is entirely self-contained. However, the 14-pin version includes a provision for the use of an external clock if required for a particular application. In addition, the ICL7650 is internally compensated for unity gain operation.

ORDERING INFORMATION

TEMP RANGE	PACKAGE	ORDER #
0°C to 70°C	14pin plastic	ICL7650CPD
−20°C to 85°C	14pin CERDIP	ICL7650IJD
0°C to 70°C	8pin TO-99	ICL7650CTY
−20°C to 85°C	8pin TO-99	ICL7650ITY
−55°C to 125°C	14pin CERDIP	
−55°C to 125°C	8pin TO-99	

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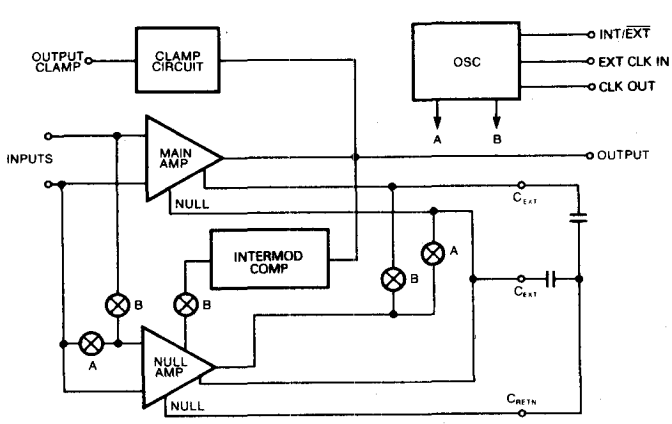
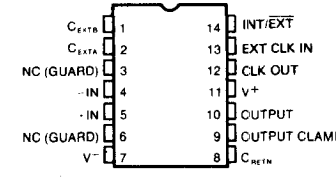
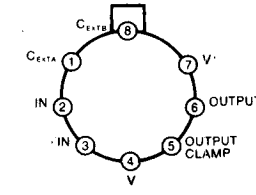
FIG. 1 BLOCK DIAGRAM



PIN CONFIGURATION



(outline dwg JD, PD)



(outline dwg TO-99)

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... 18 Volts
Input Voltage .....V^+ +0.3 to V^- −0.3 Volts
except EXT CLOCK IN: ... V^+ +0.3 to V^+ −6.0 Volts
Storage Temp. Range ..... −55°C to 150°C
Operating Temp. Range ..... −20°C to 85°C
(C series ..... 0°C to +70°C)
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on control pins ..... V^+ to V^-
Duration of Output short ckt ..... Indefinite
Current into any pin 10mA
—while operating ..... 100 μA

Cont. Total Power Dissipn (T_A =25°C)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW
TO-99 ..... 250 mW

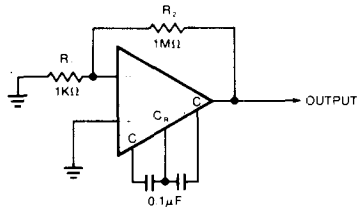
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS: Test Conditions: V^+ = +5V, V^- = −5V, T_A=25°C, Test Ckt (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input Offset Voltage	V_{OS}	T_A=25°C over operating temp. range (note 1)		±0.7 ±1.0	±5	μV
Average Temp. Coefficient of Input Offset Voltage	$\Delta V_{OS}/\Delta T$	over operating temp. range (note 1)		0.01		μV/°C
Input Bias Current (doubles every 10°C)	I_{BIAS}	T_A=25°C 0°C<T_A<+70°C −20°C<T_A<+85°C		1.5 35 100	10	pA
Input Offset Current	I_{OS}	T_A=25°C		0.5		pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ	1	5		V/μV
Output Voltage Swing	V_{OUT}	R_L = 10kΩ		±4.8		V
Common Mode Voltage Range	CMVR		−5.0	−5.2 to +2.6	+2.3	V
Common Mode Rejection Ratio	CMRR	CMV = −5V to +2.3V	120	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ± 7.5V	120	130		dB
Input Noise Voltage	e_n	R_S=100Ω 0 to 10Hz		2		μVp-p
Input Noise Current	i_n	f=10Hz		0.01		pA/√Hz
Unity Gain Bandwidth	GBW			2.0		MHz
Slew Rate	SR	C_L=50pF, R_L=50Ω		2.5		V/μs
Rise Time	t_r			0.2		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		6.0		16	V
Supply Current	I_{SUPP}	no load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	pins 12-14 open (DIP)	120	200		Hz
Clamp ON Current (note 2)		R_L=100K		70		μA
Clamp OFF Current (note 2)		−4.0V<V_{OUT}<+4.0V		1		pA
Offset Voltage vs Time				100		nV/√mnth

NOTE 1: Operating temperature range for M series parts is −55°C to +125°C, for I series is −20°C to +85°C, for C series is 0°C to +70°C.
NOTE 2: See OUTPUT CLAMP under detailed description.

TEST CIRCUIT



DETAILED DESCRIPTION

AMPLIFIER

The block diagram shows the major elements of the ICL7650. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset null capability. The main amplifier is connected full time from the input to the output, while the nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET back gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials, and the necessary nulling loop time constants. The nulling arrangement operates over the full common mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, and is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin (in the case of 14 pin devices) or the V^- pin (in the case of the 8 pin devices). This connection should be made directly to V^- by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry.

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

CLOCK

The ICL7650 has an internal oscillator giving a chopping frequency of 200 Hz, available at the CLOCK OUT pin on the 14 pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{EXT}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT. CLOCK IN pin. At low frequencies the duty cycle of the external clock is not critical, since an internal divide-by-two provides the desired 50% switching duty cycle. However, since the capacitors are charged only when EXT CLK IN is HIGH, a 50–80% positive duty cycle is favored for frequencies above 500Hz to ensure that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between V^+ and GROUND for power supplies up to ±6V, and between V^+ and $V^+ - 6V$ for higher supply voltages. Note that a signal of about 400Hz will be present at the EXT CLK IN pin with INT/$\overline{EXT}$ high or open. This is the internal clock signal before the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a STROBE signal is connected to EXT CLK IN during the time that the unknown signal is applied to the amplifier, neither capacitor will be charged as long as STROBE is low. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

COMPONENT SELECTION

The two required capacitors, C_{EXTA} and C_{EXTB} have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion. A high quality film type capacitor such as mylar is preferred, although a ceramic or other lower grade capacitor may prove suitable in many applications.

PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible to that of the industry standard 8-pin devices, the LM741, LM101, etc. The null storing external capacitors are connected to pins 1 and 8, usually used for offset null, compensation capacitors, or not connected. The output clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset null pot, connected between pins 1 and 8 and V^+, by two capacitors from those pins to V^- will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to V^- is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7650.

TYPICAL APPLICATIONS

Clearly the applications of the ICL7650 will mirror those of other op. amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input offset voltage and bias current, the ICL7650 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figs. 2 and 3. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op. amps by the ICL7650 are the supply voltage (±8V max.) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Fig. 4, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650.

Fig. 5 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current ~ V_{IN}/R without disturbing other portions of the system.

Normal logarithmic amplifiers are limited in dynamic range in the voltage input mode by their input offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be expanded to a voltage input dynamic range of close to 6 decades by using the ICL7650 to offset-null the ICL8048, as shown in Fig. 6. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps, to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

Mixing the ICL7650 with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be met fairly easily, a highly efficient voltage divider can be built using the ICL7660 voltage converter circuit 'backwards'. A suitable connection is shown in Fig. 7.

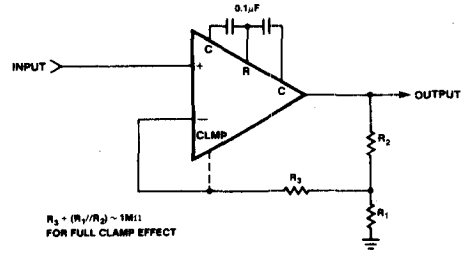


FIG. 2 NON INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

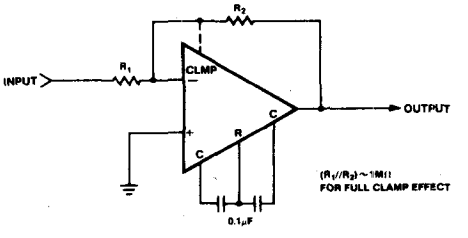


FIG. 3 INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

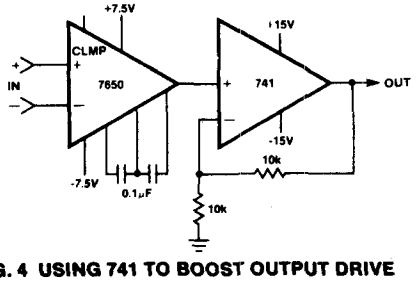


FIG. 4 USING 741 TO BOOST OUTPUT DRIVE CAPABILITY

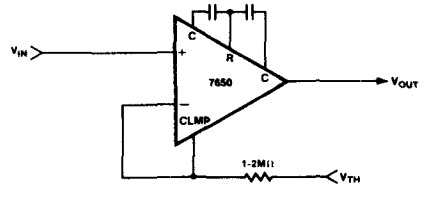


FIG. 5 LOW OFFSET COMPARATOR

STATIC PROTECTION

All device pins are static protected by the use of input diodes. However strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input leakage currents.

LATCH-UP AVOIDANCE

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

OUTPUT STAGE/LOAD DRIVING

The output circuit is a high-impedance stage (approximately 18kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open loop gain is proportional to load resistance. For example the open loop gain will be 17 dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10k or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

THERMO-ELECTRIC EFFECTS

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermo-couple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermo-electric coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage at the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

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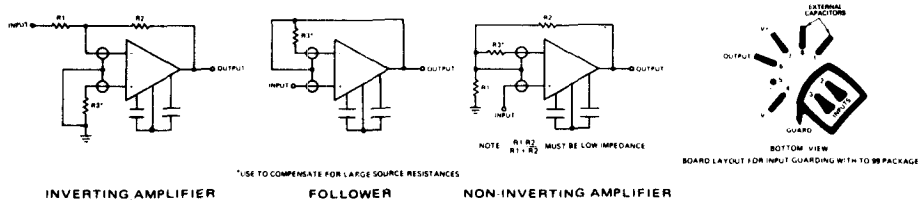
CONNECTION OF INPUT GUARDS



*USE TO COMPENSATE FOR LARGE SOURCE RESISTANCES

INVERTING AMPLIFIER FOLLOWER NON-INVERTING AMPLIFIER

TYPICAL APPLICATIONS (Contd.)

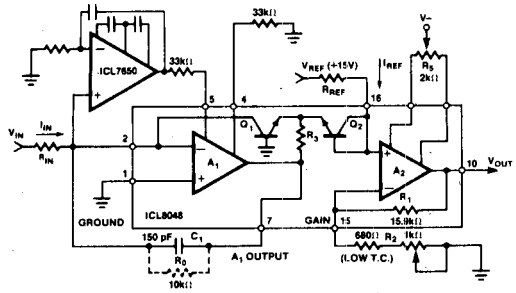


FIG. 6 ICL8048 OFFSET NULLED BY ICL7650

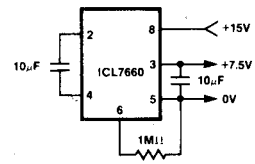


FIG. 7 SPLITTING +15V WITH ICL7660. SAME FOR −15V. >95% EFF.

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