serial number
burden (V · A)
test condition
ratio error
phase error
Print time: 10 s.

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Microcomputer-Based Calibration Systems for Variable Voltage Dividers

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***Abstract*—Two microcomputer-based systems for the calibration of ac and dc multidecade voltage dividers at NRCC are described. They permit the self-checking of the reference standards, the comparison with the test dividers, and the complete processing of the measurement data to be carried out orderly, accurately, and cost-effectively. The uncertainty in the ac voltage ratio calibration of the reference is less than 5×10^{-8} of input at 400 and 1000 Hz. For dc, the 13-bit reference standard can be automatically calibrated with an uncertainty believed to be less than 1×10^{-7} of input.**

INTRODUCTION

THE CALIBRATION of variable voltage ratio devices, such as the Kelvin–Varley divider [1], [2] for dc and the multidecade ratio transformer [3] for ac, can be a time-consuming process. Inasmuch as comparison with a reference standard is a commonly accepted method of calibration [4], [5], the proper maintenance and the periodic recalibration of the standard are important considerations which will add to the processing cost.

In upgrading these calibration services at the National Research Council of Canada (NRCC) recently, two microcomputer-based systems have been designed. These systems integrate the measurements on the reference standard, the comparison with the test divider, and the collection, management, and presentation of the measurement data into a complete and orderly calibration process, so that these services may be furnished more reliably and efficiently.

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AC CALIBRATION

The ac calibration system has evolved from an inductive voltage divider (IVD) comparator circuit [6], [7], and is presented in Fig. 1. Both the standard and the guard IVD are similar, single-stage seven-decade dividers; the test divider is in general a five- to eight-decade IVD. A two-stage 1/10/100 injection transformer, a phase shifter, and a special transformer for the two-phase detector complete the analog circuit. Coaxial chokes are used to reduce troublesome ground-loop currents, where necessary.

By definition, the transfer ratio [8] of a divider is the phasor ratio of the output signal of a divider to its input signal. For example, the three-terminal, true transfer ratio of the test IVD in Fig. 1 is given by

$$G_t = (E_t - E_{t0})/(E_{t1} - E_{t0}). \quad (1)$$

The calibration results can also be expressed as a correction, $a + jb$, to be added algebraically to the dial reading D, i.e.,

$$G_t = D + (a + jb). \quad (2)$$

In this paper, only the corrections for the more significant decade values of D will be dealt with.

The comparator in Fig. 1 may be balanced for a given setting of the test IVD by alternately adjusting the standard and the guard divider settings, D_s and D_g, respectively. Autobalance has not been seriously considered, because i) the test IVD, in all liklihood, has to be set manually, ii) the balance to within 1×10^{-7} of input converges quickly, because adjustments made by means of D_s and D_g are nearly orthogonal, and iii) any imbalance less than 1×10^{-7} will be interpolated by the

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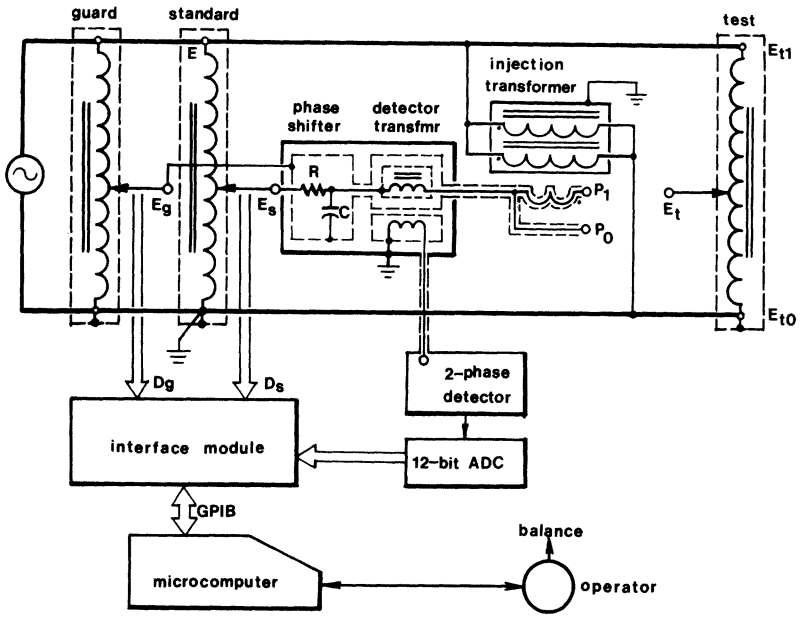

Fig. 1. Micromputer-based calibrator for ac voltage dividers. When connected to test point E_t, probe P_1 includes the secondary of the two-stage injection transformer in the comparison circuit. Probe P_0, however, bypasses the transformer altogether.

two-phase detector. To help achieve quadrature balance, the guard IVD is deliberately offset from the standard to generate a small balancing voltage across resistor R. The balance equation at ω rad/s can be shown to be

$$E_t = E_s + (E_g - E_s)[(\omega CR)^2 + j(\omega CR) - j(\omega CR)^3] \tag{3}$$

when higher order terms of (ωCR) may be ignored. By making $\omega CR = 0.0100$ and normalizing E_t with respect to input E, (3) becomes

$$E_t/E = E_s/E + 10^{-4}(E_g - E_s)(1 + j100)/E. \tag{4}$$

In practice, the phasor quantity $(E_g - E_s)/E$ is replaced in the computation by $(D_g - D_s)$, the difference between dial readings. If the discrepancy is denoted by

$$h_1 + jh_2 = (E_g - E_s)/E - (D_g - D_s) \tag{5}$$

then

$$E_t/E = E_s/E + 10^{-4}(D_g - D_s)(1 + j100) + c(h_1, h_2) \tag{6}$$

the last term being a "system correction" (see below).

To upgrade a basically manual system into a microcomputer-based one the following steps must be taken:

1) Switches of the standard and the guard IVD are fitted with multiplexed 12-position encoders for computer input.

2) Analog outputs of the two-phase detector are multiplexed to a 12-bit ADC, so that a precision of 1×10^{-9} may be obtained. Both the supply voltage and the detector zero offset are monitored.

3) An interface module, including a real-time clock, is built to provide access to the above system via a GPIB or IEEE-488 bus from the computer, through a small set of instructions.

4) Finally, an interactive BASIC program is written to allow the operator to do any one of the following (typical three-decade execution time in brackets):

TABLE I
IVD COMPARATOR SYSTEM CORRECTIONS (SYSCOR)
(in ppm of input)

Ds, Dg	400 Hz	1000 Hz	10,000 Hz*
.X	.002 - j.027	.010 - j.060	.08 - j.60
.9	.010 - j.024	.024 - j.056	.14 - j.54
.8	.010 - j.022	.026 - j.049	.14 - j.49
.7	.011 - j.019	.027 - j.043	.13 - j.42
.6	.011 - j.018	.026 - j.038	.15 - j.35
.5	.011 - j.015	.026 - j.031	.18 - j.26
.4	.011 - j.010	.026 - j.028	.17 - j.21
.3	.009 - j.009	.019 - j.022	.13 - j.15
.2	.006 - j.007	.012 - j.015	.10 - j.11
.1	.002 - j.004	.005 - j.010	.05 - j.08
.0	.001 - j.002	.002 - j.004	.02 - j.02

* Separate guard system.

a) System correction (SYSCOR) determination (10 min): When the test probe P_0 is returned to E_s, with dial setting $D_g = D_s$, the detector directly measures correction c in (6) as SYSCOR (D_s). Being quite small, these corrections (Table I) need only be determined once for the top three individual decades of D_s, if ground admittance remains substantially unchanged for the guard divider.

b) Autocalibration (25 min): The method used is that of "bootstrapping" [9]. A doubly shielded two-stage transformer

is used to inject a stepped-down voltage of 1/10 or 1/100 of input between the detector and the test IVD. Although the step-down ratios need not be exact, they must be stable throughout the autocalibration, hence the need for guarding the secondary winding as shown in Fig. 1. With known SYSCOR, the ratio corrections for the standard (STDCOR) and for the test (TSTCOR) dividers can be directly determined for the top two decades. (Third decade corrections are currently obtained by interpolation only.)

c) *Comparison calibration (18 min):* This method assumes known STDCOR and SYSCOR. It is the usual method for routine calibrations. With a normalized detector imbalance of e_d, each voltage ratio is evaluated as follows:

$$E_t/E = D_s + \text{STDCOR}\,(D_s) + \text{SYSCOR}\,(D_s) + 10^{-4}(D_g - D_s)(1 + j100) + e_d.$$

In addition, the program monitors the supply signal, helps establish correct detector phasing and sensitivities, flags any obvious missetting of dials, computes three- or four-terminal corrections, compares new corrections with stored ones, tabulates results, and issues a calibration report.

Performance of AC System

The ac system has been in service for two years. It is most often used at 400 and 1000 Hz, and occasionally at 1592 and 10 000 Hz. Resistor R is a fixed metal film 680 Ω. For each frequency, a pretrimmed set of capacitors is used to give the required ωRC product. The capacitance C actually includes the intershield contribution from the detector transformer. It can be accurately measured *in situ* (Fig. 2, with R shorted) on a capacitance bridge under the condition that the two-phase detector is also nulled. Thus the ωCR product may be readily realized with an accuracy of 0.2 to 1.0 percent between 400 and 10 000 Hz.

The total uncertainty in a calibration, while dependent on the quality of the test divider and on frequency, is a combination of the uncertainties in SYSCOR, STDCOR, detector linearity, and the constancy of the injection transformer output. The autocalibration uncertainty is estimated to be less than $(0.04 + j0.4) \times 10^{-6}$ at 1 kHz, while the reproducibility of SYSCOR and STDCOR (with different test dividers) is an order of magnitude better. Comparisons with a special single-decade, two-stage transformer [10] at 400 Hz, and with previous calibrations based on a completely different method [3] show agreements to within $(0.03 + j0.1) \times 10^{-6}$ of input at 400 Hz, and $(0.04 + j0.3) \times 10^{-6}$ at 1000 Hz.

For comparison calibrations, it should be noted that the voltage developed across R is determined to an accuracy no better than that of the ωCR product. However, this voltage rarely exceeds 0.003 percent of input at 1 kHz.

At 10 000 Hz, the guard divider is subject to considerable admittance loading from the injection transformer. For better accuracy, a separate guard to drive the midpoint of the secondary shield is recommended. Even then, the uncertainty is estimated to be about $(0.3 + j0.8) \times 10^{-6}$ of input. Such a separate guard is not necessary up to 1 kHz, for the difference rarely amounts to $(0.01 + j0.1) \times 10^{-6}$ of input.

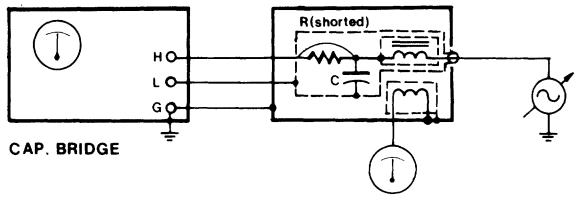

Fig. 2. Circuit for measuring capacitance C in Fig. 1. Correct result is obtained when both detectors are nulled. The auxiliary variable source is usually derived from the calibrator supply.

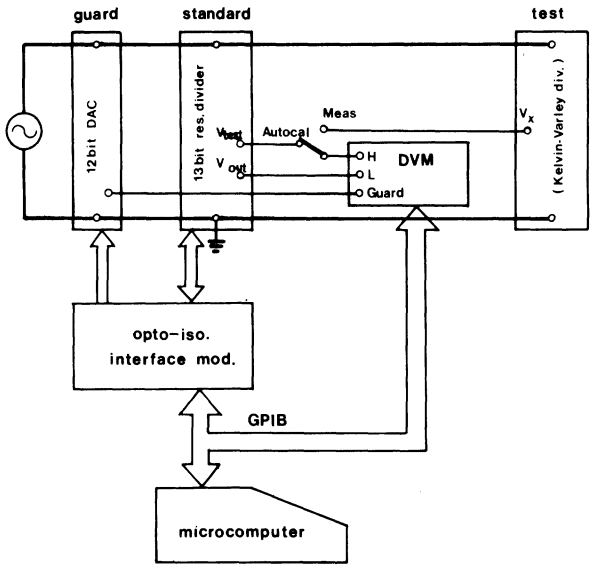

Fig. 3. Microcomputer-based calibrator for dc voltage dividers.

Experience has shown that a three-decade calibration takes 30 to 60 min, resulting in a calibration report containing tabulated corrections.

DC Voltage Ratio Standard and Calibration

The dc voltage ratio calibration system, represented in Fig. 3, bears some resemblance to the ac system. However, the reference standard is a 13-bit resistive divider that employs a new switching technique [11], which can only be gainfully exploited with a computer.

An N-bit resistive divider is shown in Fig. 4. If a binary sequence $S = (S_0 S_1 \cdots S_{k-1} S_k S_{k+1} \cdots S_{N-1} S_N)$ represents the switch positions of the divider, then there exist two such sequences which will give the same nominal division ratio between 1.0 and 0. In particular, to obtain the correction for the kth divider, one measures the change in output V_{out} when the switch code S changes from $(00 \cdots 010 \cdots 00)$ to $(00 \cdots 110 \cdots 00)$. When wiring and contact resistance is negligible compared to the nominal resistance R_{nom}, it is sufficient to make N such difference measurements to completely calibrate the N-bit divider (see [11] for detail).

The 13-bit divider is made up of a set of 100 000-Ω wirewound resistors matched to about 20 ppm. Bistable (latching) relays with 4PDT gold-plated contacts are used with a specially designed and gold-plated circuit board to minimize switching resistance and thermal EMF. Multiple relays are used in parallel for the most significant five switches, and the resistors are terminated close to the circuit pads for the relay contacts.

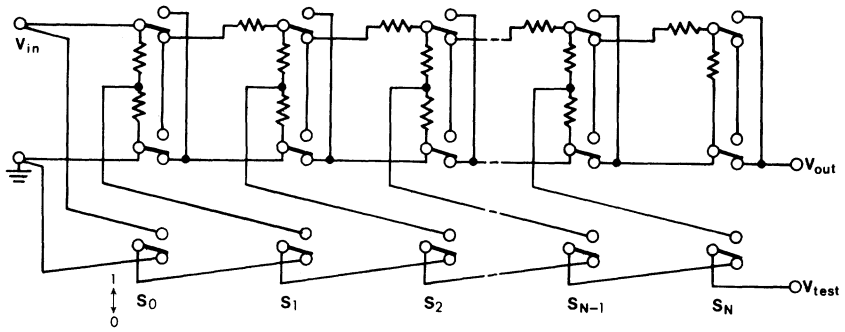

Fig. 4. An N-bit divider (after Cutkosky [11]) where all resistors are nominally equal. Note minor modifications in switching circuit and switch designation.

It is especially important to reduce the wiring, contact, and change in contact resistances to a few milliohms in the most significant stages of the divider.

For autocalibration, the detector or DVM having a linearity of 1 in 20 000 is connected between V_{out} and V_{test}. Let

$$d_{k,1} = (V_{out} - V_{test})/V_{in}, \qquad \text{when } S = (00\cdots010\cdots00) \tag{7}$$

and

$$d_{k,2} = (V_{out} - V_{test})/V_{in}, \qquad \text{when } S = (00\cdots110\cdots00). \tag{8}$$

The parameter of interest for the calibration of the kth and following stages is

$$\Delta_k = d_{k,1} - d_{k,2}. \tag{9}$$

The corrected voltage ratio for a given switch code may be computed from the following recursion formula:

$$V_{out}/V_{in} = \sum_{n=0}^{N} -S_n M_n Q_n \tag{10}$$

where S_n is the logical value of the nth switch (0 or 1)

$$M_n = M_{n-1}(1 - 2S_n), \qquad M_0 = (1 - 2S_0) \tag{11}$$

$$Q_n = (Q_{n-1} + \Delta_n)/2, \qquad Q_0 = 1. \tag{12}$$

The summation terms, if error-free, will be of the form $\pm 2^{-n}$ or 0.

Typical values obtained for Δ_n and Q_n are given in Table II. It can be demonstrated that this method of calibration is not very sensitive to detector offset and loading. For a nominal 10-V input, Δ_n can be determined unambiguously to 0.02 ppm if guarded measurements are made after an appropriate delay in proportion to the change in common-mode voltage (e.g., 10 s for a full-scale change). Under microcomputer control, the entire autocalibration can be done within 3 min resulting in a standard deviation of <0.02 ppm for Δ_n. Faster calibration can be traded for less precision. Daily variation in these corrections can be easily followed.

The two switch codes that will give a nominal voltage ratio $0 < D < 1$ may be constructed as follows:

1) convert ratio D into an equivalent N-bit sequence B;

TABLE II
CORRECTIONS AND CORRECTED RATIOS FOR A 13-BIT DIVIDER

n	Δn	Qn	Qn-2^-n
1	1.04 x 10^-6	.500 000 52	0.52 x 10^-6
2	-4.34	.249 998 09	-1.91
3	9.09	.125 003 59	3.59
4	-0.15	.062 501 72	1.72
5	0.18	.031 250 95	0.95
6	-0.13	.015 625 41	0.41
7	-0.36	.007 812 53	0.03
8	0.02	.003 906 27	0.02
9	0.12	.001 953 20	0.08
10	0.03	.000 976 61	0.05
11	-0.00	.000 488 31	0.03
12	0.02	.000 244 16	0.02
13	-0.01	.000 122 08	0.01

2) form $2B$ (left shift) and $2B - 1$;
3) Convert these into Gray codes which will become the required switch codes for the ratio D.

With this algorithm and with readings from the DVM, the computer can set up the divider to match an unknown ratio within two measuring cycles with a precision of 1×2^{-N}. This is the approach taken for this prototype system.

Experiments with measuring unknown ratios showed that many detectors or DVM's would load the divider to some extent even when guarded measurements were made, the guard voltage being supplied by a 12-bit DAC. If the ground conductance is stable and can be determined with sufficient accuracy, the effect of loading can be compensated. To this end, the output resistance of the divider is also computed according to the switch code. For this 13-bit divider, the worst case output resistance amounts to $3.1R_{nom}$, or 310 kΩ. The ground conductance loading by the detector can be determined *in situ* by introducing a known resistance change in the output circuit of the divider. This can be accomplished by the addition of a

known resistance or by altering the less significant bits in the switch code.

Preliminary measurements against a pretrimmed Kelvin–Varley divider have been carried out with a precision of 2×10^{-8} of input. The measured (and corrected) ratio errors for the first decade of the Kelvin–Varley divider were found to be within 0.1 ppm of input. Some possibilities for improved measurements are being considered: to reduce R_{nom}, to reduce N, and to optically isolate the detector.

Conclusions

The analog circuitry of the ac voltage ratio calibrator places some limits on quadrature range, achievable accuracy at 10 kHz, and non-decade calibrations. On the other hand, the microcomputer-based system has handled numerous calibrations with sufficient accuracy, proven reliability, and very significant saving in man-hours.

The autocalibration facility has been the most positive aspect of the dc binary divider as a reference standard. The high output resistance of the divider has presented some measurement problems to the detector (or DVM) at hand. Correction by computation offers a viable solution.

The use of a microprocessor interface module makes the system available as a GPIB "instrument" to other microcomputers.

Acknowledgment

The assistance of P. Grant in solving many interface problems is gratefully acknowledged.

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A Computer Program for Algebraic Error Analysis of Complex Microwave Systems

BIRTHE GULDBRANDSEN

***Abstract*—The aim of the program is to examine the way in which usually neglected errors of subcomponents influence the scattering elements of a composite system. This is done by determining the Taylor series expansions of the wanted scattering elements, including terms to fourth order in the errors. These formulas are derived by inspection of the scattering diagram of the composite system.**

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Introduction

In recent years, some rather comprehensive error analyses have been carried out by hand on the following subjects: the two-port rotary vane attenuator [1], the four-port rotary phase shifter [2], and the four-port directional coupler [3]. Similar analyses might be of interest in other cases as, for example, the dual six-port analyzer [4]. The initial step common to these types of error analysis is the determination of the Taylor series expansion for the considered reflections and/or

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