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Progress on Cryocooled 2-V Programmable Josephson Voltage standard system at NIM



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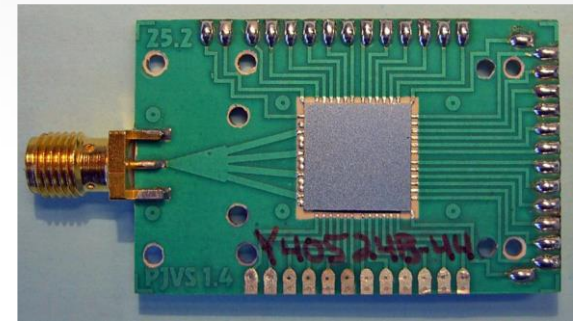
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Josephson Voltage Standards

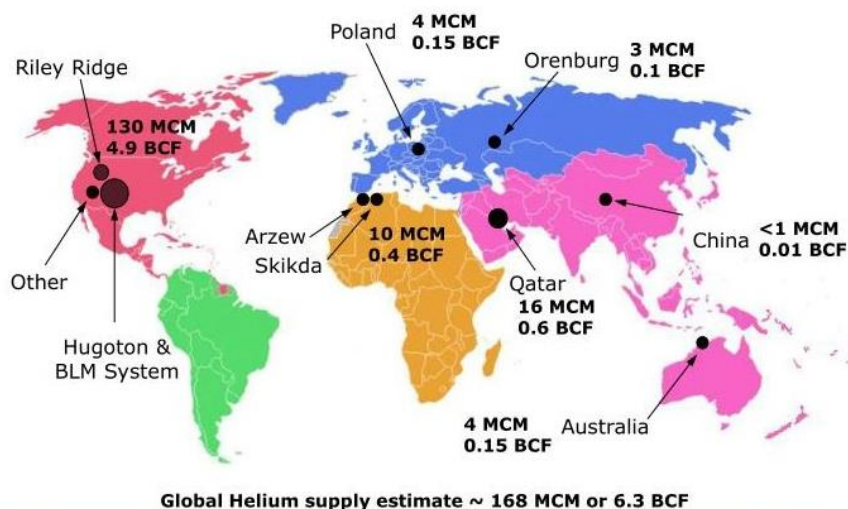
- Provide the volt unit realization
- Very low uncertainty (10^{-9} to 10^{-10})
- Normally use liquid helium to cool the chip
- Dissipation 4~5 liters per day
- Liquid helium shortage (Scarce Resource)
- Increase cost



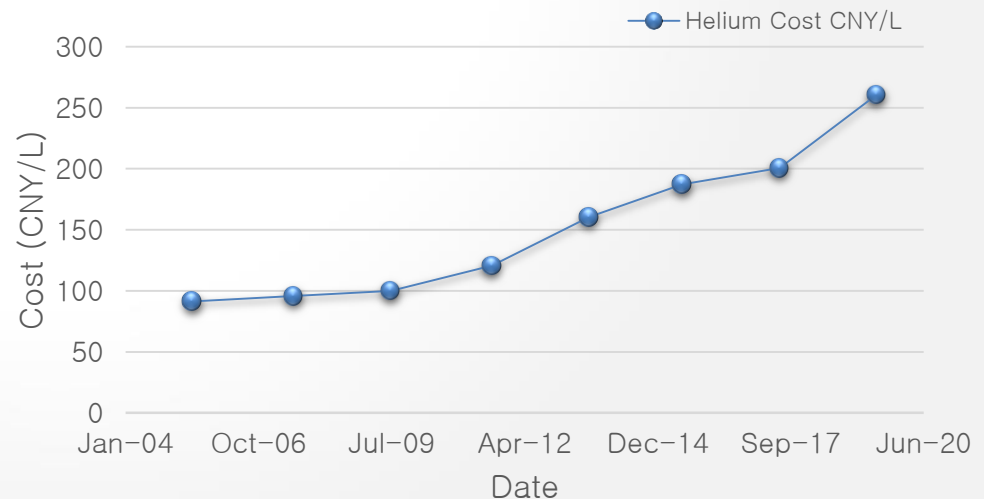
Josephson Junction Array (JJA) chips
↓
DC voltage measurement uncertainty:
 $10^{-9} \sim 10^{-10}$ V/V

Increasing need of Liquid-helium free PJVS system

Liquid Helium Distribution



Cost of liquid helium per liter rises by years



Liquid He:

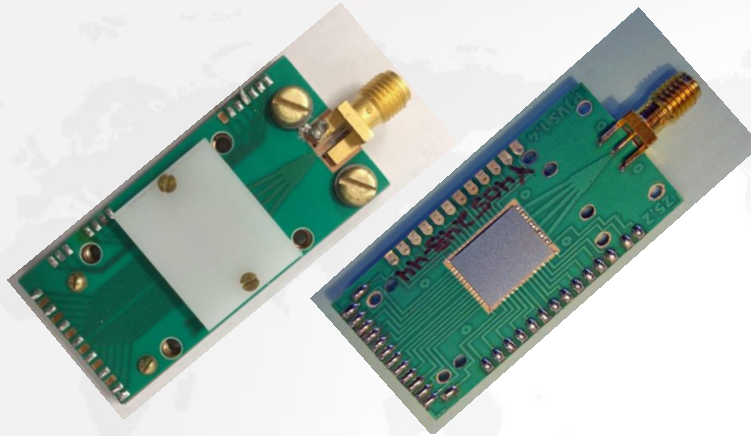


- + Temperature is constant in time
- + Essentially infinite power dissipation
- + Cooldown takes around 20 minutes
- + Chip is always at helium boiling point
- Exorbitant costs
- Hard to obtain in many instances
- Operation at only one temperature

Cryocooler:



- + Low, one-time cost
- + Temperature can be controlled
- + Deployable anywhere with AC power
- + Takes ~2 minutes to expel flux
- Limited cooling power
- Cooldown often longer than 3 hours
- Temperature oscillates in time
- Thermal gradient exists between chip and coldhead



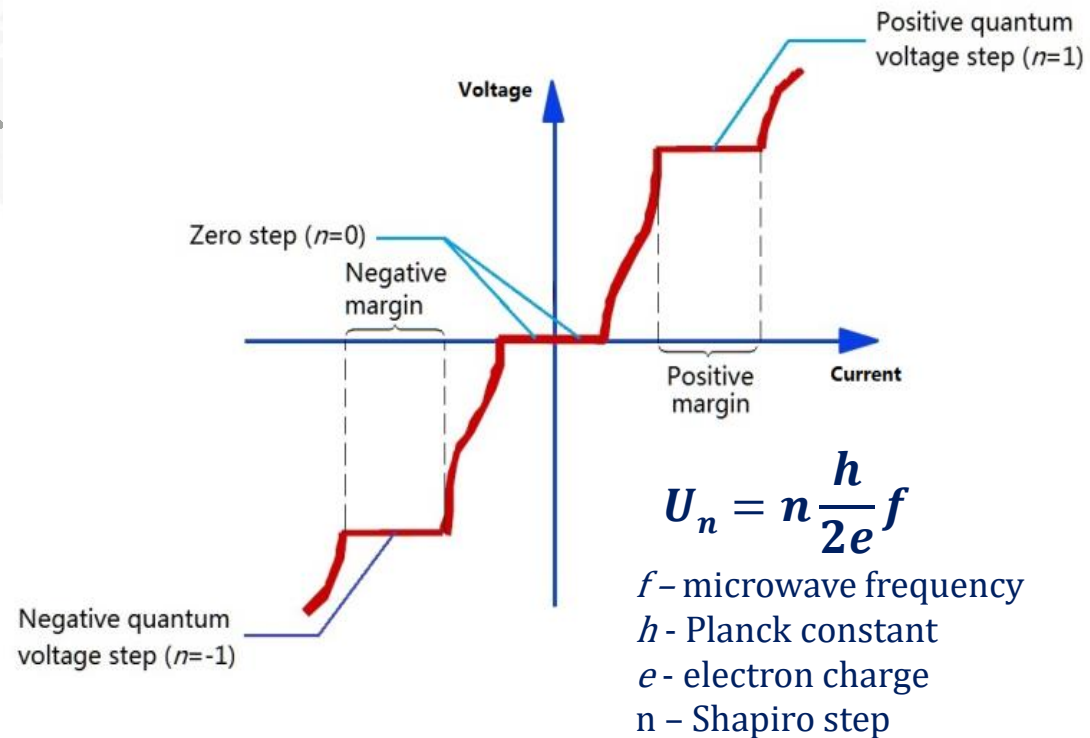
Programmable Josephson array chips



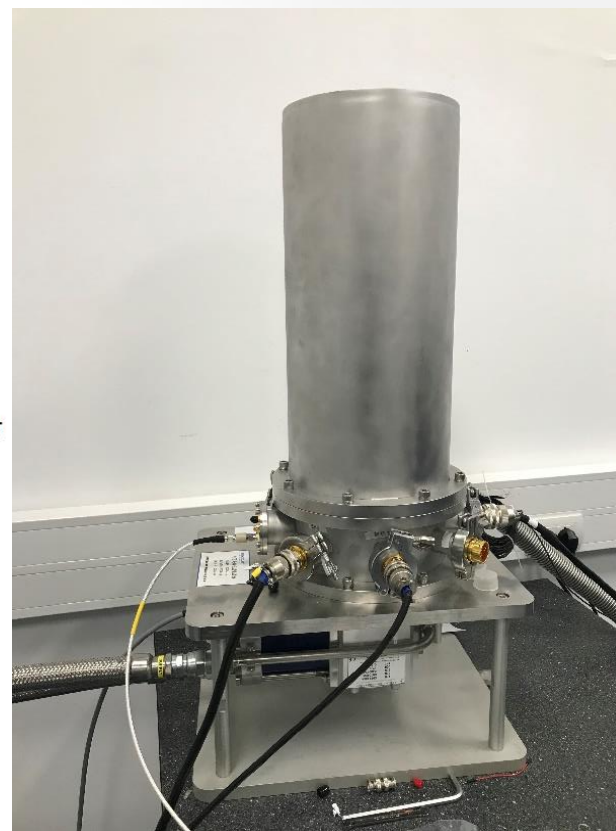
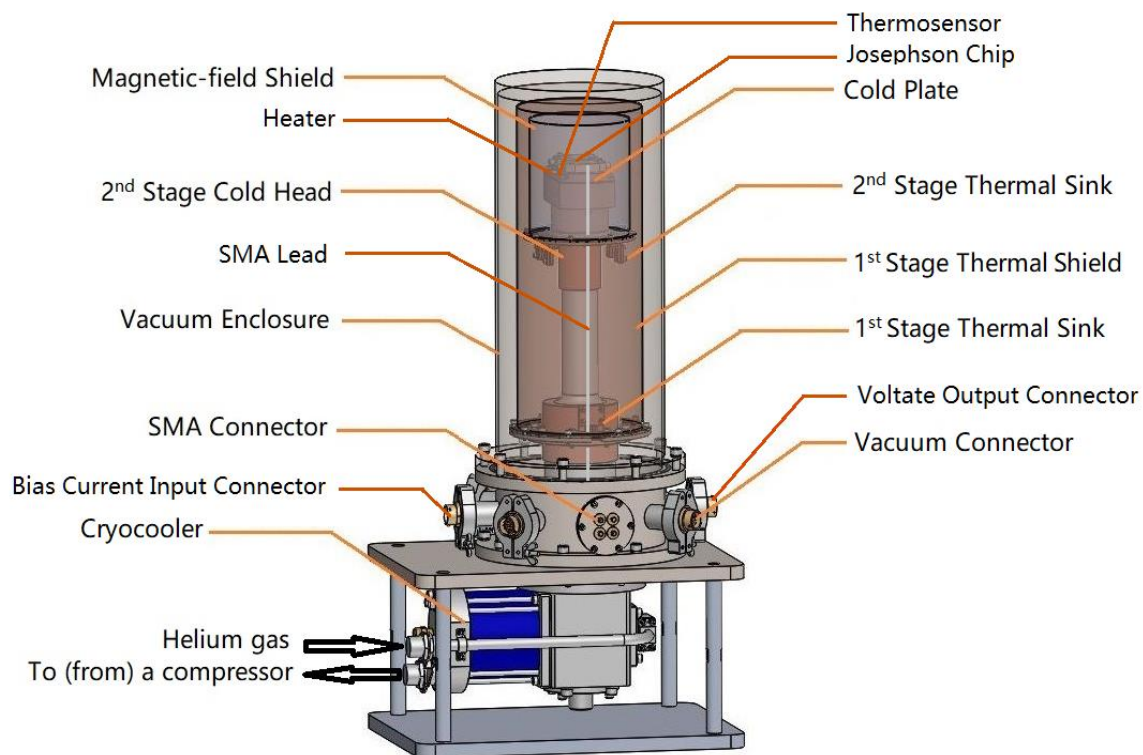
Quantum voltage standard
DC voltage measurement
uncertainty: $10^{-9} \sim 10^{-10}$ V/V

• Goal

- Development of cryocooled PJVS system.
 - Research on domestic cryostat design and its thermal behavior (minimize temperature oscillations and increase temperature stability).
- Investigating the performance of JJA as integrated with the cryopackage.
- Challenge: Extracting the heat dissipation; Reducing the electromagnetic interference coming from the cryogenic system, such as high-power compressor, water chilling unit, molecular pump etc..



- The cryopackage is built with a domestic two-stage G-M cryocooler which provides a temperature floor of around 3.5 K and 1.5 [watt @4.2 K](#) cooling capacity.
- A heater and two thermometers mounted on the second stage are used for temperature control.

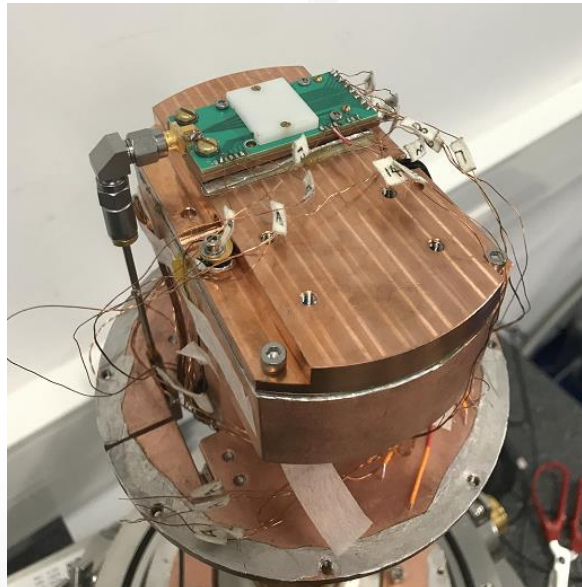


Domestic cryopackage design and its layout

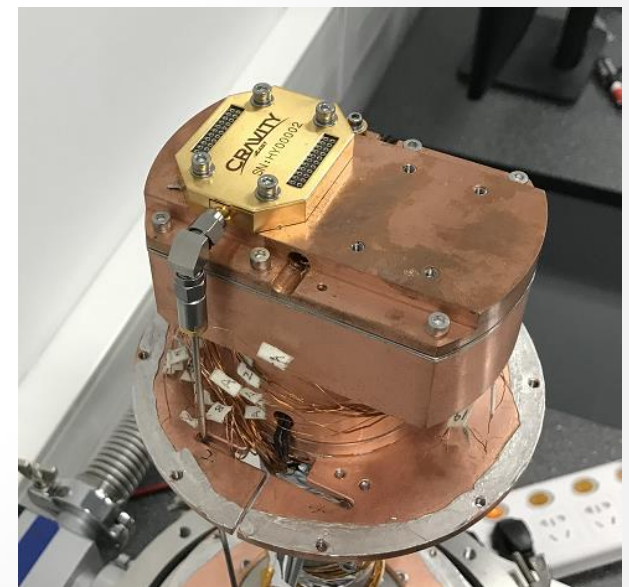
- The cryostat has a multipoint temperature control system, which is designed to work at temperatures around **4.2 K** or around **10 K** for two kinds of JJA chips.
- One kind of JJA is a NIST-fabricated 2 volt superconductor-normal metal-superconductor (SNS) Josephson array which works at temperature around 4.2 K.
- Another kind of JJA is NMIJ-fabricated 2 volt NbN-based programmable Josephson array which works at temperatures around 10 K.



Two-stage G-M cryocooler

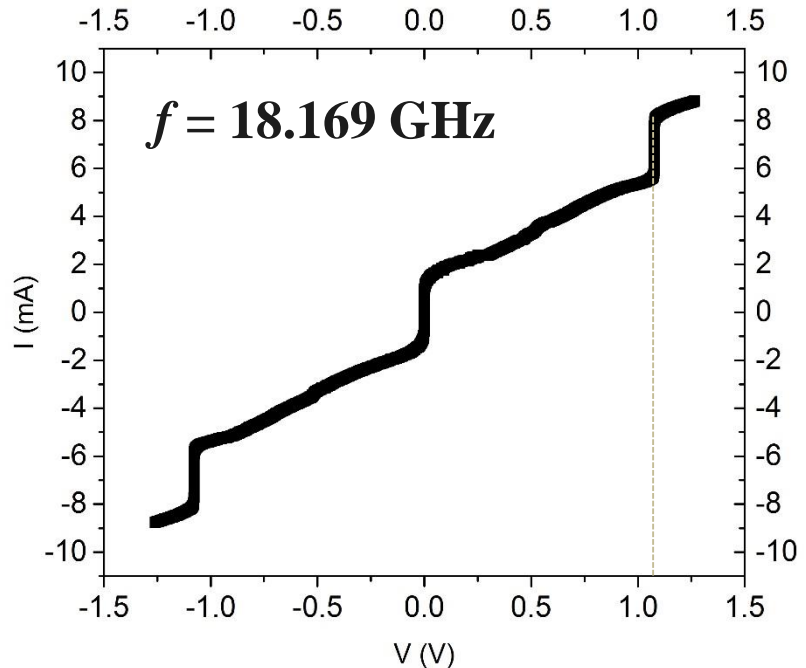
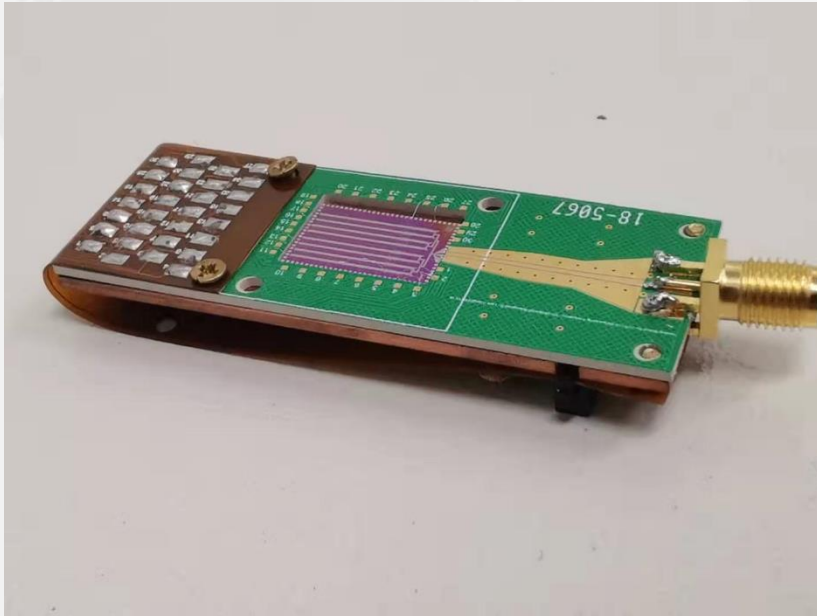


NIST-fabricated two volt Josephson chip mounted on the cold plate



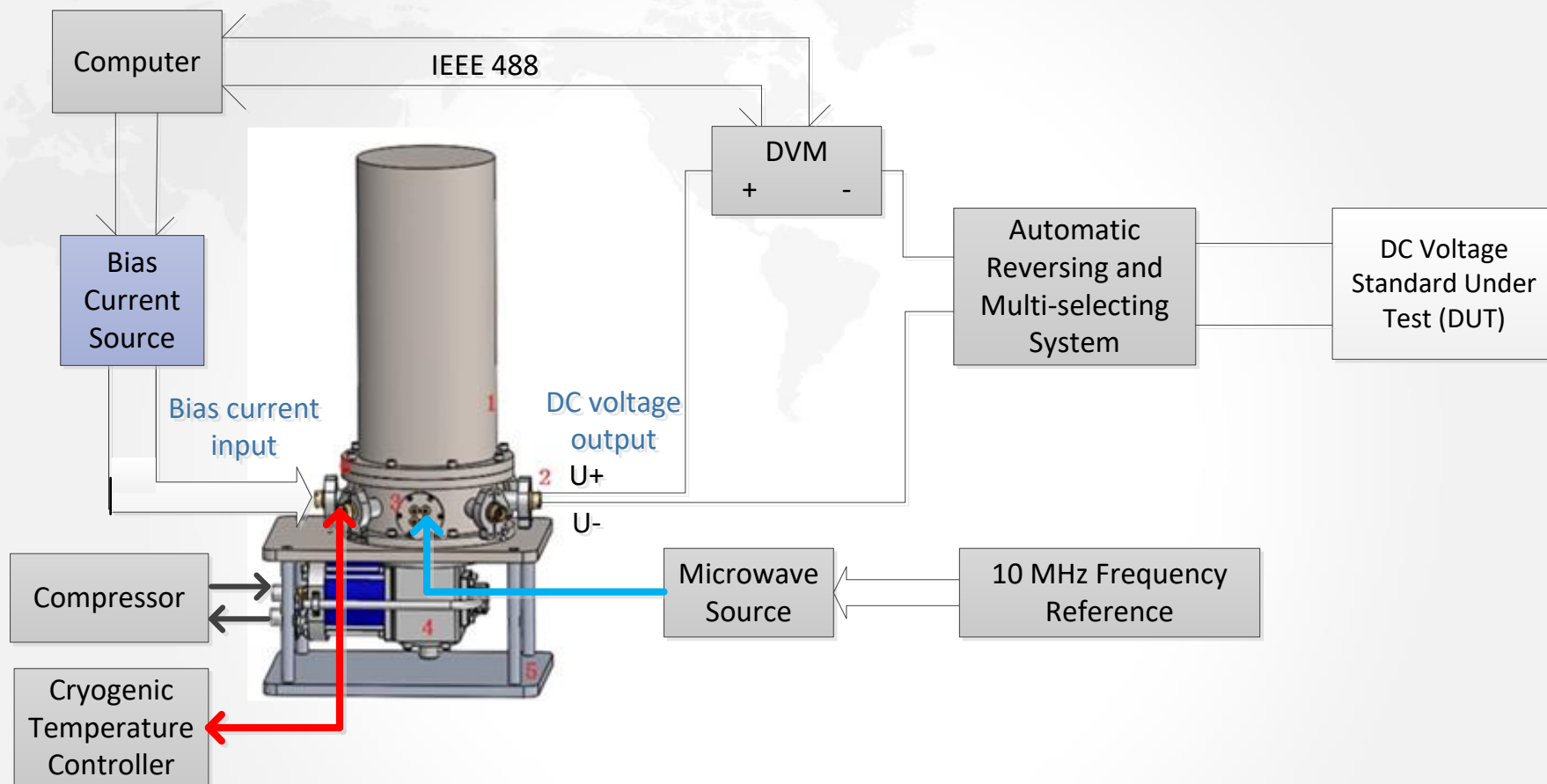
NMIJ-fabricated two volt Josephson chip mounted on the cold plate

NIM 1 V Josephson Junction Array Chip(2019)



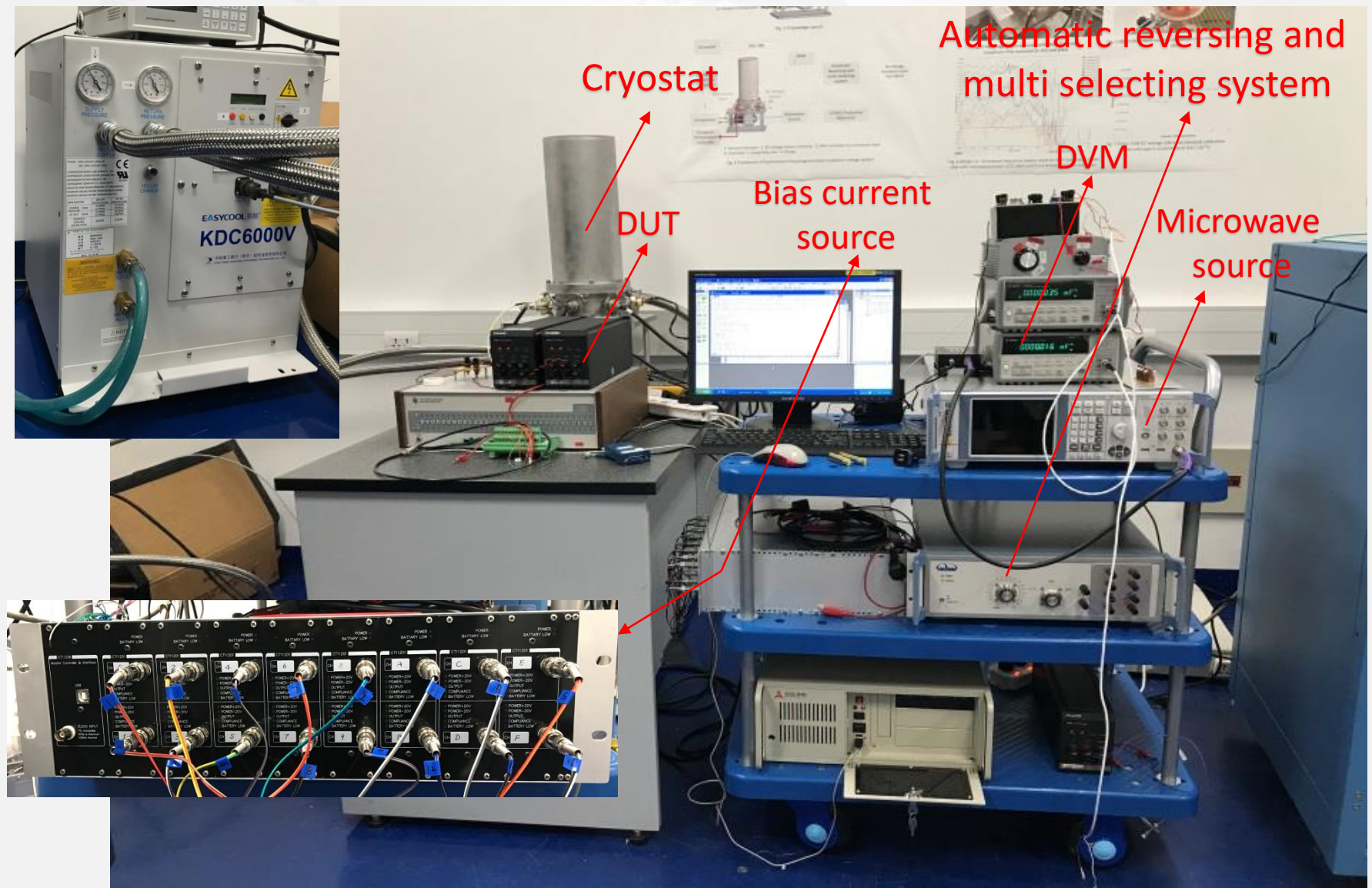
V = 1.077 Volt

- ~ 30000 JJ, 8 arrays, 2-junction stacked vertically.
- 3-stage, 2-way microwave power divider.
- Improved device packaging.
- Performance of NIM-fabricated 1 volt programmable JJA (4.2 K) as integrated with the cryopackage is still under testing.



1. Vacuum enclosure
2. DC voltage output connector
3. SMA connector for microwave input
4. Cryocooler
5. Supporting seat
6. Flange

Framework of liquid-helium free programmable Josephson voltage system

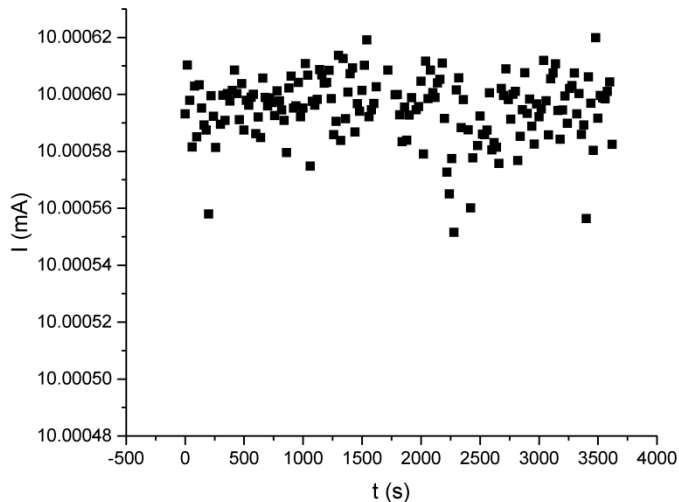




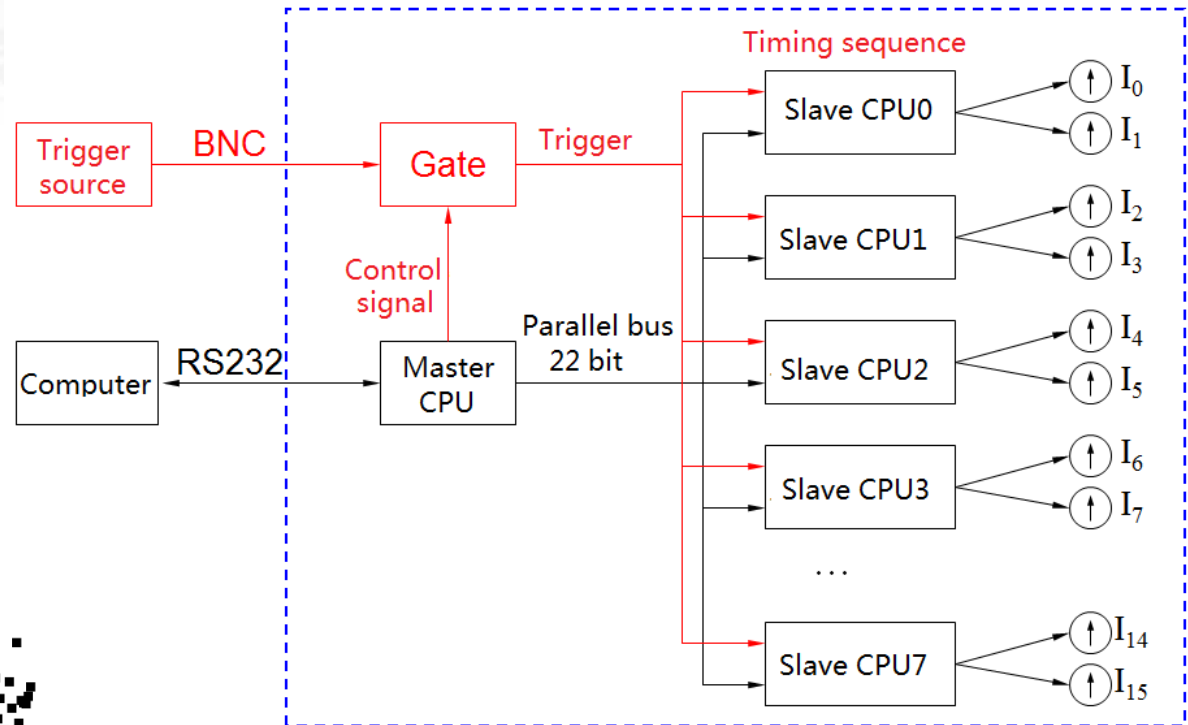
Bias current source



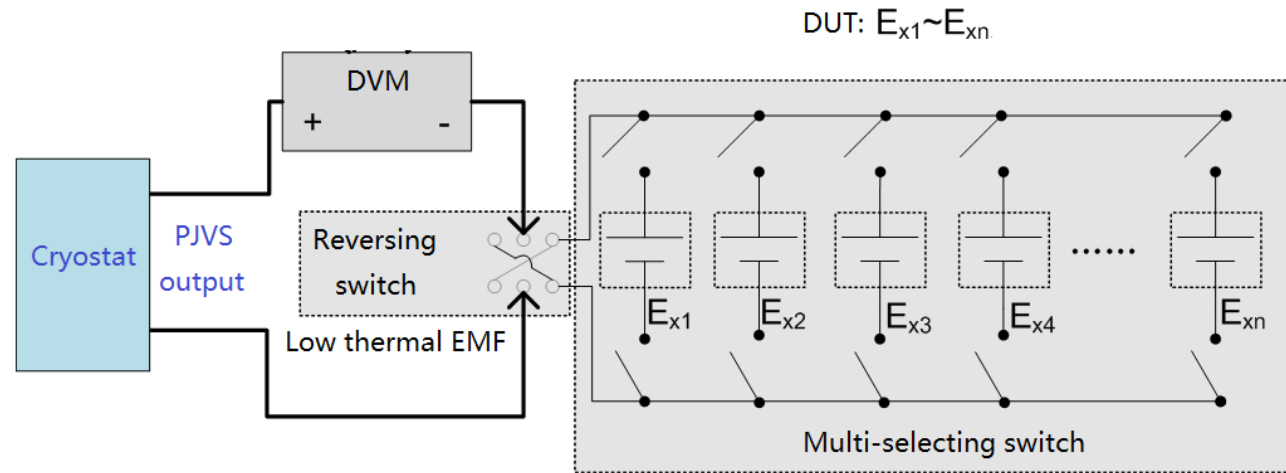
Battery package



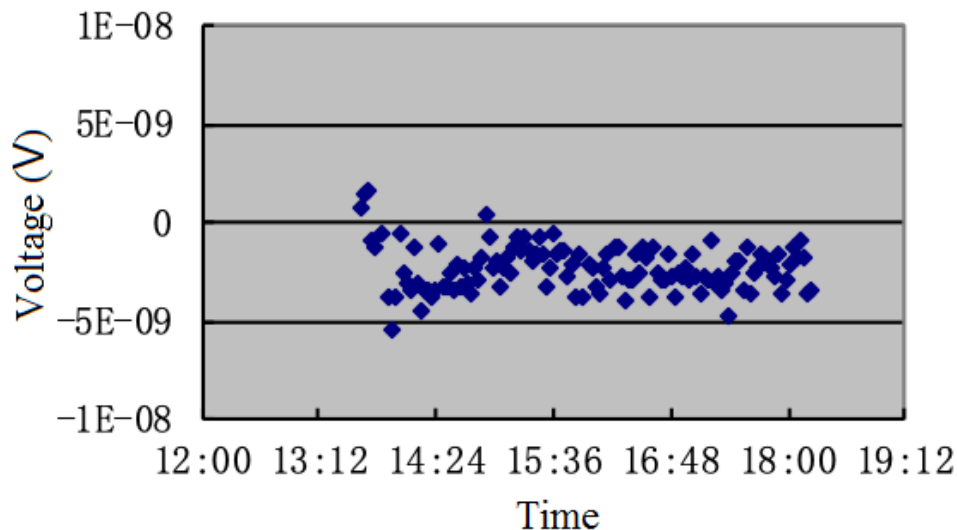
Output current stability in 1 hour (10 mA)



- ✓ Low noise 16-channel bias current source designed for cryocooled PJVS system.
- ✓ Optical couples are used for isolation.
- ✓ Battery-powered channels are independent of each other.
- ✓ Output current stability : **<0.1 μ A in 1 hour**



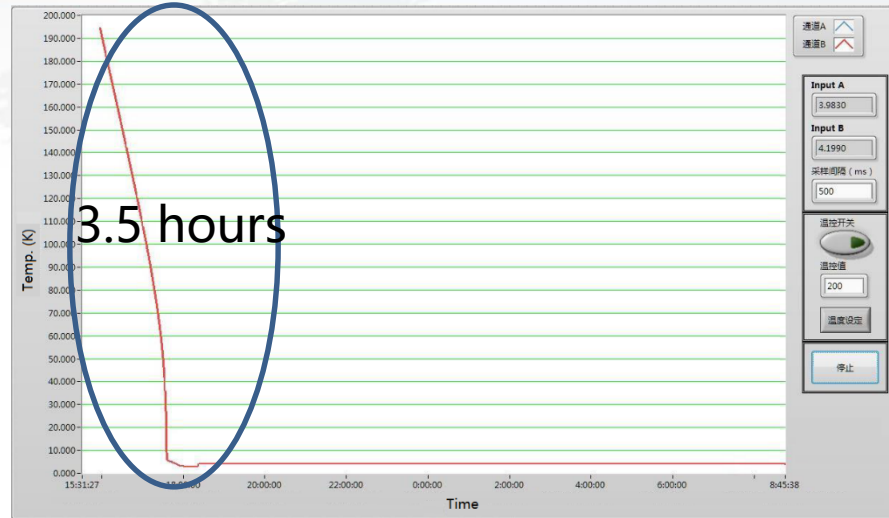
Ineluctable thermal EMFs effect



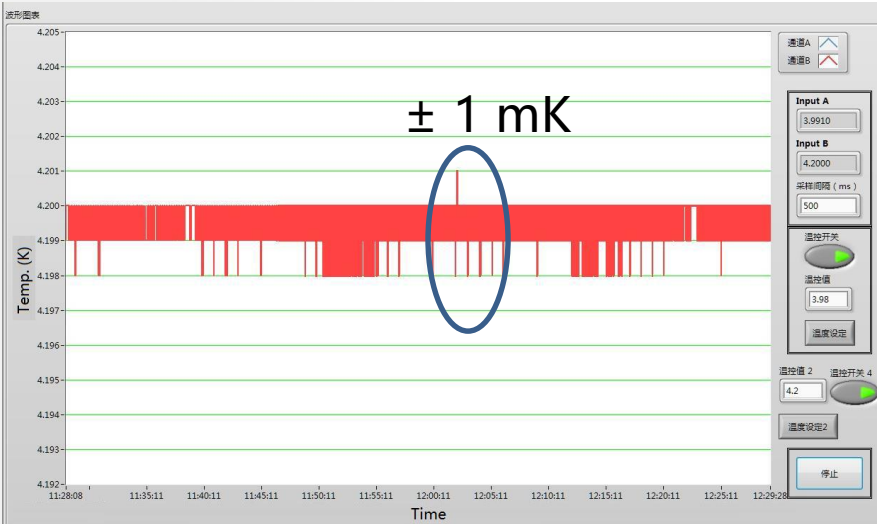
- ✓ One special designed mechanical rotary switch was used to minimize the thermal EMFs generated by the switches.
- ✓ Rotary switches were chosen deliberately to ensure the thermal EMFs of each silver contact.
- ✓ Battery-powered solution.
- ✓ Inevitable thermal EMFs contribution to the measurement uncertainty is less than 5 nV.



Lakeshore 325



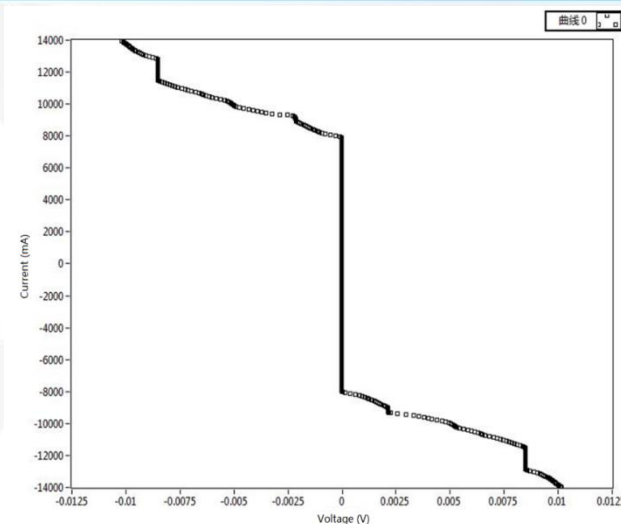
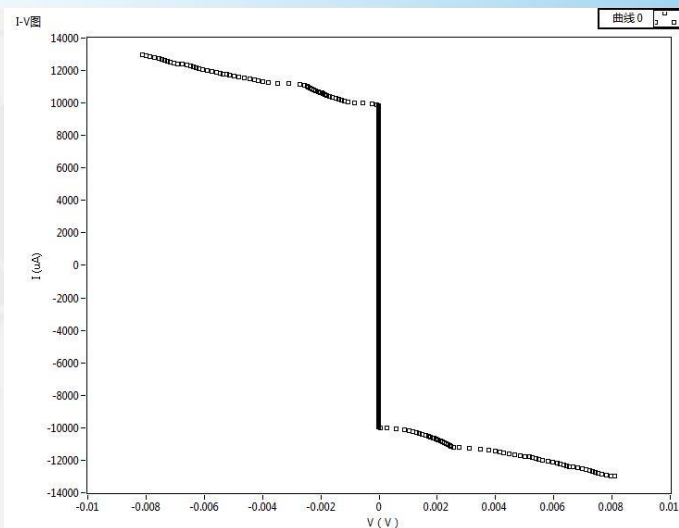
Cool down a JJA chip from room temperature to 4.2 K within 3.5 hours



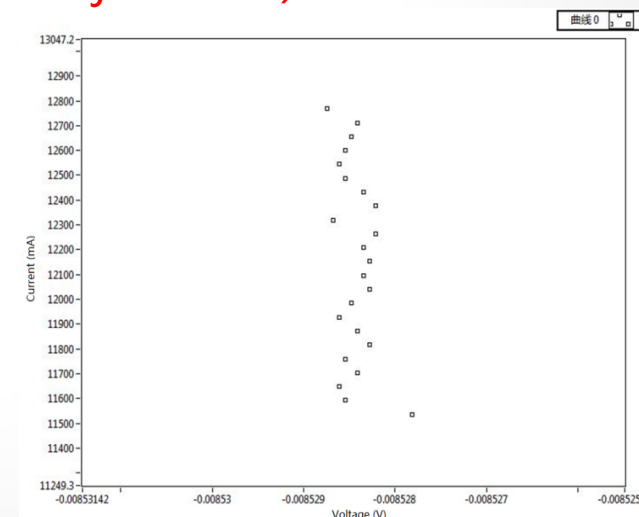
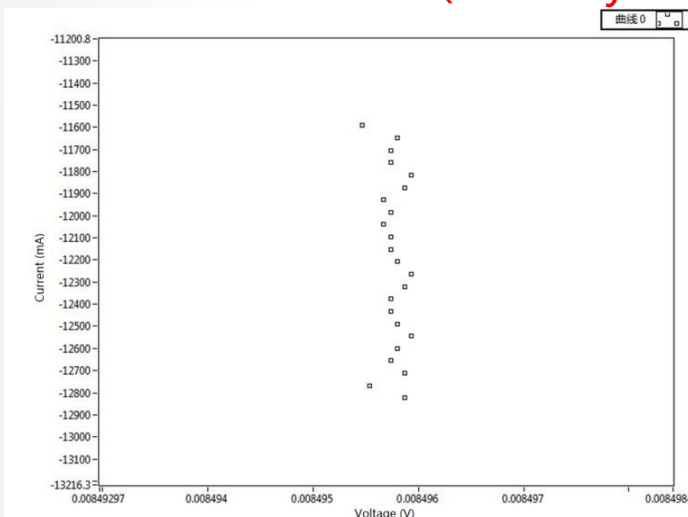
Short term temperature stability (1 hour)



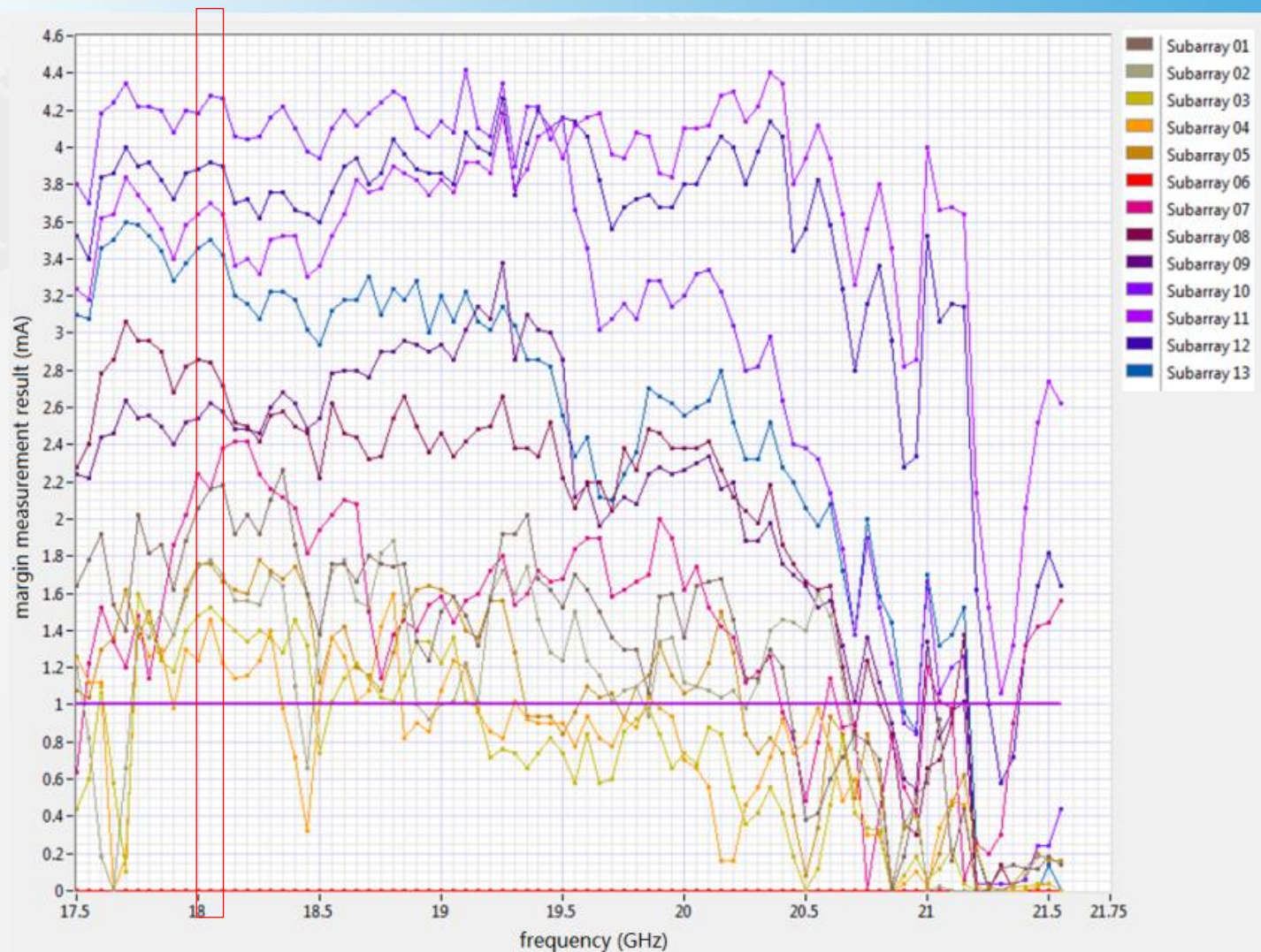
Long term temperature stability (7 hours)



Measured IC and IV curve for NMIJ fabricated 10 K JJA chip
(subarray 5 with 256 junctions)

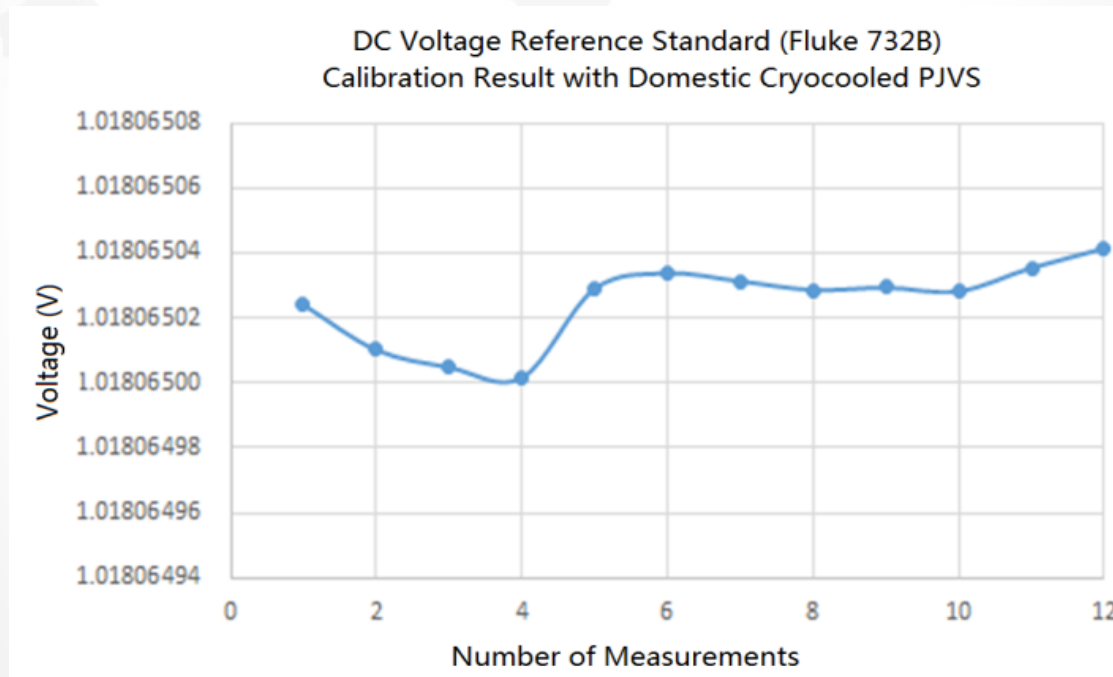


Positive margin and negative margin of the NMIJ-fabricated programmable Josephson chip (larger than 1.0 mA at 16.04 GHz, 23 dBm)



Width of quantum voltage step (margin) vs. microwave frequency sweep results for NIST-fabricated 2 Volt chip with microwave power of 22 dBm at 3.5 K on cold plate
Operating margins of all NIST fabricated subarrays greater than 1.5 mA at 18.05 GHz

- The cryocooled PJVS system is successfully used to calibrate 1.018 volt output of the Fluke 732B dc voltage reference standard.
- One measurement includes 40 readings with the measurement procedure in accordance with "+, -, -, +".
- The type A uncertainty of 12 measurements is $3.6 \times 10^{-9} \text{ V}$ in 1 hour.



DC voltage reference standard (Fluke 732B, 1.018 V) calibration result

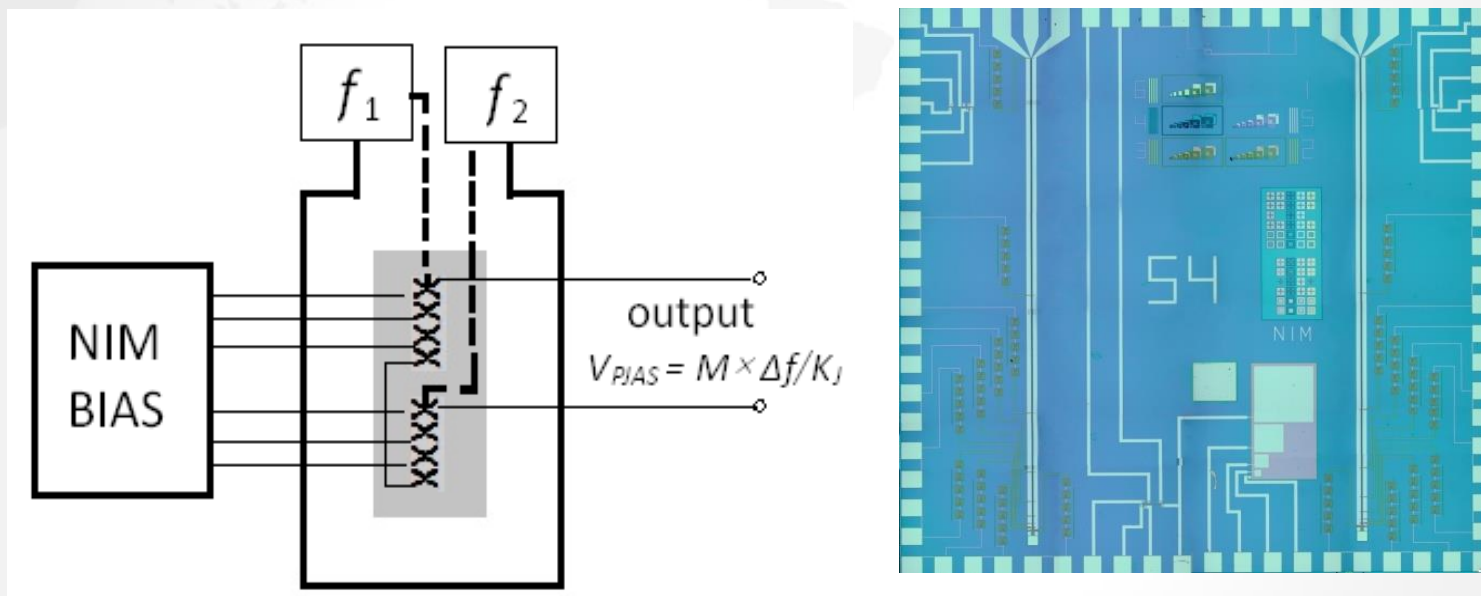
- A domestic liquid helium free dc PJVS operating on a cryocooler at 4K or 10 K is introduced.
- In this work, the performance of a NIST-fabricated two volt Josephson junction chip and a NMIJ-fabricated two volt chip operating in a cryopackage around the Gifford-McMahon (GM) cryocooler is presented.
- Experimental results have shown that both of the chips operate successfully in the domestic design cryopackage.
- The dc voltage reference standard calibration result with the type A uncertainty of 3.6×10^{-9} V shows a high accuracy of this cryocooled PJVS system.
- The system still needs some improvements
 - Heating problems while upgrading the output voltage level to 10 V
 - Further reducing the noise coming from the ground loop
 - ...

A faint, light gray world map is visible in the background of the slide, centered behind the main text.

**Thank you for your
attention!**

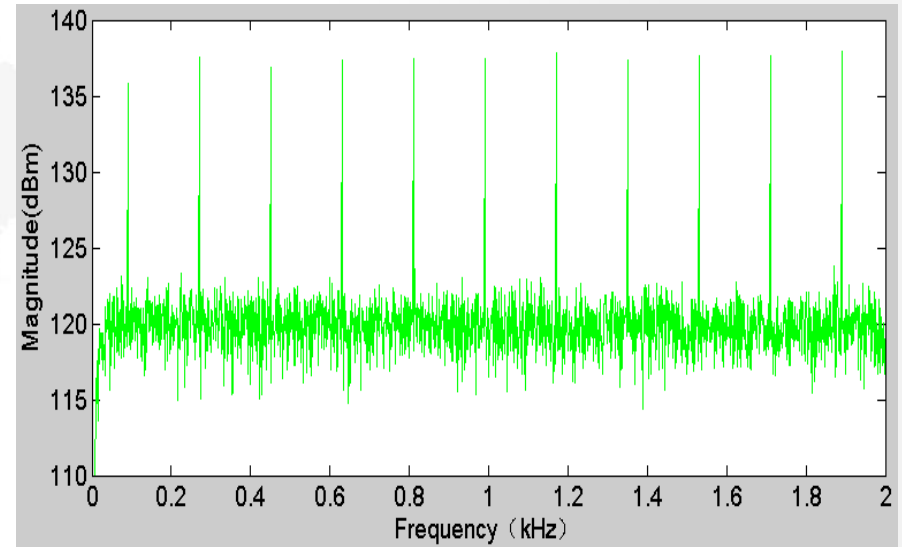
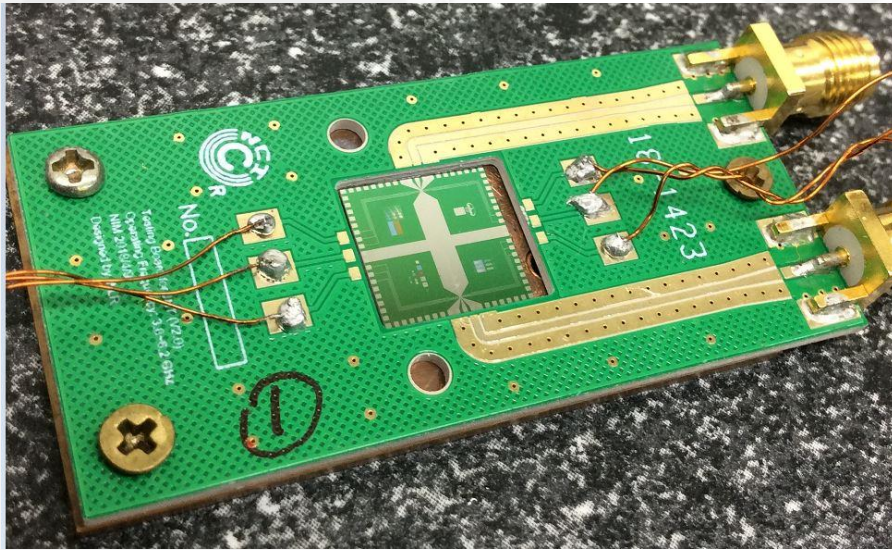
Chip for differential microvolt quantum voltage system

The device for double-channel differential microvolt quantum voltage system has been developed.



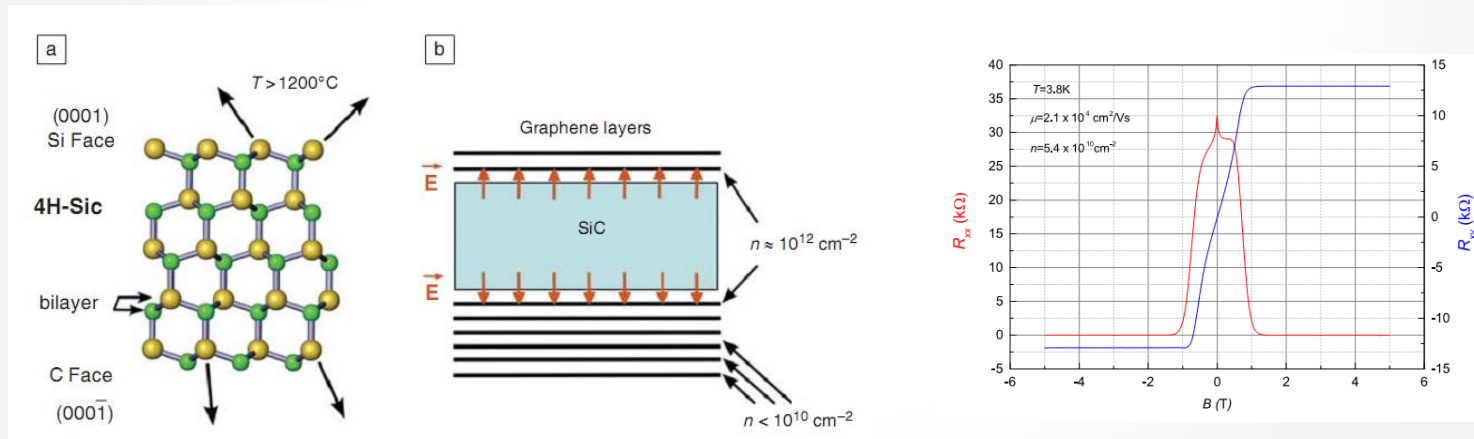
- Two JJ arrays are used and driven by MW with different frequency to generate voltage of several μV with high precision.
- This method expand the lower output of Josephson voltage standards from $150 \mu\text{V}$ to around $1 \mu\text{V}$ level. The system is also used to calibrate the nanovoltmeter.

Chip for quantized voltage noise source

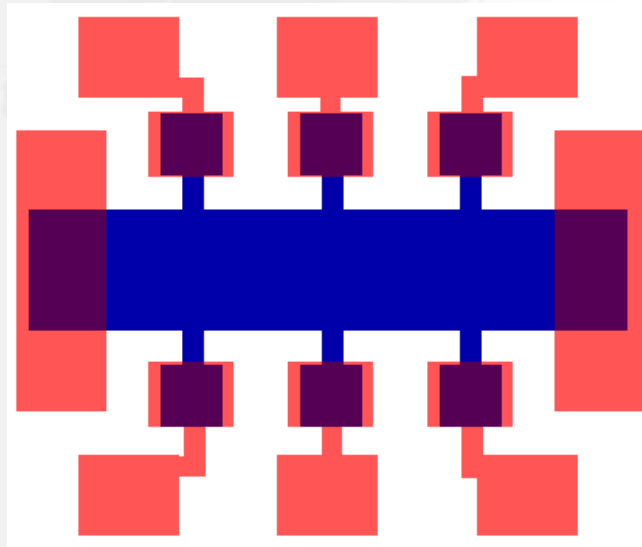


- We made the device for the quantized voltage noise source in the noise thermometry system. The chip which consists of 2 channels can successfully generate accurate quantum pseudo-noise signals.

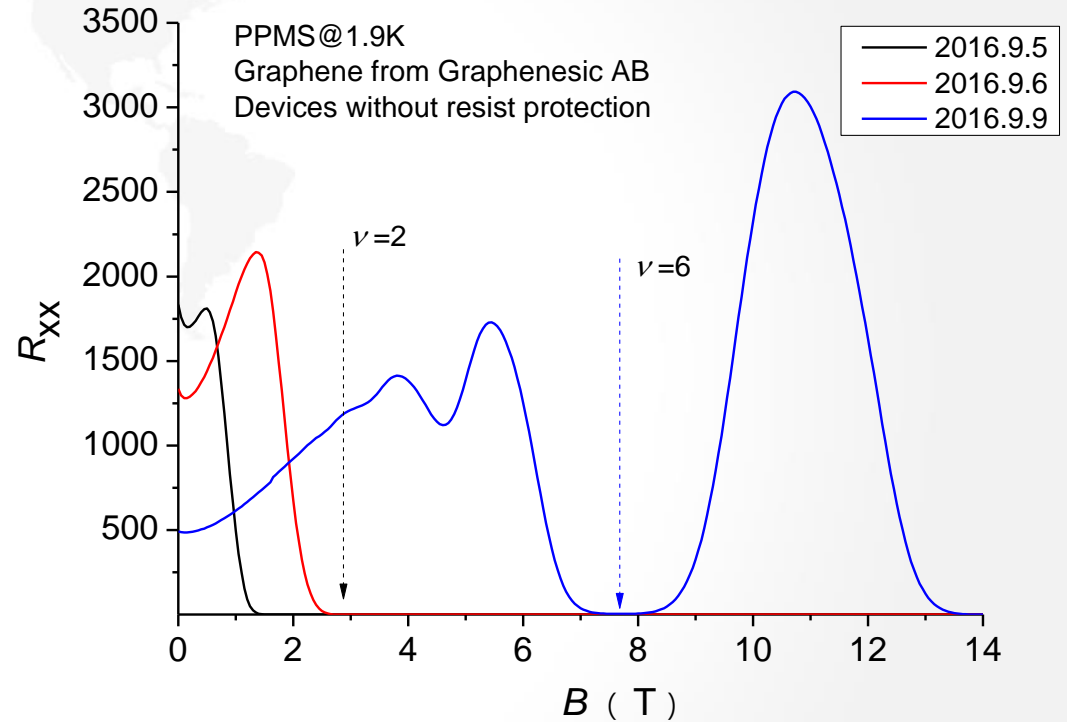
- ME graphene: small scale, large R_c , low I_c ...
- CVD graphene: defects, impurities, doping, gate, grain, wrinkles...
- Epitaxial SiC graphene: carrier concentration and mobility controlled, homogeneous layer fantastic candidate for resistance standard
- **Our aim: $B < 6$ T, $T < 4$ K (from 2016)**



NIM QHR on SiC graphene



300 μm \times 1500 μm



Elementary measurements were performed on SiC-graphene QHR using PPMS. The carrier concentration increased in vacuum with time because the adsorbing doping mediums on the surface desorbed. So controlled doping is critical and we are now researching on the method.