1 Volt DC Programmable Josephson Voltage Standard

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***Abstract* — NIST has developed a programmable Josephson voltage standard (JVS) that produces intrinsically stable voltages that are programmable from –1.1 V to +1.1 V. The rapid settling time (1 μs), large operating current margins (2 to 4 mA), and inherent step stability of this new system make it superior to a conventional JVS for many dc measurements. This improved performance is made possible by a new integrated-circuit technology using intrinsically shunted superconductor-normal-superconductor (SNS) Josephson junctions. These junctions operate at lower excitation frequencies (10 to 20 GHz) than a conventional JVS and have 100 times greater noise immunity. The Josephson chip consists of a binary array sequence of 32 768 SNS Josephson junctions. The chip has been integrated into a completely automated system that is finding application in mechanical / electrical watt-balance experiments, evaluation of thermal voltage converters, electron-counting capacitance standards, and metrology triangle experiments.**

I. Introduction

This paper describes a new programmable Josephson voltage standard (JVS) system that has been fully automated for DC metrology applications. In this new JVS, the output voltage $V = Nf / K_{J\text{-}90}$ is defined by digitally programming the step number N. Here f is the applied microwave frequency, and $K_{J\text{-}90} = 483\,597.9$ GHz/V is the Josephson constant. The system uses a series array of nonhysteretic junctions, divided into a binary sequence as shown in Fig. 1. The microwave excitation for each junction is set to equalize the amplitude of the $n = 0$ and $n = 1$ steps as shown in the inset. Each segment of the array can be set to the $n = -1$, 0, or +1 steps by applying bias current ($-I_s$, 0, $+I_s$) at the appropriate nodes. The combined step number N for the whole array can thus be set to integer values between $-M$ and $+M$, where M is the total number of junctions in the array [1, 2, 3].

The rapid settling time, inherent step stability, and large operating current margins of the JVS in Fig. 1 make it superior to a conventional JVS for many dc measurements. (We define a dc measurement to be one in which the transient associated with changing N can be excluded from the measurement.) This improved performance is made possible by a new integrated-circuit technology using intrinsically shunted SNS (superconductor-normal-superconductor) Josephson junctions. These junctions operate at lower excitation frequencies (10 to 20 GHz) than a conventional JVS and have 100 times larger step amplitudes (2 to 4 mA) [4].

The new JVS chip contains 32 768 Josephson junctions that are distributed such that the device functions as a 9-bit (including sign) digital-to-analog converter (DAC) [4]. The microwave drive is split 8 ways and delivered to 8 array segments of 4096 junctions each. The first segment is further divided into arrays of 128, 128, 256, 512, 1024, and 2048 junctions. Limiting the largest segment to 4096 junctions ensures adequate microwave power uniformity to the junctions, and allows the bias currents to compensate for critical current variations between individual 4096 junction segments. Chips with one or more defective segments can be operated at reduced voltages. The microwave drive frequency is near 16 GHz, so the voltage generated by each junction is $V = f / K_{J\text{-}90} \approx 33\ \mu V$. The smallest cell in the device consists of 128 junctions, which makes the least-significant-bit (LSB) resolution about 4 mV. Better output resolution is obtained by adjusting the frequency f to cover the voltage range between LSB's. This allows the JVS to provide gap-free coverage of the voltage range from 50 mV to 1.1 V (and from -50 mV to -1.1 V), where the voltage resolution is limited only by the resolution of the frequency source.

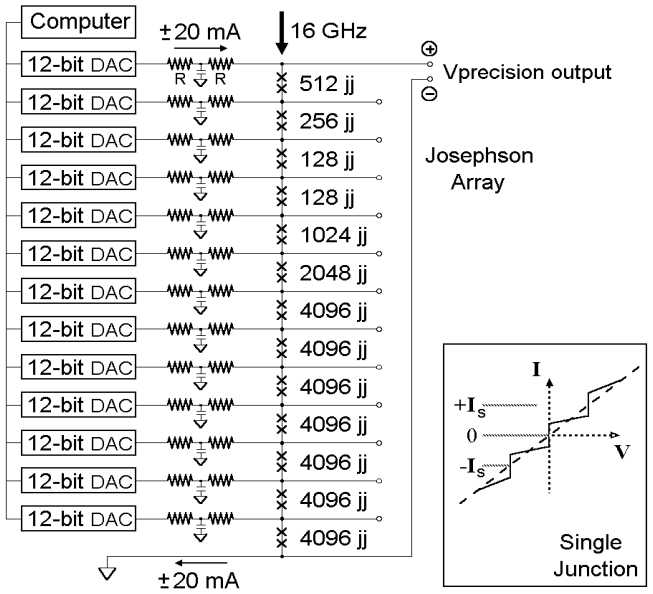

Fig. 1. Bias schematic of the 1 Volt programmable JVS.

II. Bias Circuit Design

As shown in Fig. 1, each node of the Josephson array is connected to a 12-bit DAC voltage source. These voltages are converted to currents by the two series resistors in each RCR filter (R = 100 Ω, C = 0.02 μF). The bias current to a typical array segment is about 15 to 20 mA. To set the Josephson array to any of its 511 quantized output levels, the computer calculates the voltage for each DAC output based

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on the bias current required by each array segment. After the 13 DAC input buffers have been loaded by the computer, the DAC outputs are simultaneously updated with a common trigger signal. The Josephson chip settles to the new voltage within a few microseconds.

The computer controls the bias electronics through an ordinary PC parallel port. Programming the array to a new output level takes about 500 µs. To ensure that noise from the computer and the environment is not coupled into the Josephson array biases, each signal wire from the parallel port is passed through a 1 MHz low pass filter. Additionally, the analog bias circuit is powered from rechargeable batteries and optically isolated from the digital logic. This not only reduces the potential for ground loops and unwanted RFI (radio frequency interference) coupling, but it also allows the Josephson array to float with respect to ground, allowing greater flexibility when the JVS is connected to other measurement systems.

III. Cryoprobe Design

A critical component of the new JVS is the cryoprobe that interfaces the Josephson chip to the laboratory environment. The precision output voltage from the Josephson array must be brought from liquid helium temperature to room temperature with a thermal offset voltage less than a few parts in 10^8, and a drift rate in that offset of a few parts in 10^9 per hour or less. To accomplish this, the head of the cryoprobe has two independent chambers that are thermally isolated from each other by a Delrin spacer, as shown in Fig. 2. This allows the thermally isolated chamber to equilibrate to room temperature, even though the main chamber is colder because it is in contact with probe components that extend into the Dewar. The main chamber contains connectors for the dc-bias wires and the 16 GHz microwave input coax.

The thermally isolated chamber minimizes thermal voltages in the precision output by bringing the wires from the Josephson chip and the wires to the outside world to the same temperature. The terminal blocks are OFHC (oxygen-free high-conductivity) copper and are electrically insulated from the aluminum body of the isolated chamber by a Mylar spacer approximately 50 µm thick. The large thermal mass of the isolated chamber makes it respond slowly to temperature changes in the room.

Another important feature of this cryoprobe is its small thermal load (only 2.5 liters of liquid helium per day for the cryoprobe and dewar) which allows the chip to remain cold in a 100 liter storage Dewar for over a month. To achieve this, the cold helium gas leaving the Dewar is forced to flow up the inside of the cryoprobe tube in contact with the wires and coax. The escaping gas cools these components and reduces the heat that they conduct into the Dewar. To ensure low thermal conduction, the dc-bias wires are only 0.15 mm in diameter, and the semirigid coax has a stainless steel outer conductor. The top of the cryoprobe tube is sealed where it enters the main chamber, so the helium gas escapes through a check-valve on the side of the probe.

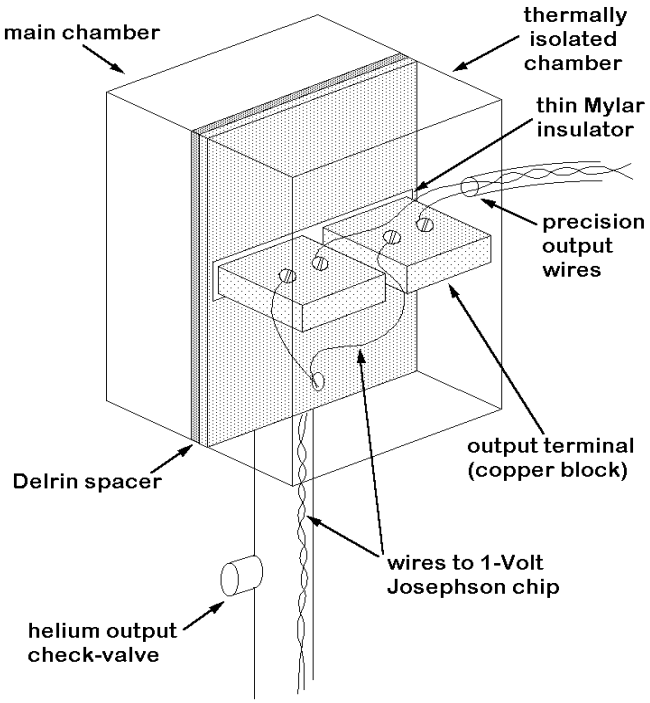

Fig. 2. Diagram of the JVS cyroprobe head with thermally isolated chamber for precision output voltage connections.

IV. System Overview

Figure 3 is a block diagram of the 1 V programmable JVS. The system computer controls the microwave frequency and power through GPIB (general purpose

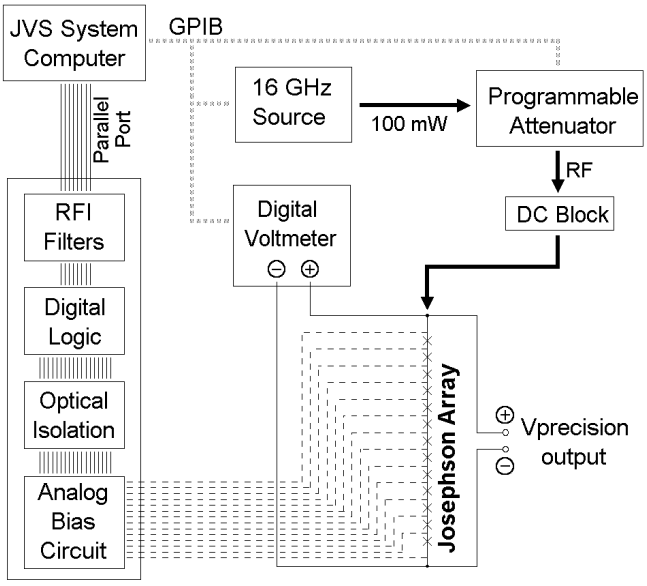

Fig. 3. Block diagram of the 1 Volt programmable JVS.

interface bus) connections to the 16 GHz source and the programmable attenuator. The output from the array is connected independently to both the precision output leads and the system digital voltmeter (DVM). This allows the system computer to continually monitor the array output with a resolution of a few microvolts (parts in 10^6 at 1 V).

Chip testing and diagnostic procedures are performed automatically. The individual I-V (current-voltage) curves of each array segment are measured to confirm functionality and to select the optimum bias points for the –1 and +1 steps. The chip operating margins for both dc-bias currents and microwave power are measured, and the output voltage step flatness is verified over the full step height with sub-micro-ohm resolution.

In order for the SNS programmable chips to be used in a voltage standard, it is important that the operating margins and step flatness be verified immediately before any measurements using the precision output. Unlike conventional SIS (superconductor-insulator-superconductor) voltage standards, it is possible for an SNS array to produce stable output voltages even when it is not on a constant voltage step. This can occur if the dc bias currents are incorrect, if the chip traps magnetic flux, or if the microwave frequency or power is changed without double-checking the bias operating range. The computer monitors the performance of the SNS array repeatedly between changes from one precision output level to another. In a few minutes it can verify that the SNS array output voltage is independent of bias current. A complete reoptimization of the chip's operating parameters at a given frequency and power takes about 10 to 15 minutes.

V. Test Results

The JVS system regularly performs diagnostic tests to ensure that the programmable standard is functioning at the required level of precision (parts in 10^9, including contributions from thermal offset voltage drift). The first test is to verify that the margins for the dc-bias currents are not overly sensitive to changes in the applied microwave power level. The results of such a test are shown in Fig. 4 for V_{out} = 1.018 V (largest 8 cells *on*), and V_{out} = 0 V (all cells *off*). As the figure illustrates, the rf-power level needs to be stabilized only to a few tenths of a dB to have a large (±1 mA) operating margin for the Josephson array output current. Furthermore, this particular chip can operate over the full ±2 dB power range of Fig. 4 with a smaller output current margin of ±500 µA.

The second test is to confirm that the thermal offset voltage has a low drift rate, even when the temperature in the room is changing. These measurements are made by setting the JVS output to 0 V, and connecting the system nanovoltmeter directly to the precision voltage outputs. Figure 5 shows the results of such a test over a 2 day period

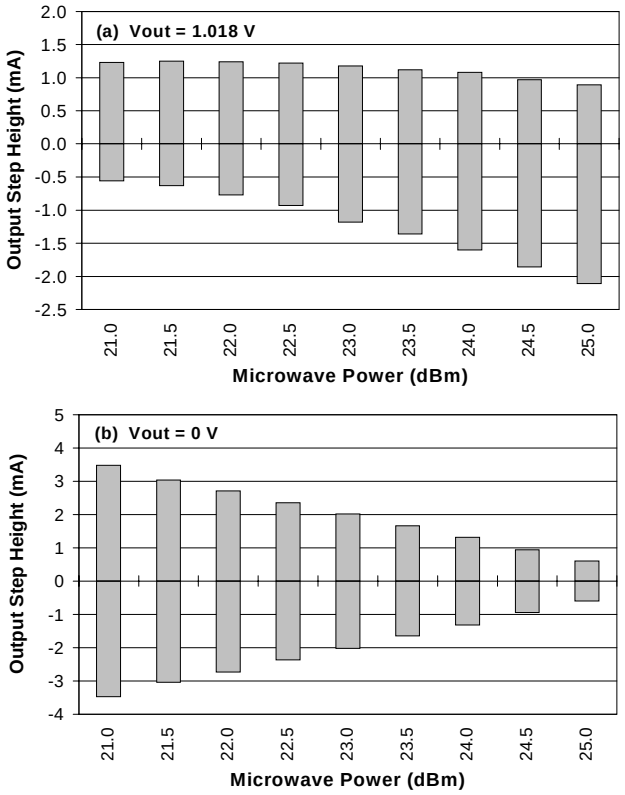

Fig. 4. Josephson array output step height vs. microwave power for (a) V_{out} = 1.018 V [all cells *on*], and (b) V_{out} = 0 V [all cells *off*].

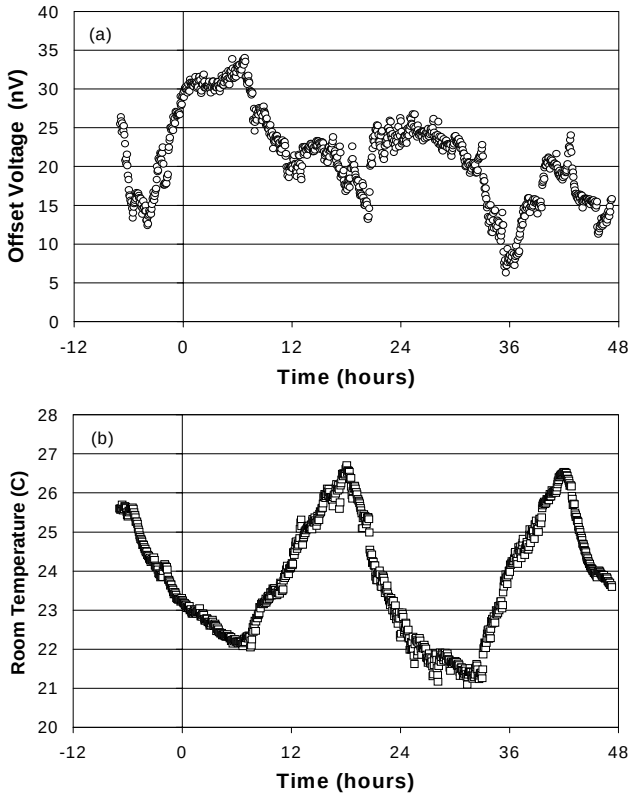

Fig. 5. (a) Thermal offset drift of JVS output voltage vs. time. (b) Temperature in the room vs. time for the same time period.

in a room without temperature control. As the graphs show, the offset voltage drift rate never exceeds a few nV per hour (parts in 10^9 per hour at 1 Volt) even in the presence of significant changes in room temperature. Even smaller offset voltage drifts are obtained by stabilizing the temperature in the room.

VI. Applications

The 1 V programmable JVS makes possible a number of dc measurements that take advantage of its rapid programmability, intrinsic output stability, and large operating margins (noise immunity). Some of these measurements have already been reported, including fast characterization of D/A and A/D converters, comparison against conventional SIS voltage standards, Zener reference calibrations using null voltages of 1 μV or less, etc. [3, 5]

The latest application of the 1 V JVS is the watt-balance experiment [6] which requires a stable, reversible voltage reference with high noise immunity. In the first mode of this experiment, a servo system controls the velocity of an induction coil moving in a magnetic field such that the voltage across the coil is equal to the 1 V reference from the programmable JVS. This configuration is illustrated in Fig. 6. By setting the JVS to either +1 V or –1 V, the coil moves up or down along the z-axis in order to precisely characterize the radial magnetic field.

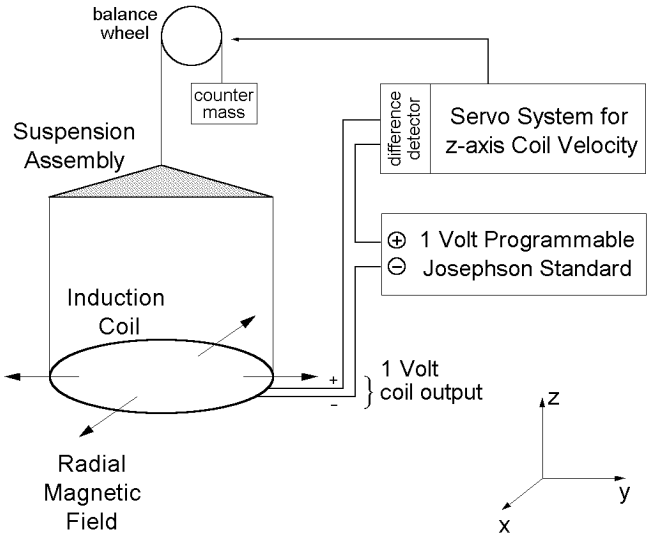

Fig. 6. Block diagram showing watt-balance wiring connections when using the 1 Volt programmable JVS as the voltage reference for the z-axis coil-velocity servo.

In the second mode of the experiment, the current in the induction coil is controlled in order to balance the gravitational force of a 1 kg mass, as shown in Fig. 7. This current is precisely measured by passing it through a resistance standard and comparing the resulting voltage to the programmable JVS with a null-meter. In both modes, the JVS provides a direct voltage reference for the experiment, thereby eliminating voltage transfers and the associated noise and uncertainty contributions. The large step height and flokes
it ideal for use in an experiment of this complexity. A system dedicated to the NIST watt balance experiment is in the final stages of construction. A similar system is being developed for a comparable experiment at the Swiss Federal Office of Metrology [7].

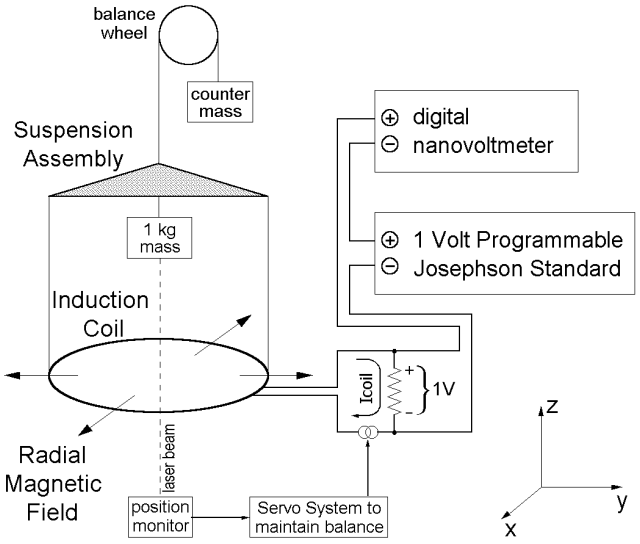

Fig. 7. Block diagram showing watt-balance wiring connections when using the 1 Volt programmable JVS to measure the current through the induction coil required to balance a 1 kg mass standard.

The programmable JVS has also been proposed for use as the voltage leg in a metrology triangle experiment [8]. In the metrology triangle, a precise reference frequency (f = 10 MHz) is translated into a voltage through a sequence of metrology experiments using several different quantum standards as shown in the simplified block diagram of Fig. 8. The objective is to test the consistency of the results obtained by the two different legs of the experiment. The path on the left in Fig. 8 uses a single electron pump at frequency f to generate a precisely known current, $I = fe \approx 1.6$ pA, where e is the fundamental electron charge. This current flows into a cryogenic current comparator where it is multiplied by a factor of 1000 and fed into a quantum-Hall resistance standard. The resulting voltage is given by $V = 10^3\, hf/e \approx 40$ μV, where h is Planck's constant. The path on the right of Fig. 8 uses a completely different technique to generate the same result. In this case, the 10 MHz reference is multiplied up to 20 GHz so that it can drive a single junction of our SNS programmable voltage standard. Comparing the results obtained by the two different methods checks for systematic errors in all of the standards involved. To reduce the final uncertainty, both legs of the experiment can be performed at higher voltages by using more junctions of the SNS programmable standard and adjusting the parameters of the other quantum standards.

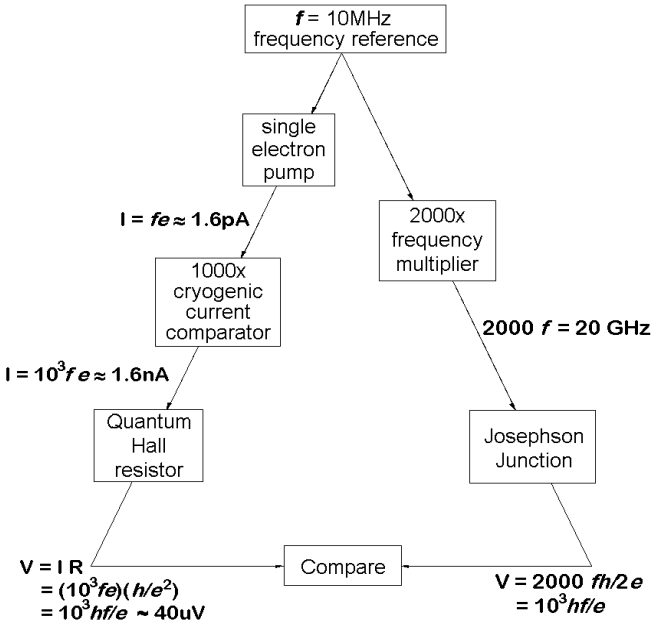

Fig. 8. Block diagram of the metrology triangle experiment.

Another experiment that combines the advantages of fast switching and stable output voltage of the programmable JVS is the precise characterization of capacitors used in electron counting experiments. When a nearly perfect step function generated by a Josephson array is applied a capacitor, the measured charging current can be Fourier-transformed to yield the frequency dependence of the capacitance.

The programmable JVS can also provide both the dc and ac inputs for the fast reversed dc (FRDC) method of measuring the thermoelectric transfer difference of thermal voltage converters (TVC). The first use in this application yielded a Type A uncertainty of 0.13×10^{-6} in the measurement of the thermoelectric transfer difference of a single-junction TVC and a multi-junction TVC [9].

VII. Conclusion

We have developed a fully automated 1 Volt programmable Josephson voltage standard system for DC metrology applications. It generates stable, reversible, precision voltages between +1.1 V and –1.1 V that are known with Josephson accuracy. The system is controlled by a standard PC-486 computer which can program the array in roughly 500 µs, after which the output voltage switches between levels in a few microseconds. The computer controls all operating parameters for the system including dc bias currents, rf drive frequency, and rf power level. The Josephson chip is optically isolated and battery powered to allow the greatest flexibility when connecting to experiments or other measurement systems. The system can also perform rigorous diagnostic tests of the chip to confirm that it does not have systematic errors such as rf-induced offsets or slopes in the output voltage steps.

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