A very low-noise FET input amplifier

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We describe the design, schematics, and performance of a very low-noise FET cascode input amplifier. This amplifier has noise performance of less than 1.2 nV/$\sqrt{\text{Hz}}$ and 0.25 fA/$\sqrt{\text{Hz}}$ over the 500 Hz to 500 kHz frequency range. With modest changes it could be extended to a wide variety of uses requiring low-noise gain in the 1 Hz to 30 MHz frequency range.

INTRODUCTION

A low-noise amplifier has been designed utilizing a Toshiba 2SK117 N channel J-FET[1] as the input device in a cascode[2] configuration. Noise measurements on this amplifier yield a low-frequency noise current of 0.25 fA/$\sqrt{\text{Hz}}$ and a voltage noise of less than 1.2 nV/$\sqrt{\text{Hz}}$ in the 500 Hz to 500 kHz region. Bloyet, Lepaisant, and Varoquaux[3] suggest a figure of merit of the product of the noise voltage and current as being appropriate for amplifiers of this type. This amplifier has a figure of merit of $\sim 3\times 10^{-25}$ W/Hz, which is almost two orders of magnitude smaller than other amplifiers reported elsewhere.[3]

This improvement is primarily a result of the extremely low-bias current and large transconductance of the 2SK117.

I. EQUIVALENT CIRCUIT FOR NOISE ANALYSIS

The schematic of the amplifier is shown in Fig. 1. The biasing scheme used for $Q\,2$, the common base portion of the cascode, is attractive for its simplicity and inherent low noise, but it does require that I_{dss} of $Q\,2$ be larger than I_{dss} of $Q\,1$ to work properly.

The gain of the cascode input stage is large; hence, the noise in this stage is dominant, and we can confine our analysis to the input stage and the associated biasing circuitry. Using the model of Fig. 2, the equivalent input noise, E_{ni}, can be written[4]

$$E_{ni}^2 = E_{nQ1}^2 + I_{nt}^2 Z_g^2 + E_{nRs}^2 + \left(\frac{1}{K_{Q1}}\right)^2 (E_{nQ2}^2 + I_{nQ2}^2 R_{s1}^2) + \left(\frac{1}{K_t}\right)^2 E_{nRd}^2, \quad (1)$$

where $K_t = g_{m1} R_d$ and

$$K_{Q1} \approx -(g_{m1}/g_{m2})(1 + g_{m2} r_{d1})$$

is the gain ratio of the common source component of the cascode. K_{Q1} has additional terms arising from parasitic capacitances to ground at the drain of Q_1 which are small at these low frequencies and are therefore neglected here. r_{d1} is the output resistance of $Q\,1$. Z_g is the impedance presented to the gate of $Q\,1$ formed by the parallel combination of C_g, the gate capacitance, and R_g, the gate bias resistor. I_{nt}^2 is the quadrature sum of the noise current from $Q\,1$ and the noise current from R_g.

II. NOISE MEASUREMENTS

The amplifier noise was measured by first measuring the transfer function of the amplifier (see Fig. 3). The input capacitance was measured using a known capacitance in series with the input of the amplifier and measuring the change in apparent amplifier gain as a function of capacitance. In order to measure the input current noise, the gate bias resistor R_g was increased to 7×10^{11} Ω so that the term $I_{nt}^2 Z_g^2$ would dominate in Eq. (1). A measurement of the noise from 1.5 to 10 Hz coupled with the known input capacitance

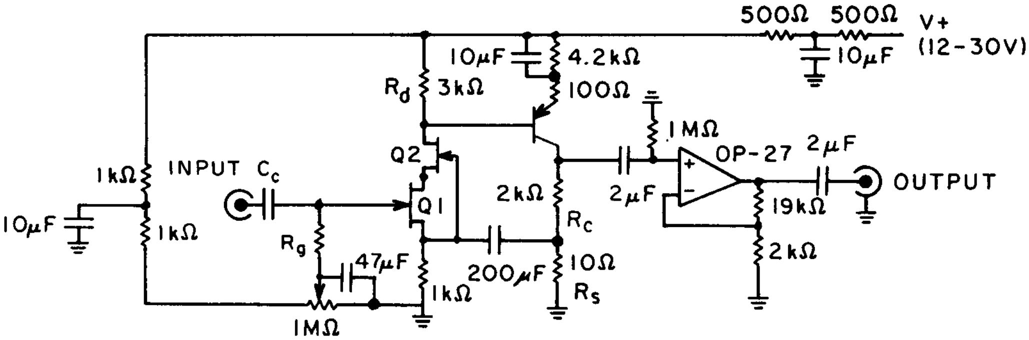

FIG. 1. Schematic diagram of the low-noise preamplifier.

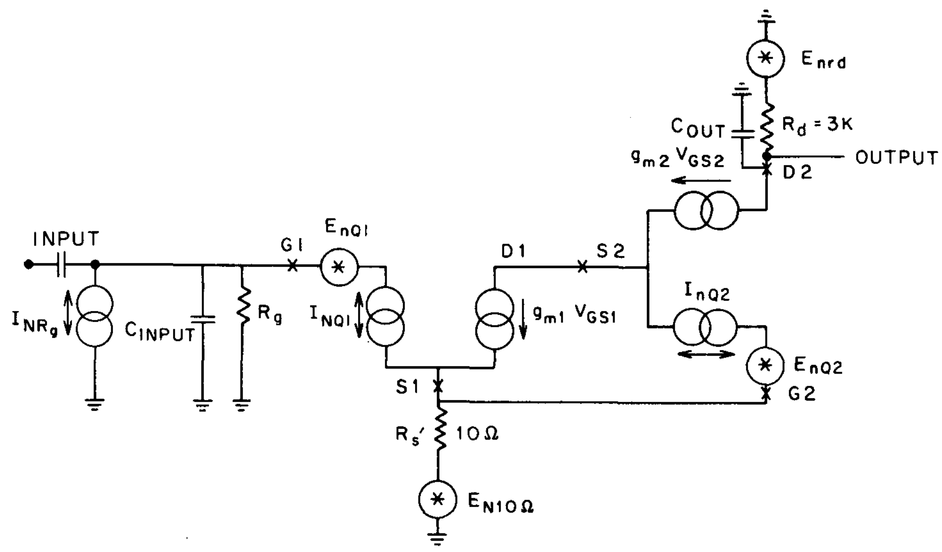

FIG. 2. The noise equivalent circuit of the cascode input stage.

C_g allows one to write

$$\frac{1}{E_{ni}(f)} \simeq \frac{1}{R_g I_{nt}} (1 + 2\pi C_g R_g f), \tag{2}$$

where $E_{ni}(f)$ is the equivalent noise at frequency f at the input of $Q\,1$. Using a linear regression analysis to find the slope m of the $1/E_{ni}$-vs-f line, we can then write

$$I_{nQ1} = \left[\left(\frac{2\pi C_g}{m}\right)^2 - \left(\frac{4KT}{R_g}\right)^2\right]^{1/2}. \tag{3}$$

The $1/f$ contribution of current noise in both the input FET and R_g was measured to be less than 10^{-16} A/$\sqrt{\text{Hz}}$ at 1.5 Hz.

E_{nQ1} the voltage noise associated with $Q\,1$, was measured by replacing the 7×10^{11}-Ω resistor used for R_g with a 10-Ω resistor. From the noise associated with $Q\,2$ and the rest of the circuit and the measured output noise, we can infer the noise associated with $Q\,1$.

III. RESULTS

Measurements using three different 2SK117 FETs for $Q\,1$ and a variety of different 2N4116 FETs for $Q\,2$ give the following results for the amplifier:

$$E_{ni} \simeq 1.1 \text{ nV}/\sqrt{\text{Hz}}, \quad I_{ni} \simeq 0.25 \text{ fA}/\sqrt{\text{Hz}}. \tag{4}$$

Figure 4 shows the measured voltage noise as a function of frequency for the amplifier. Independent measurements with 2N4116 FETs show that the noise voltage associated with them is approximately 3 nV/$\sqrt{\text{Hz}}$. Using this value and Eq. (1), we can infer a noise voltage for the 2SK117 of about 1 nV/$\sqrt{\text{Hz}}$. It is interesting to compare this to the theoretical result derived by van der Ziel[5]:

$$e_{nQ1} = \left(\frac{2}{3}\frac{4KT}{g_{m1}}\right)^{1/2}. \tag{5}$$

Using $g_{m1} = 16$ mmhos, the transconductance of the 2SK117 at 3 mA of drain current, and a drain-source voltage of 10 V (as taken from the data sheet), this gives $e_{nQ1} = 0.82$ nV/$\sqrt{\text{Hz}}$, which, given the rough knowledge of g_{m1} seems to be in reasonable agreement with the measured result. In the actual amplifier the drain-source voltage was approximately 2.5 V, which probably reduces g_m slightly from the above value.

If one measures the gate current of the input FET in a version of this amplifier in which $Q\,2$, the common gate por-

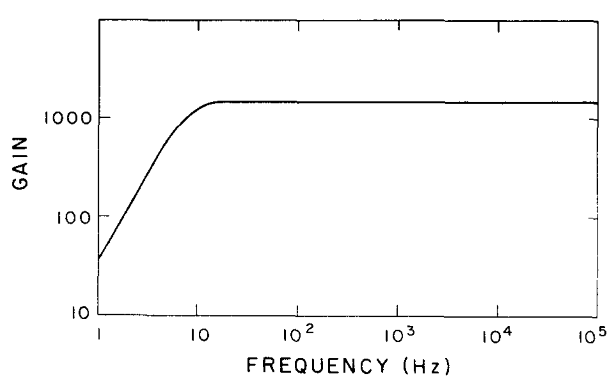

FIG. 3. Measured transfer function of the amplifiers.

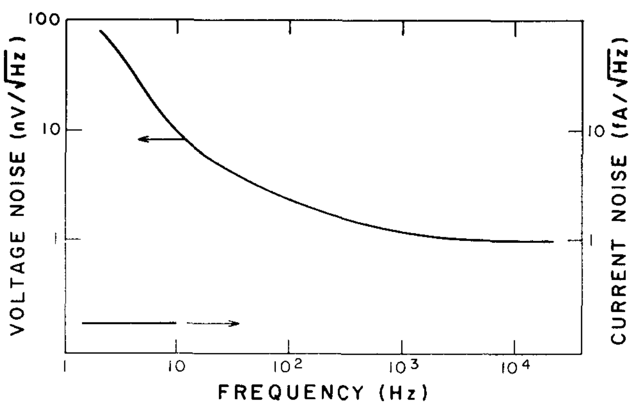

FIG. 4. Measured input voltage noise.

tion of the cascode, is shorted, making the input of the amplifier a common source stage, then an interesting effect occurs. The gate current, as measured by the voltage drop across R_g, decreases and finally changes sign, with increasing drain current. In our amplifier this was with about 4.5 mA of drain current and a drain-to-source voltage of 10 V. The gate-to-source voltage at this point was approximately -0.2 V so that forward bias of the gate-source diode is unlikely to be the cause of the zeroing of the bias current. A measurement of the noise current in this region yields a monotonically increasing value in the region of apparently zero gate bias current, indicating that two or more processes are at work. This effect is, however, potentially useful in an application in which the amplifier must draw a minimal bias current through the gate. A drawback to this circuit is, however, that the input capacitance is ~ 50 pF as opposed to ~ 11 pF for the cascode configuration. The cascode amplifier also exhibits very low input bias current, typically less than 0.3 pA for drain currents in the 3-mA range, but it does not exhibit an apparent vanishing of this bias current as does the common source configuration. It should be noted that the cascode amplifier performance was approximately constant with drain currents from 1 to 4.5 mA and that the 3-mA drain current used was simply convenient for our purposes. One further related point is that the 2SK117s that we used all had $I_{dss} > 5$ mA, the drain current clearly should be less than I_{dss}, and one should ensure that V_{ds} of $Q\,1$ is large enough ($\gtrsim 1.0$ V, depending on the operating parameters) to ensure that $Q\,1$ is thoroughly pinched off.

The bandwidth of the amplifier as shown in Fig. 1 is limited to about 500 kHz. This bandwidth limitation is, however, due to the limited bandwidth of the op-amp used for the output stage. If additional bandwidth is required, R_c and R_d should be reduced and a video amplifier used as the output stage. One further point to be made is that the coupling capacitors in the circuit (200 and 2 μF) can be decreased considerably at the expense of only a small increase in the low-frequency cutoff. It is suggested that this be done in any application not needing very low-frequency response. As a further practical point, the resistors in the signal path should be metal-film low-noise resistors, particularly R_g, R_d, R_c, R_s, and the 100-Ω emitter resistor in the second stage. Carbon resistors should generally be avoided.

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[1]The commercial equipment used has been identified for technical completeness. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology.

[2]R. Q. Twiss and Y. Beers, in *Vacuum Tube Amplifiers*, MIT Radiation LABS Series, edited by G. E. Valley Jr. and M. Wallman (Boston Technical Lithographers, Boston, 1963), Chap. 13.

[3]D. Bloyet, J. Lepaisant, and E. Varoquaux, Rev. Sci. Instrum. **56**, 1763 (1985).

[4]C. D. Motchenbacher and F. C. Fitchen, *Low Noise Electrical Design* (Wiley, New York, 1973), p. 231. The factor K_{Q1} neglects shunting of the input impedance of $Q\,2$ due to the output impedance of $Q\,1$ and stray capacitance from the $Q\,1$-drain–$Q\,2$-source connection to ground. These are of importance at higher frequencies, but are of negligible consideration here.

[5]A. van der Ziel, Proc. IEEE **50**, 1808 (1962).