NIST 10 V Programmable Josephson Voltage Standard System

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***Abstract*—The National Institute of Standards and Technology has developed and implemented a new programmable Josephson voltage standard (PJVS) that operates at 10 V. This next-generation system is optimized for both dc metrology and stepwise-approximated ac voltage measurements for frequencies up to a few hundreds of hertz. The nonhysteretic Josephson junctions produce intrinsically stable voltages and are designed to operate in the 18–20 GHz frequency range. The most recent 10 V PJVS circuits have total output current ranges greater than 1 mA.**

***Index Terms*—Digital–analog conversion, Josephson arrays, power measurement, quantization, signal synthesis, standards, superconducting device packaging, superconducting devices, voltage measurement.**

I. Introduction

SINCE the demonstration of uniform series arrays of intrinsically shunted Josephson junctions starting in the mid-1990s [1], [2], continued research and development has led to programmable Josephson voltage standards (PJVSs) with various performance characteristics and features. In recent years, the output voltage of PJVS circuits has increased beyond the original 1 V maximum voltage and reached the 10 V benchmark [3]–[6], which was set over 20 years ago by conventional dc Josephson voltage standard (JVS) systems. Junction uniformity and yield have recently been improved through the use of junctions with Nb–Si barriers [7], [8].

As a result of these improvements, PJVS technology is now poised to replace conventional JVS systems in the coming years for those who wish to utilize its unique advantages, which include the following: 1) comprehensive automation and the ability to fully characterize all operating margins of the device with minimal operator participation; 2) inherent voltage-step stability and large current margins (greater than 1 mA), which eliminate the need for output filters, thus enabling applications not previously possible with conventional JVS; and 3) short settling time (200 ns), which allows the generation of both dc and stepwise-approximated ac voltages, which are metrologically useful up to a few hundreds of hertz.

Because PJVS systems directly "program" the output voltage, they require completely different dc and microwave bias electronics and wiring and therefore are not a "drop-in replacement" for existing conventional JVS systems. The realization of 10 V PJVS devices at the National Institute of Standards and Technology (NIST) has given us the opportunity to completely redesign each component of the PJVS system, including audio-frequency bias electronics, control software, cryopackaging, cryoprobe, microwave generator, etc. These system design improvements for the new PJVS circuits are essential for extending the capabilities and features beyond the conventional application of dc metrology and into ac metrology applications through the use of the intrinsically stable and rapidly programmable voltages.

II. 10 V PJVS System Design

The NIST 10 V PJVS system includes newly designed bias electronics, along with comprehensive control software. Our dc and ac metrology objectives for the next decade require bias electronics that is capable of meeting the following criteria: 1) precise bias-current set-point accuracy in both dc and stepwise ac modes of operation; 2) consistent and reliable channel-to-channel gain and dc-offset matching, so that calibration of these quantities is not necessary; 3) fully automated PJVS operating margin setup and verification, so that the system is ready for use with Josephson accuracy within a measurement time of 15 min for a given microwave frequency and power; and 4) modular design to facilitate easy hardware updates and/or repairs to bias module subcomponents such as digital-to-analog converters (DACs), output amplifiers, digital circuitry, and power supplies (battery, isolated wall power, or both). Additionally, we have implemented a flexible architecture in both hardware and software in order to support an expandable number of drive channels (presently demonstrated up to 24, but additional channels are possible if desired). While developing ac measurement techniques [9], [10], we found that the PJVS system performance was severely limited because the previously used bias electronics lacked the aforementioned features.

Our new bias system presently supports PJVS output voltages from $+12$ to -12 V. Future circuit designs could achieve ± 15 V operation with a small change in output amplifier circuitry. We have verified that the bias electronics meets our

Manuscript received June 11, 2010; revised November 5, 2010; accepted November 15, 2010. Date of publication January 13, 2011; date of current version June 8, 2011. This paper was presented at the Conference on Precision Electromagnetic Measurements, Daejeon, Korea, June 2010. The Associate Editor coordinating the review process for this paper was Dr. George Jones.

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Digital Object Identifier 10.1109/TIM.2010.2101191

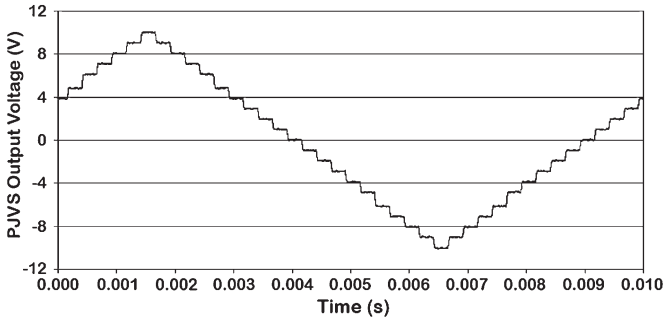

Fig. 1. Digital oscilloscope measurement of a 10 V (zero-to-peak) 100 Hz triangle wave generated by the 10 V PJVS system. This 10 V circuit design consists of 32 equally sized subarrays, giving a "digital" resolution around 400 mV. We are also developing a new "high-resolution" 10 V PJVS chip, and these more versatile devices will have a least significant bit of approximately 200 μV.

TABLE I
BIAS ELECTRONICS DESIGN SPECIFICATIONS

Design Parameter	Requirement	Resulting Set-point Deviation (each individual channel)
DAC resolution	16 bits	0.004 mA/LSB
Output Resistor Tolerance	± 0.05 %	± 0.01 mA
Cryoprobe Line Resistance	± 0.05 Ω	± 0.01 mA
Output Stage Gain Uniformity (channel to channel)	± 0.02 %	± 0.02 mA
Output Stage dc offset Uniformity (channel to channel)	± 0.5 mV *(max)*	± 0.005 mA

(Required tolerances on each channel for the primary design parameters. When the performance of every channel falls within the "requirement" range in the second column, then the bias electronics will never need calibration to guarantee a set-point accuracy within ± 0.05 milliamperes (i.e., the sum of the entries in the third column, which is the absolute worst case). The bias electronics must meet these requirements at any operating temperature that it experiences.)

specifications using a 10 V PJVS device in both dc and stepwise ac modes (Fig. 1) of operation. As we described previously [5], [6], we chose a target for a bias-current set-point accuracy of $\pm$0.05 mA (absolute maximum) on each channel. PJVS circuits are current-biased devices, and the calculations that are necessary to program the total output to different quantized voltages are relatively straightforward [11]–[13]. However, *accurately and simultaneously delivering the intended calculated bias current to all PJVS subarrays* (in typical measurement environments) requires careful attention to the design of the bias electronics. Additionally, it is desirable to have bias electronics with component tolerances sufficiently tight that they never require calibration. The critical design considerations are shown in Table I.

The target bias set-point accuracy of $\pm$0.05 mA on each channel was chosen by assuming a 1 mA minimum step current range for every subarray and by our desire to have ten discrete points on each step. The resulting step increment of 0.1 mA allows a sufficient number of points on each step to ensure that the set points are properly centered and to carefully measure PJVS step flatness and step-corner behavior. To accomplish

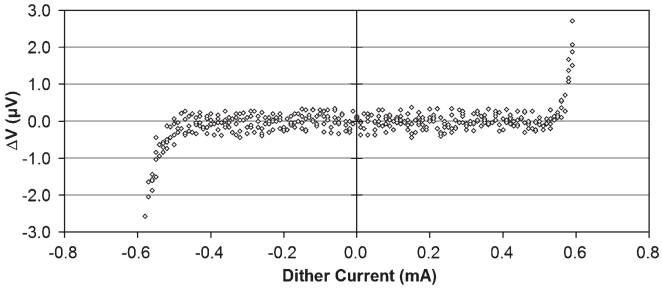

Fig. 2. Operating current margin measurement of a 10 V PJVS circuit in one of the most demanding output voltage states for the bias electronics, pnpnpnpnpnpnpnpnpnpnp. The "dither" current is an offset current through all subarrays of the device and shows how much current the PJVS can source or sink before moving off the quantized Josephson voltage step. The measured center of the "on step" section of these data is +0.04 mA even for this "worst case" subarray combination with all drive channels active.

TABLE II
BIAS ELECTRONICS SET-POINT ACCURACY DATA

Output State (10V PJVS circuit configured as 23 sub-arrays)	Measured Step Center (mA)	Measured Total Step Width (mA)
"pnpnpnpnpnpnpnpnpnpnpnp" (Fig. 2)	+0.04	1.02
"npnpnpnpnpnpnpnpnpnpn"	+0.02	1.03
"ppnnppnnppnnppnnppnnpnn"	-0.03	1.05
"nnnpppnnnpppnnnpppnnnpp"	+0.02	1.04
"ppnnnnpppnnnpppppnnnnn"	-0.01	1.05
"nnnnnnnnnnnnpppppppppp"	+0.03	1.07

this, the sum of all five values in the rightmost column of Table I must not exceed the worst case limit of 0.05 mA. Because the values in Table I are worst case, it is anticipated that the typical set-point deviations will generally be a little more favorable (possibly within $\pm$0.03 to $\pm$0.02 mA), which would be helpful when characterizing Josephson steps smaller than 1 mA.

To determine how well the bias electronics meets the specifications in Table I, the parameters of each channel can be measured and compared to the target values in the table. The first three rows of requirements are easy to verify (since they constrain the value of an individual component), and channel-to-channel measurements are performed to confirm the requirements of rows four and five because these values depend upon the many components that comprise the output stages. We have performed many such tests during development, but a much faster and more meaningful method of evaluation is shown in Fig. 2. The PJVS output states that are most sensitive to nonidealities in the bias system are those where all the odd subarrays are set to the opposite polarity of all the even subarrays. This bias configuration maximizes the current flowing on all drive channels, thus maximizing the effect of channel-to-channel mismatch of gain, dc offset, and resistances, including those of the amplifier output stages and cryoprobe lines. Of course, in this "pnpnpnpnpnpnpnpnpnpnp" state, there is a possibility that some of these errors might cancel each other to

TABLE III
10 V PJVS CIRCUIT OPERATING PARAMETERS

Cell Number	Number of Josephson Junctions	Positive Set Point (mA)	Negative Set Point (mA)	Range +1 State (mA)	Range 0 State (mA)	Range -1 State (mA)	Critical Current (mA)
23	8400	12.37	-12.38	1.28	10.35	1.26	10.76
22	8400	12.35	-12.25	1.25	11.42	1.32	11.26
21	8400	11.95	-11.99	1.33	10.45	1.38	10.98
20	8400	12.15	-12.16	1.34	10.74	1.36	11.10
19	8400	11.78	-11.79	1.66	10.03	1.68	11.06
18	8400	12.06	-12.08	2.10	10.86	2.11	11.69
17	16800	11.55	-11.55	1.86	9.62	1.86	10.93
16	16800	11.65	-11.71	1.57	9.95	1.60	10.86
15	16800	11.52	-11.51	1.66	9.26	1.65	10.80
14	16800	11.67	-11.68	1.60	9.47	1.62	10.84
13	16800	11.27	-11.31	1.84	9.20	1.86	10.79
12	8400	11.70	-11.73	1.55	10.30	1.58	10.80
11	8400	11.85	-11.91	1.42	10.42	1.33	10.84
10	16800	11.56	-11.60	1.46	9.31	1.46	10.70
9	16800	11.56	-11.57	1.55	9.30	1.55	10.74
8	8400	11.17	-11.19	2.05	8.54	2.05	10.76
7	8400	11.02	-11.01	1.95	8.61	1.95	10.80
6	16800	11.50	-11.50	1.71	9.74	1.97	10.77
5	16800	11.36	-11.36	1.70	8.75	1.70	10.72
4	8400	11.25	-11.26	2.18	8.61	1.76	10.85
3	8394	11.41	-11.42	2.21	9.39	2.22	11.01
2	8400	11.06	-11.02	2.38	8.22	2.34	10.81
1	8400	10.88	-10.99	2.12	8.24	2.14	10.98

Measured bias parameters for a 10 V PJVS circuit operating at 18.52 GHz. This particular circuit is a triple-stacked 10 V circuit with 32 sub-arrays, each having 8400 Josephson junctions. Many of the sub-arrays are sufficiently identical that they can be simultaneously operated from a single common drive channel. The table shows data for many sub-array pairs that are biased in common so that we can test all drive channels of the bias electronics. An important detail to observe is the matching between the measured bias current values for positive and negative voltage states of a given cell. This is a rough indication of how accurately and precisely we expect the applied biases to agree with the target setpoint biases in an ac waveform.

some degree. In order to ensure that the bias set-point accuracy is working properly for arbitrary combinations, we perform this same "flat spot" measurement at dozens of other PJVS output voltages where the output state of each subarray is randomly selected. Examples of such measurements are shown in Table II.

During stepwise ac operation, the bias electronics utilizes a versatile onboard clock and timing card, which allows the ac PJVS to be synchronized with other measurement electronics. The waveform memory is loaded with up to 4095 PJVS states that comprise the stepwise-approximated arbitrary waveform. When the bias electronics switches from one quantized PJVS state to another, the output DACs on every drive channel update simultaneously with a settling time at the PJVS circuit of 200 ns. At the present time, we are primarily interested in using stepwise ac PJVS waveforms to perform synchronized sampling comparisons with other sources [9], [10], so a 200 ns transition time is perfectly acceptable for that purpose. In a future improvement, we will modify the DAC outputs to minimize the settling time, which may be useful for some applications.

III. PJVS CONTROL SOFTWARE

The new comprehensive software control program is designed for maximum flexibility. Not only does it control our most recent 24-channel bias electronics described earlier for the new NIST 10 V PJVS system, but also it operates several older ac and dc PJVS bias modules. These older bias electronics require frequent calibration procedures so that a correction table of the gains and dc offsets of each individual channel can be measured and compensated during subsequent PJVS operations.

The software utilizes a nanovoltmeter to precisely determine the center position and step height of the quantized output voltage states for each PJVS subarray, as shown in Table III. It takes about 15 min for the software to determine (to 1 μV precision) the bias parameters for a particular microwave frequency and power, after which the PJVS is ready for precision dc or stepwise ac operations. Typically, it is desirable to remeasure the parameters in Table III every few days to ensure consistent system operation.

IV. 10 V PJVS CIRCUIT PERFORMANCE

Details of NIST superconductor–normal-metal–superconductor PJVS circuits, systems, and bias methods have been described elsewhere [11]–[13]. In recent years, numerous technological improvements [14]–[16] have enabled the successful development of 10 V PJVS circuits with practical operating margins. The culmination of those efforts is illustrated in Fig. 3(a), which shows the operating current margins over a range of microwave frequencies for two 10 V PJVS devices (from different wafers whose junctions have different critical currents). The reproducible broad frequency response of these 10 V circuits is due primarily to the improved PJVS microwave design, which features an integrated 32-way microwave splitter that resides entirely on chip.

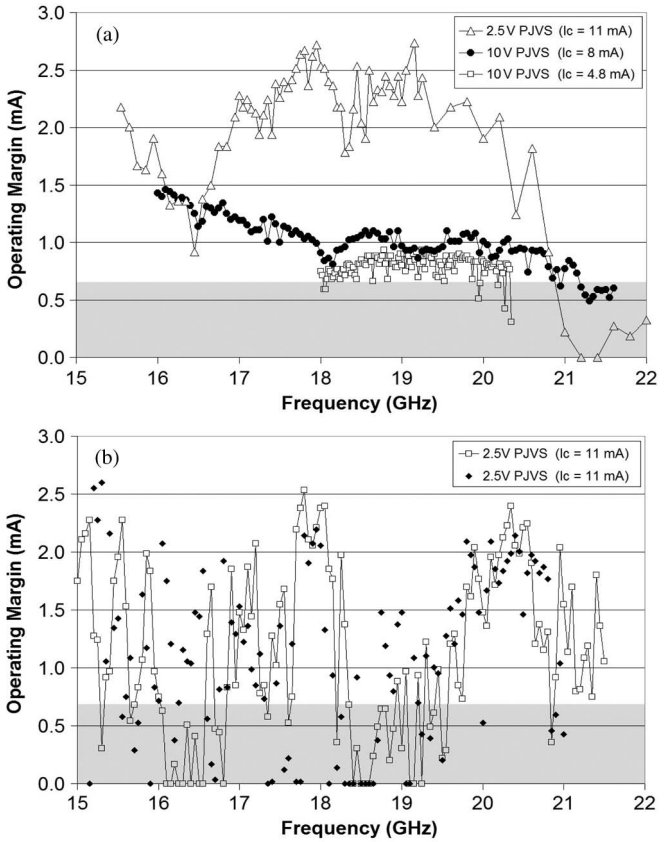

Fig. 3. (a) Measured operating current range for several "flip-chip-on-flex" cryopackaged PJVS devices at numerous microwave frequencies. Each current value is the height of the quantized PJVS output voltage when all subarrays are biased at nonzero voltage steps. The 10 V chips have 32 subarrays (a total of 268 800 Josephson junctions), and the 2.5 V chip has 13 subarrays (a total of 58 620 junctions). (b) Measured operating current range for two typical 2.5 V PJVS circuits mounted in flex-bonded cryopackages. The most robust operating points are those values *above* the 0.7 mA gray-shaded region.

Fig. 3(a) also shows our "best case" 2.5 V PJVS that utilized our previous generation technology in the design of the chip and cryopackage. This configuration consisted of a four-way microstrip splitter on the flex cryopackage, followed by four two-way splits on chip, which, in total, produced an eight-way microwave split. This approach consistently produced 2.5 V devices with very large operating margins (2 to 3 mA at several microwave frequencies). We have flex bonded over a dozen PJVS chips of this design, and although they provided perfect operation at numerous frequencies over a range of several gigahertz, more typical behavior is shown in Fig. 3(b). Operating points that have a current margin greater than 0.7 mA (i.e., above the gray-shaded region) are most desirable for system reliability. Chips made with this technology tended to have useful margins in the frequency range from 17.6 to 18.2 GHz and also in the range from 19.8 to 20.5 GHz. However, the rest of the frequency range generally produced a mixture of varying performance, having excellent margins at some frequencies while having unusable or zero margins at neighboring frequencies. Usually, these "low-margin" frequencies were due to just one or two subarrays that were receiving nonuniform microwave power, and the particularly low-margin subarrays often varied across the frequency range.

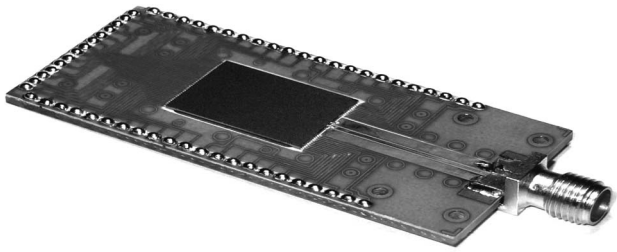

Fig. 4. Photograph of a newly developed flip-chip-on-flex cryopackage for the 10 V PJVS devices. The 330 μm center-to-center finger spacing of these new cryopackages is half that of their predecessors due to the large number of wiring connections required (and the fact that the 12 mm-by-17 mm 10 V circuits have room for pads on only two sides).

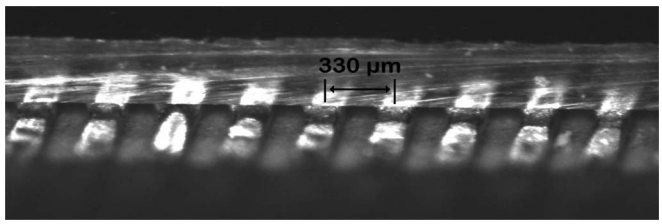

Fig. 5. Magnified view of the InSn solder bonds between (top) a 10 V PJVS silicon chip and (bottom) the copper traces on the "flex" microwave dielectric base layer. The recently reengineered chip-bonding machine precisely controls the thickness of the solder in the gap (approximately 50 μm on this cryopackage). *(Note: The mirror finish of the diced chip edge shows the reflection of the copper fingers below.)*

Exactly why the typical 2.5 V devices of Fig. 3(b) are so different from that of Fig. 3(a) is not fully understood, but it is likely related to variability in the features that comprise the eight-way microwave splitting network to the Josephson arrays. The microwave path includes a coax-to-microstrip transition onto the cryopackage, a four-way symmetry-based microstrip splitter (that may permit the subarrays to affect each other's microwave uniformity), four microstrip-to-coplanar stripline transitions at the chip interface (with through-hole vias adding additional nonidealities), and more on-chip splitters and impedance transformers. It is conceivable that, with such a complex microwave-distribution configuration, a random defect or abnormality (on chip or at the soldered cryopackage-to-chip interface) could produce a frequency-dependent nonuniform microwave power distribution. Thus, for the new 10 V PJVS devices, we elected to place the entire splitter network on the chip itself, which streamlines the cryopackage by replacing the various microstrip features with one coplanar stripline from the coax to the chip. An example of such a cryopackage is shown in Fig. 4, and in Fig. 5 we show an end view of a bonded 10 V PJVS chip, which illustrates the uniform solder bonds and precise chip alignment made possible by our new flip-chip-on-flex bonding machine.

Presently, the 10 V PJVS operating margins [Fig. 3(a)] are smaller than the typical 2 mA margins of our lower voltage 2.5 V devices. However, the lower current range is partially due to the lower critical current of the junctions in the 10 V circuits (roughly half the critical current of the 2.5 V devices). This lower critical current was intentionally chosen to reduce the circuit's total power dissipation so that its heat load would be more compatible with cryocooler operation.

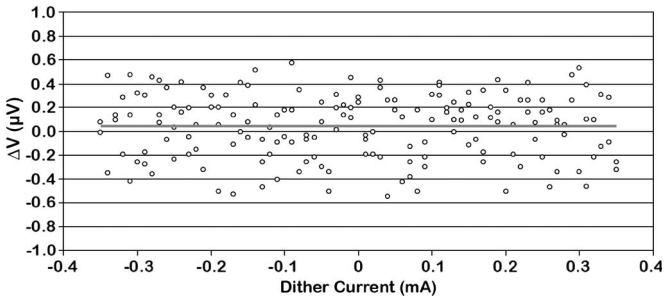

Fig. 6. Measured output voltage deviation from the expected quantized dc voltage versus dither current for a 10 V PJVS with all 32 subarrays active. These particular data demonstrate a perfectly flat "operating margin" of 0.7 mA (for the device in Fig. 3(a) having $I_c \approx 4.8$ mA). The dither bias current flows simultaneously through all cells.

Fig. 6 shows a 10 V PJVS output voltage step that is perfectly "flat" (i.e., constant voltage within the noise of the measurement) over a full 0.7 mA range of bias current with all the junctions biased at a nonzero voltage. Half of the junctions are biased on the positive voltage step, and the other half are biased on the negative step, which, in combination, produces a small net voltage that can be measured on a low voltage range. The microwave drive frequency is 19.3 GHz for this measurement, and the total usable step height is 0.7 mA. The calculated slope is -9 ± 41 nV/mA $(k = 2)$, which has an uncertainty of ± 5 parts in 10^{10} for a bias-current set-point accuracy of ± 0.1 mA. The measurement uncertainty could be reduced further by using a lower voltage range and averaging more data.

V. 10 V PJVS Applications

PJVS systems are capable of both dc metrology and stepwise-approximated ac voltage metrology, and they can perform a wider range of applications than conventional JVS systems. For dc metrology, the benefits offered by PJVS systems are higher noise immunity (generally, no filtering is required on the PJVS output voltage connections), inherent output stability, and ease of automated system setup and operation. For ac applications, PJVS systems offer rapid programmability and large output voltages with stepwise-approximated waveforms. Unfortunately, this method of ac synthesis cannot approach the unprecedented low distortion and high spectral purity that have been demonstrated by pulse-driven ac JVSs (ACJVSs) [17]. However, since ACJVS systems are presently limited to 250 mV rms, PJVS stepwise ac synthesis is worth exploring, because 10 V circuits can produce rms voltages up to 7 V, as shown in Fig. 1.

There has been extensive research over the past decade into the use of PJVS systems for stepwise-approximated ac waveform synthesis. Stepwise ac metrology with PJVS systems has been most successfully implemented through the use of digital sampling techniques [9], [18], with the best uncertainties at frequencies of 50 to 60 Hz for power applications [19], [20]. Recent research and specialized measurement methods suggest that useful stepwise ac voltage measurement techniques may be extended up to audio frequencies. However, as we have previously reported [21]–[23], there are significant challenges that must be circumvented in order to accomplish this.

VI. Future Directions

Our most recent efforts have concentrated on verifying the robust functionality of all the new 10 V PJVS system components for dc operation, but we are now starting to evaluate system performance for stepwise-approximated ac operation as well. The present objective is to verify that the bias-current set points for each subarray are consistent for all subarray output combinations, particularly for more dispersed random combinations of the $+1$, 0, and -1 states, because these require the bias electronics to supply the largest currents on many drive channels simultaneously and are therefore more sensitive to any channel-to-channel nonidealities. Also, these widely varied output states cause very different amounts of power to be dissipated in the output amplifiers, and performance verification under these conditions is an important task to ensure that the bias electronics will consistently produce the targeted subarray bias set points at update rates of hundreds or thousands of samples per second.

In stepwise-approximated ac synthesis, we refer to the PJVS as an "adjustable" voltage standard because the output voltage can be "adjusted" over a wide range of output values by changing various parameters that change either the shape of the PJVS I–V curves or the bias-current set points on the steps [21]–[23]. The objective for over 15 years has been to determine how to implement a PJVS that behaves as a truly intrinsic standard in stepwise ac mode, i.e., where the rms output voltage can be precisely computed from the sequence of PJVS voltages and their timing. Unfortunately, this goal is still elusive after all these years, particularly at audio frequencies, for the reasons that we described [21]–[23], and the primary standard worldwide for ac voltage is still ac–dc transfer.

Of course, we could consider using a thermal voltage converter (TVC) to "tune" the PJVS ac rms voltage to an ac–dc difference of zero and then operate the PJVS as an ac source at that operating point. However, such methods merely exploit the relative stability of the PJVS, because the true ac reference is still the TVC, and the Josephson voltage is not determined and irrelevant to the measurement. The PJVS in such a measurement scheme is unnecessary, because a stable ac calibrator could be used to accomplish exactly the same measurement.

In pursuit of the original objective of accurately determining the PJVS synthesized rms voltage without the use of a TVC, we prefer the following scheme: 1) Digitize the entire ac PJVS stepwise-approximated waveform with a sigma–delta analog-to-digital converter; 2) apply our knowledge of the sections of the PJVS waveform that are precisely known (i.e., the voltage values of the fully settled PJVS steps) to correct the gain and dc offset of the digitizer (and also remove the drift in those quantities on a very small timescale); 3) average thousands of waveform cycles to reduce measurement noise; and 4) account for effects due to the finite bandwidth of the digitizer. All this data processing will yield a value for the rms voltage of the PJVS, but the analysis also requires the evaluation of systematic errors in this complex measurement process. Fortunately, the ac PJVS has additional characteristics that we can utilize to reveal systematic errors in the digitization. Specifically, the transition timing shifts that make the ac PJVS output adjustable

[21], [22] have a magnitude that scales directly with the PJVS output frequency. In other words, a plot of "rms voltage versus microwave power" at 1 kHz, for instance, will have a specific slope (due to the rise time of the bias electronics), and at 2 and 3 kHz, the measured slopes will be exactly $2\times$ and $3\times$ higher, respectively. Furthermore, since these plots at different frequencies have different slopes, the plots have to intersect each other somewhere, and as many of us have observed [21], [24], it often happens that, over a significant PJVS output frequency range, the plots intersect around a common point. We propose to utilize our knowledge of the slopes of these data and the nature of those intersections to derive further information about the PJVS rms voltage and then compare predicted PJVS behavior with the measured PJVS data from the digitizer. We believe that this consistency check may eventually be accomplished with agreement of a few parts in 10^7 at 1 kHz, which would allow us to finally reach our objective of creating a measurement method with ac PJVS stepwise synthesized waveforms with precisely calculable rms voltage without the use of either ac–dc transfer or a TVC reference.

VII. Conclusion

NIST has developed a PJVS system at 10 V for both dc metrology and stepwise-approximated ac synthesis. All system components have been redesigned and optimized so that these systems are a long-term alternative to "conventional" 10 V JVS for users who desire additional measurement capabilities. These new systems incorporate a modular design philosophy to facilitate easy verification (and repair if necessary) of as many components as possible. Additionally, several of the PJVS subsystems are widely available commercial products with multiple suppliers, which enables long-term reliability and rapid repair time.

Acknowledgment

The authors would like to thank Y. Chong, N. Hadacek, B. Baek, and M. Watanabe for helping develop the stacked junction fabrication process used for the programmable Josephson voltage standard (PJVS) circuits. The authors would also like to thank I. Budovsky for providing a precision buffer amplifier to support ac PJVS development and for the collaborative discussions regarding ac waveform synthesis using Josephson arrays. Contribution of the U.S. government is not subject to copyright. The National Institute of Standards and Technology is part of the Technology Administration, U.S. Department of Commerce.

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