NIST 10 V Programmable Josephson Voltage Standard System Using a Low-Capacity Cryocooler

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***Abstract*—The recent shortage and increasing cost of liquid helium provides motivation for cryogen-free operation of superconducting devices such as NIST programmable Josephson voltage standard (PJVS) systems. However, operation on closed-cycle cryocoolers must not compromise the performance of the PJVS system. New cryogenic packaging and cryostat integration are presented that have been optimized for the NIST 10 V PJVS, demonstrating improved attenuation of coldhead temperature oscillations, and improvement of thermal conductances in the junction-to-coldhead path. When combined with an improved design of 10 V PJVS devices employing $Nb/Nb_xSi_{1-x}/Nb$ junctions with increased operating margins, we have operated a NIST PJVS at 10 V with over 1.32 mA current margins on a nominal 200 mW cryocooler using a 3.0 kW water-cooled compressor. The new cryo-package, in conjunction with the improved generation of chips, eliminates the need for liquid cryogens in applications using NIST 10 V PJVS systems.**

***Index Terms*—Josephson arrays, standards, superconducting device packaging, superconducting integrated circuits, voltage measurement.**

I. Introduction

PROGRAMMABLE Josephson voltage standard systems are becoming a more common alternative to conventional Josephson voltage standards to represent the SI volt [1]–[4]. 10 V PJVS systems utilize between 10^5 to 10^6 superconducting Josephson junctions (JJs) to realize a quantized voltage step that is determined solely by fundamental constants, the number of JJs, and the frequency of the microwave bias signal. Operation of 10 V PJVS systems on cryocoolers [5]–[7] presents complications that are not present during operation in liquid helium. Previous work [8], [9] on the operation of a NIST 10 V PJVS on a closed cycle cryocooler implied that ideal operation—i.e., achieving 1.0 mA current margins, as defined in Section II, with all sub-arrays biased—would require a cooling power of nearly 500 mW at 4 K. However, in this paper we present packaging and cryogenic improvements which, combined with increased JJ uniformity of the PJVS chip fabrication [10], have enabled successful operation at 4.3 K on a nominal 200 mW coldhead with a 3.0 kW water cooled compressor. Identical performance would be expected using an air cooled version of the same compressor, however at a slightly higher power consumption of $\sim$3.4 kW. This paper presents the recent developments that have enabled the dissemination of a cryogen free NIST 10 V PJVS.

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II. PJVS Operation and Operating Margins

To optimize operating margins, PJVS arrays are typically biased on the first Shapiro step $(n = 1)$ [11]. The term "operating margin" refers to the range over which those parameters affecting the operation of the PJVS may vary without affecting the output voltage of the PJVS. These parameters include Josephson array temperature, dc bias current, and microwave input power. For example, the dc bias current operating margins of the PJVS are measured by determining the range over which the bias may be dithered while maintaining a constant voltage step. This flatspot width shows how much current the PJVS can source or sink before moving off the quantized voltage step.

The JJ temperature, the dc bias current, and the microwave input power are interrelated when operating the PJVS on a cryocooler, because changing any one of these parameters affects the operational range of the other two. The heat capacity of a helium bath is large, hence when operating in liquid helium, the PJVS chip temperature is essentially constant as long as the heat flux is below the nucleate to film boiling transition. Thus, for practical purposes, microwave input power and PJVS output voltage can be varied without changing the junction temperature. In a cryocooled system, however, the chip temperature is defined by the load curve of the cryocooler and the actual power dissipated at the cryocooler second stage (the coldhead). The chip temperature is also somewhat higher than that of the coldhead due to the thermal impedance of the cooling path.

The heat load presented to the coldhead arrives via two paths: heat conducted from the first stage down the dc wires and microwave coax, and power dissipated on the chip itself. The on chip dissipation is the sum of the microwave power and the dc power dissipated in all the sub-arrays and terminations. The present generation NIST 10 V PJVS employs a 32-way microwave splitter that divides the Josephson arrays into individual segments, which the PJVS electronics groups into 23 sub-arrays that are independently current biased either on the positive or negative voltage step. After the current margins of each sub-array have been measured, the output voltage of the PJVS can then be "programmed" by biasing the desired sub arrays either positive (p), negative (n), or zero (0). The total PJVS output voltage is simply the algebraic sum of the voltages from all the sub-arrays, and the current margin for a given voltage is typically limited by the sub-array with the smallest individual

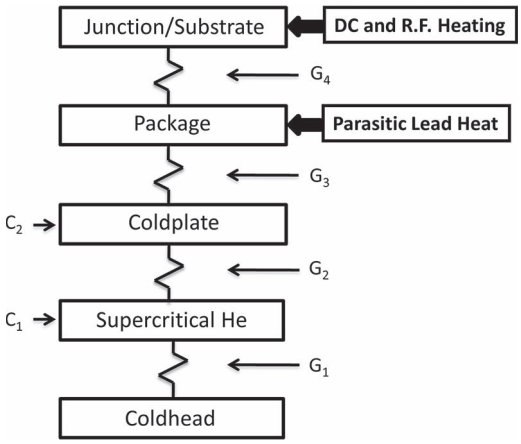


Fig. 1. Thermal block diagram for the improved cryostat. The junction-substrate conductance is very large so the JJ and substrate temperature are considered to be identical. $G_4(> 12$ W/K) is the In solder joint to the Au-Pd metallization on the backside of the substrate. G_3 and G_2 are pressed In foil connections ($\sim$3 W/K). G_1 exists due to the supercritical He reservoir in the coldhead assembly and is non-configurable but large. G_2 and C_2 comprise the second stage of the thermal filter as described in [8].

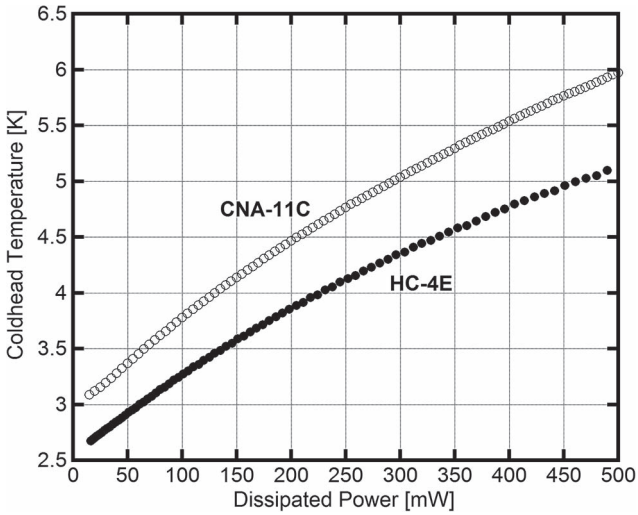


Fig. 2. Load curve of the new cryostat employing a Sumitomo RDK-101DP coldhead with two different compressors: the CNA-11C (air-cooled) and the HC-4E (water-cooled). Includes all parasitic heat loads.

margin. The on chip dc power dissipation is the sum of the products $I_{\rm bias}V_{\rm sub\text{-}array}$ for all biased sub-arrays. When providing the maximum 10 V output, the chip produces the maximum dc dissipation, which is about 100 mW for a nominal 10 mA bias.

In liquid helium, microwave power and microwave frequency are chosen to maximize the current margin, and the frequency may be fine tuned to obtain a precise output voltage. Normal microwave power dissipation at 4 K, from the chip and loss in the coax, is $\sim$250 mW. When operating on a cryocooler, however, increases in microwave power result in increases in on chip temperature and subsequent reduction of current margins. Thus, determination of the optimum operating conditions is somewhat more complex due to the concurrent optimization of microwave power, dc power, and chip temperature [12].

III. Cryogenic Systems

Use of a cryocooler to cool a PJVS presents three technical challenges not present with liquid helium. First, as noted above, due to the existence of a load curve, the temperature of the coldhead and thus of the PJVS, is a direct function of the heat dissipated on chip. Second, the temperature of the coldhead oscillates at the cryocooler operating frequency ($\sim$1.2 Hz). Third, use of a cryocooler requires the transfer of heat through multiple mechanical joints creating a temperature gradient between the PJVS circuit and the coldhead. In previous research [8], [9], a Sumitomo RDK-101D/CNA-11C cryocooler[1] was used, but the cooling capacity of such a system and its temperature stability proved to be insufficient to successfully operate the current NIST PJVS at 10 V.

A thermal block diagram is shown in Fig. 1. Maximization of the thermal conductances G_2–G_4 was addressed extensively in [8], [9]. The recent focus has been on reducing thermal oscillations and increasing the net cooling power available at the chip—partially by reducing the parasitic heat loads through a redesign of the cryostat. The previous cryocooler was replaced with a Sumitomo RDK-101DP/HC-4E that attenuates temperature oscillations through use of a supercritical helium reservoir integrated into the coldhead. This supercritical helium reservoir provides a large specific heat at C_1 and a large G_1 through the He in the reservoir. This combination replaces the brass shim/Pb block 'RC' thermal filter which comprised G_1 and C_1 in the previous design [8], [9]. The supercritical helium reservoir, in conjunction with a 1.6 kg Cu mounting surface known as the coldplate (C_2) and the conductance G_2, attenuate temperature oscillations at the PJVS chip to 38 mK peak to peak at 4 K. Previously oscillations were 136 mK peak to peak. Elimination of the brass shim also removes a 1.44 W/K conductance at G_1 thus reducing the temperature gradient between the chip and the coldhead by $\sim$0.25 K during 10 V operation. The HC-4E compressor supplies a higher flow rate of helium gas to the coldhead, providing increased cooling capacity as shown in Fig. 2, although this increase in cooling capacity does come with the cost of increased compressor power consumption.

The cryostat wiring has been redesigned to reduce parasitic heat loads and provide leads for the PJVS output voltage with minimal thermoelectric voltage offset. Microwave signals are transported from room temperature to the PJVS chip via 2.19 mm diameter coax with a Cu-Ni outer conductor and Ag plated Cu-Ni center conductor. This combination minimizes the parasitic power (conduction plus dissipation) applied directly to the coldhead. DC bias and thermometry leads are woven looms of phosphor bronze twisted pairs. The PJVS output voltage is routed via a continuous pure Cu twisted pair, which runs from the solder pads on the chip package, through a vacuum feedthru, to the measurement instrumentation. All wiring is heat sunk to both stages of the cryocooler; the Cu voltage leads and looms via epoxy impregnation and the coax via clamps augmented with thermal grease. Furthermore, through the development of a new chip package (discussed in the following section), we have optimized the Cu carrier to eliminate extraneous pressed In mechanical joints and their attendant thermal impedance.

[1]Commercial software and instruments are identified in this paper to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the equipment identified are necessarily the best available for the purpose.

IV. Packaging Improvements

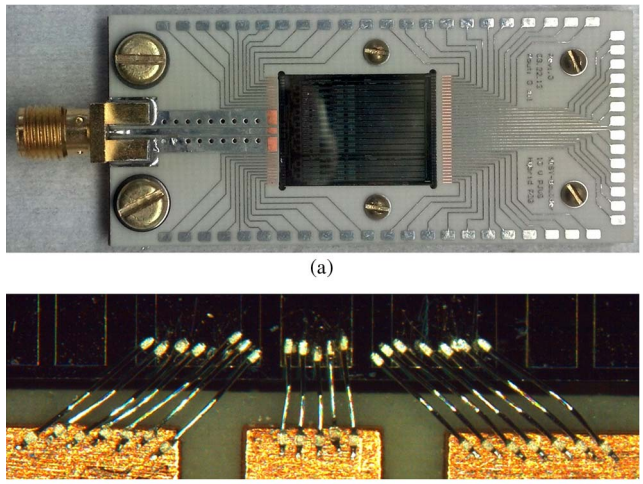
A. Chip to Carrier Solder Connection

In [8] we proposed a method of soldering a copper carrier directly to the back of a PJVS chip by applying metallization to the chip backside, followed by an automated soldering process using pure In solder. During extended reliability testing after publication, it was found that the CrCuAu multilayer metallization on the back of the chip provided a limited process window for bonding the chip to the Cu carrier. This was due to the rapid diffusion of In through the Cu metallization, and the fact that once the In diffuses completely through the Cu it will not adhere to the Cr layer. Bonding of chips outside the narrow process window resulted in bonds with poor mechanical strength, low thermal conductance, and a tendency to delaminate after repeated thermal cycling. We have therefore incorporated backside metallization consisting of a Ti adhesion layer and Au-Pd sputtered alloy directly into the PJVS chip fabrication process. This approach ensures interface cleanliness for the deposition process and provides a wider process window for chip bonding. Additionally, the thickness of the In solder layer has been increased to better accommodate the shear strain generated by the differing thermal contractions of the Si chip and the Cu carrier. No adverse effects have been observed in the thermal or mechanical properties of these joints and the measured thermal conductances remain $\geq$ 10 W/K, which is an effective maximum for the chip carrier thermal interface [8].

B. Chip Interconnects and Printed Circuit Boards

The NIST flip-chip-on-flex package [13], which has been very successful for PJVS operation in liquid helium, incorporates copper traces on a thin RO3003 dielectric layer (the "flex"), which is bonded to a composite reinforcement. In the flex package, connections between the chip and the flex are made using Sn-In eutectic solder, and the microwave signal is transmitted via a co-planar waveguide from an SMA connector to the chip. This package has excellent microwave properties, but precludes the use of a soldered thermal interface between the PJVS substrate and a Cu carrier. We have instead employed a hybrid printed circuit board (PCB) that consists of a 0.3 mm RO4003C dielectric that is bonded on top of $\sim$1.3 mm composite (FR4). Cu layers exist on the top and bottom of the RO4003C forming a grounded coplanar waveguide (GCPW) designed to provide the best impedance match with a variety of 3.5 mm bulk mount SMA connectors [14]. Various GCPW configurations, including GCPW tapers, were modeled and several were tested for the best match to the on chip CPW [15]. In the new PCB based package, wirebonds are used to connect the PCB to the chip.

The wirebonded PCB-to-chip microwave launches can present a larger impedance mismatch compared to the previous flex packaging because of the intrinsic variability of wirebonds and the fact that the wirebonds do not form a well-defined microwave structure. To minimize the impedance mismatch, effort was made to decrease the air gap between the PCB and the chip, minimize the bond loop height, and increase the number of parallel bonds. The continuous wave nature of the microwave radiation leads to a reflection from this interface and acts only as a small reduction of power to the chip; there are no significant effects on any other operating margin. A completed package with wirebonds is presented in Fig. 3.



(a)

(b)

Fig. 3. (a) The new NIST 10 V PJVS wire-bonded chip package using hybrid-PCBs with an RO4003C dielectric top layer. This particular package has SnPb plated traces, except in the locations where the wirebonds connect. The 0–80 screws adjacent to the chip are used to attach a Delrin cover that protects the chip and wirebonds from user handling. (b) Close-up of the wirebonded microwave launch between the PCB and chip CPW. The center conductor of the PCB is 0.72 mm wide.

C. Wirebond Metal Characterization

Initially, Al wire was utilized, with Cu bond pads on the PCB and Au-Pd pads on the chip (which are necessary for rapid chip testing using a spring finger probe prior to packaging). During thermal cycling tests, significant corrosion of the bonds was observed, which resulted in failure of a number of wirebonds. This has been attributed to an electrochemical reaction between the Al wire and the Au-Pd pad, made possible by the condensation of water vapor on the package during rewarming.

One solution to wirebond corrosion is to use Au wire and Au PCB bond pads.

Another solution was to protect the PJVS devices from environmental degradation and water condensation with a chemical vapor deposition encapsulation process using the polymer Parylene. Parylene provides excellent protection against user and environmental damage to both the PJVS circuitry and the wirebonds, but it can affect the wirebond microwave performance, as Parylene encapsulation introduces a new dielectric in the wirebond region [16]. Presently, packages using both Al wire with Parylene encapsulation, and Au wire with no Parylene encapsulation have proven reliable in deployed PJVS systems. While the performance of a wirebonded CPW-chip microwave launch has been acceptable for PJVS (i.e., dc voltage standards), the wirebond microwave performance has been found to reduce operating margins for pulse-driven ac Josephson voltage standards (ACJVS), as compared to spring finger and flip chip bonded interfaces [2], [18]. This is because for ACJVS biasing a high fidelity of pulses is required over a much broader frequency range (up to 40 GHz), whereas for a PJVS the microwave bias is simply a $\sim$18 GHz continuous wave signal.

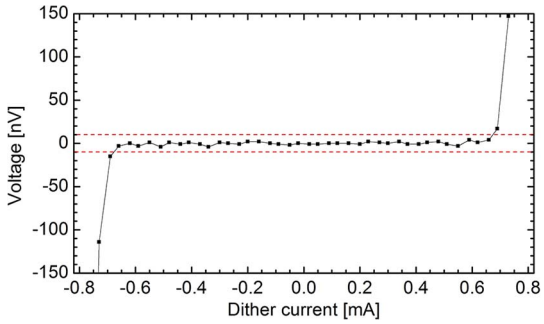


Fig. 4. Current-voltage trace of the PJVS zero net voltage step for the output state "pppppppppnnpnpnpnpnpnpnp" while operating at 4.3 K on the RDK-101DP/HC-4E cryostat. All sub-arrays on the 10 V PJVS chip are biased at a non-zero voltage, and the estimated total on-chip power dissipation is ∼300 mW. The current margin for this step is 1.32 mA. The dashed lines are at ±10 nV. The dither current is added in series across the entire array.

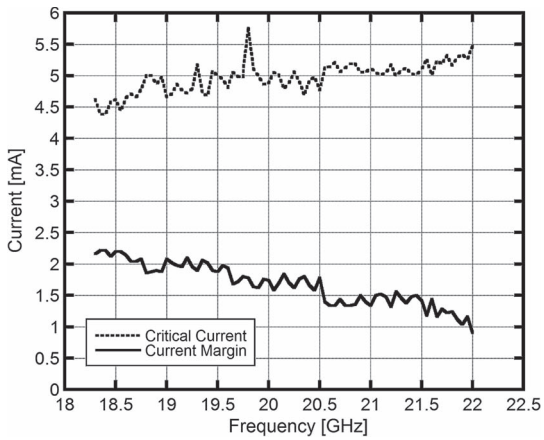


Fig. 5. Frequency dependence of the critical current and the current margin of the most significant bit (16800 JJs) with the lowest current margin. The 10 V current margins are largely determined by the sub-array with the lowest margins so we can expect the 10 V margins to be no worse than those of the worst sub-array. The absence of large resonance-like behavior is indicative that the microwave launch introduces no difficulties in operation over the 18 GHz–22 GHz frequency range.

V. Data

In combination with the latest generation of NIST 10 V PJVS chips [10], the new package design has enabled successful cryogen free operation. Fig. 4 demonstrates a 1.32 mA current margin at 18.38 GHz for state "pppppppppnnpnpnpnpnpnpnp," which is one of the most challenging because the heat load is nearly maximized. Such large current margins are due to both greatly increased current margins (1.90 mA in 4.0 K liquid helium when operated at the same microwave power as previous chip designs) of this chip, and to minimization of both cryocooler temperature oscillations and the chip coldhead thermal gradient. Fig. 5 shows the frequency dependence of the most significant bit (16800 JJs) with the lowest critical current and current margin. The fact that this sub-array has a current margin that is over 1.0 mA for a bandwidth of ∼18 GHz–22 GHz demonstrates that wirebonds do not introduce microwave resonances that would adversely affect current margins. Further details of NIST cryocooled 10 V PJVS measurements and operation, as well as temperature dependence of the PJVS current margins, are presented in [12].

VI. Conclusion

In this paper we presented a packaging method and cryogenic design for liquid cryogen free 10 V PJVS systems. By developing a dependable process of In soldering a PJVS device with Au-Pd backside metallization to a Cu carrier, we produced a high thermal conductance mechanical connection. Combining this scheme with minimization of cryocooler temperature oscillations and increased 10 V bias current operating margins from the latest PJVS chip revisions, we demonstrated successful operation of a NIST 10 V PJVS at 4 K with "worst case" current margins of 1.32 mA, effectively eliminating the need for liquid helium in future NIST 10 V PJVS systems.

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