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Simulation challenges in high-resolution $\Delta\Sigma$ ADCs: the experimental case study of CERN DS-22

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***Abstract*—The intrinsic switching nature of Delta-Sigma ($\Delta\Sigma$) Analog-to-Digital Converters (ADCs) makes challenging to achieve accurate and effective simulations. In this paper, several simulation models and methods are proposed and compared with actual measurements to demonstrate their accuracy. As an experimental case study, an upgraded design of the DS-22, presently in operation at CERN to regulate the output current of the main power converters of the world largest particle accelerator, the Large Hadron Collider (LHC), is presented. LHC upcoming upgrade, named High-Luminosity LHC, foresees a performance enhancement of the power converters and, in turn, its regulation capabilities. A strategy is to upgrade the DS-22 design by means of a reliable simulation model. In particular, a noise floor of about $186\,nV/\sqrt{Hz}$ for the Power Spectral Density (PSD) of the quantization noise is achieved showing a good agreement with the measurements.**

***Index Terms*—$\Delta\Sigma$ ADCs, PSpice simulations, Simulink, LHC, HL-LHC.**

I. Introduction

Many electronic measurements systems requiring very high-SNR exploit analog to digital converters based on the $\Delta\Sigma$ approach [1]. This is the case, among many others, of high-quality audio applications [2] or wireless communication systems [3].

$\Delta\Sigma$ modulators are in general very difficult to simulate because of the mixed signal nature of the feedback loop. The most common approaches are based on Spice modeling [4], solving differential equations analytically and numerically [5], implementing difference equations based on impulse invariance [6] and using Simulink [7]. Spice simulations usually begin with macro–level simulations using ideal components to determine the $\Delta\Sigma$ modulator ideal performance. Afterwards, specific transistor level models, can be substituted for the macro–level components to observe actual effects such as finite amplifier gains, parasitic capacitance, and so on. However, Spice simulations are very time consuming even for macro models, especially for higher-order $\Delta\Sigma$ modulators. $\Delta\Sigma$ modulators are also often simulated by solving differential equations describing the analog circuitry. Although this method is faster than Spice approaches, building up the system of differential equations can be quite difficult if reasonably high level of accuracy is required for the model. Indeed, the more accurate and complete the model is, the more complex the equations become. MATLAB/Simulink is a relatively simple and fast method for such simulations but it is usually used for behavioral high-level simulations. Indeed, accurate modeling of deeper effects of $\Delta\Sigma$ modulators is quite often very difficult to achieve with this tool. Another approach foresees the use of the *delta transform* to determine difference equations of the $\Delta\Sigma$ modulator [8]. These equations allow to determine the input at the quantizer next sample time by using the quantizer input and feedback signals at the current sample time. In conclusion, each simulation method has a trade-off between speed, simplicity and accuracy and the best method is very dependent on the specific application. For this reason, a unique tool cannot be identified for a complete simulation of a $\Delta\Sigma$ modulator.

At CERN, the next upgrade of the LHC, the world largest particle accelerator, named High-Luminosity LHC [9], needs a performance enhancement of the LHC power converters [10]. A measurement chain composed by a current-to-voltage transducer (*DCCT*) and a third–order $\Delta\Sigma$ ADC developed at CERN, named DS-22, is currently used to regulate the output current of the LHC power converters [11][12]. In order to achieve the required enhancements for High-Luminosity LHC, improving the performance of the measurement chain is crucial. One possible strategy is to produce an upgraded design of the DS-22. In this framework, having a reliable simulation model of the current version of the DS-22 is a key point of the new design.

In this paper, the simulations of a high–resolution third–order $\Delta\Sigma$ ADC are reported and discussed by referring to the challenging case study of the DS–22 at CERN. In particular, in section II, a brief introduction to the design of DS-22 is reported whereas in section III, the DS-22 Signal and Noise Transfer Functions are both simulated and derived analytically highlighting one of the limits of PSpice simulations in this context. Furthermore, the simulation accuracy is discussed

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DS-22 Performance	
ER @ 1 kS/s ($BW \approx 500$ Hz)	21 bits
ER @ 50 S/s ($BW \approx 25$ Hz)	23 bits
Non-Linearity Error (max)	≤ 1 ppm
Offset TC	$\leq \pm 0.5$ ppm/$^{\circ}C$
Gain TC	$\leq \pm 0.25$ ppm/$^{\circ}C$
Offset stability (1 week)	≤ 1 ppm peak-to-peak

TABLE I: DS-22 Performance

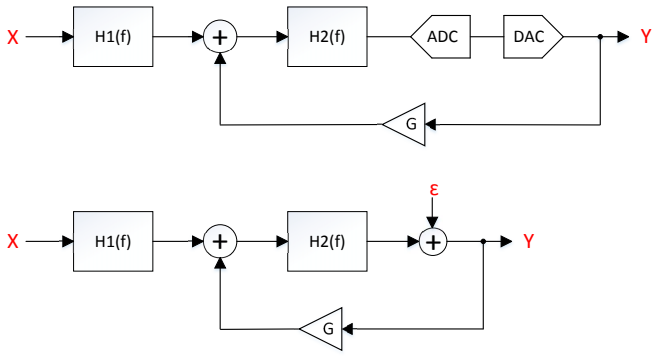


Fig. 1: Equivalent block diagrams of the DS-22 $\Delta\Sigma$ modulator. The bottom one is used to highlight STF and NTF.

and the importance of the simulation maximum step size is highlighted. Finally, in section V, a well–known undesired effect of $\Delta\Sigma$ modulators, the idle tones [13], is simulated.

II. Concept Design of the CERN DS-22

The DS-22 is a high-resolution 3^{rd} order $\Delta\Sigma$ ADC fully developed at CERN. Its metrological performance, reported in [14], is summarized in Table I.

Two equivalent simplified block diagrams of the DS-22 $\Delta\Sigma$ modulator are sketched in Fig.1.

It is composed by an input analog circuitry, $H_1(f)$, which is devoted to input buffering and a preliminary filtering of the out-of-band noise, followed by a chain of analog integrators, $H_2(f)$, whose number defines the order of the modulator. The integrated input is then quantized by the series of a 1-bit ADC and a 1-bit DAC which can be modeled as *additive quantization noise* as sketched in the lower side of Fig.1. Finally, the quantized output is fed back to the input of the chain of integrators. It is worth mentioning the presence of a gain stage (G) which is fundamental for stabilizing the loop.

The simplified schematics of the DS-22 is depicted in Fig.2. The input signal X is filtered by a 2^{nd} order low-pass RC filter and then buffered before entering the chain of three integrators. The first integrator also performs an inversion whereas the other two are non-inverting. It is worth noting that the presented $\Delta\Sigma$ loop is composed by the cascade of three integrators without intermediate feedback loops [12],[15] even though less common in literature. After being integrated, the input signal is compared with a triangular dither signal for idle tones suppression [13]; in this stage the signal is inverted again. In this design, the comparator represents the 1-bit ADC which quantizes the input signal. This has the big advantage of exploiting the very high linearity of a 1-bit ADC to digitize the input signal [16]. To close the feedback loop, the digitized signal has to be converted back to the analog domain. This is done by the 1-bit DAC depicted in Fig.2 for which similar considerations on the linearity of the 1-bit ADC remain valid. In order to uniquely define the switching instants a specific *guard pulse* is used to enable the *NAND* gates. It is worth mentioning that the PSpice default level for Analog-to-Digital interfaces (e.g. flip-flops, D-latches or logic gates) is set to 1. This enables the generation of the intermediate logic levels, called *R,F,* and *X*, when the input falls within the voltage range $[VIL_{MAX}\,,\,VIH_{MIN}]$ at the sampling instants. To disable this unwanted feature, level 2 is used. Finally, the *XOR* gates allow injecting a precise charge into the capacitor of the 1^{st} integrator by connecting the $\pm V_{REF}$ to the resistor network R_7, R_8, and R_9.

III. Signal and Noise Transfer Functions

Both noise and signal transfer functions, NTF and STF, can be derived by looking at the equivalent block diagram depicted in Fig.1 (bottom):

$$Y = \frac{H_1 \cdot H_2}{1 - G \cdot H_2} \cdot X + \frac{1}{1 - G \cdot H_2} \cdot \epsilon$$
$$\begin{cases} STF \triangleq \frac{Y}{X} = \frac{H_1 \cdot H_2}{1 - G \cdot H_2} \\ NTF \triangleq \frac{Y}{\epsilon} = \frac{1}{1 - G \cdot H_2} \end{cases} \quad (1)$$

It is worth noting that H_2 has a negative *DC* gain as will be shown in equation (3). For the DS-22:

- $H_1(s)$ is the transfer function of the second order low-pass filter implemented in the input stage.

$$H_1(s) = \frac{1}{1 + s\left(R_1C_1 + R_2C_2 + R_1C_2\right) + s^2 R_1C_1R_2C_2} \quad (2)$$

- $H_2(s)$ is the transfer function of the cascade of the three *integrators*. From Fig.2 it can be computed to be:

$$H_2(s) = -\frac{G_1(s)}{1 + sR_3C_3[1 + G_1(s)]} \cdot \frac{G_2(s)\left(R'_4 + R''_4 + \frac{1}{sC_4}\right)}{R'_4[1 + G_2(s)] + R''_4 + \frac{1}{sC_4}} \cdot \frac{G_3(s)\left(R_5 + \frac{1}{sC_5}\right)}{R_5[1 + G_3(s)] + \frac{1}{sC_5}} \quad (3)$$

  where $G_1(s)$ (for OPA627) and $G_2(s) = G_3(s)$ (for OPA2604) are the simplified models of opamps taken from their datasheets: nominal open-loop gain and single time constant low-pass behavior.

IV. PSpice Simulation

A. AC Simulation: Transfer Functions

A simplified circuit, shown in Fig.3 has been considered for this PSpice simulation aimed at comparing results with the NTF and STF derived in equation (3). The ADC and DAC (comparator and logic gates net in Fig.2 respectively) are omitted in this simulation as they are transparent with respect to these transfer functions. It is worth noting that the V_{REF} noise generator, discussed in section IV-B, has no impact on this simulation. The STF is obtained by connecting an AC

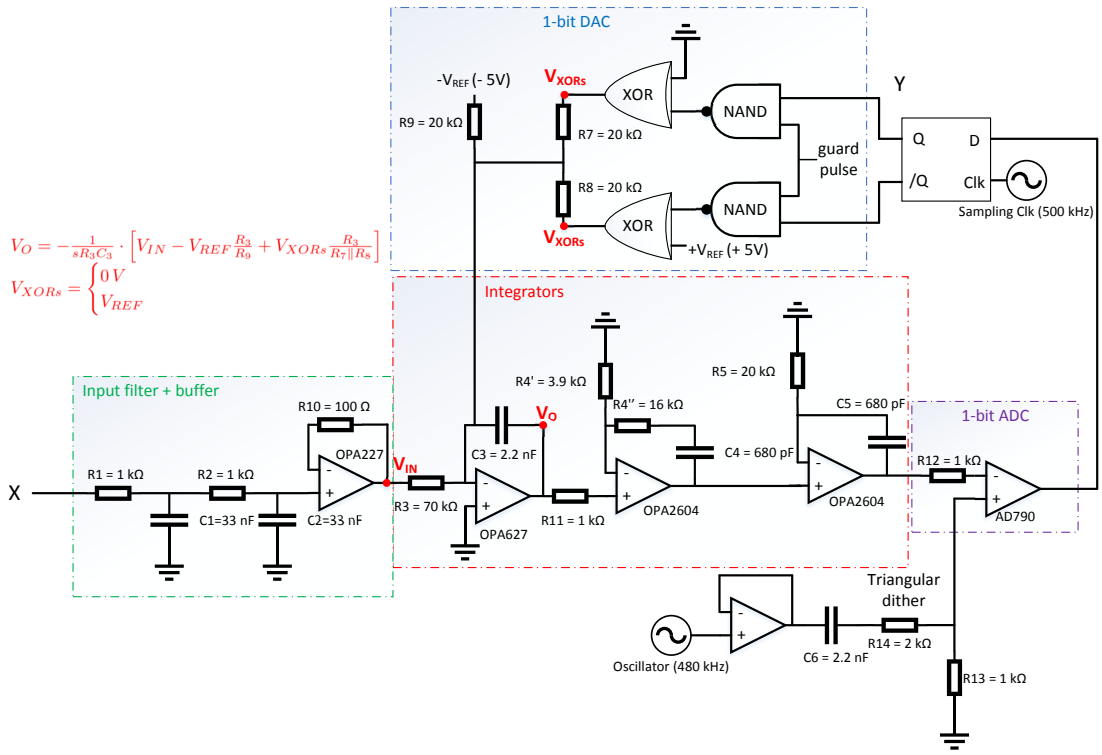


Fig. 2: Simplified DS-22 Schematics (used for PSpice transient simulations).

source to the modulator input X (and shorting ϵ to ground). Analogously, the NTF is simulated by connecting an AC source to ϵ and shorting X to ground. As it can be observed in Fig.4b, PSpice gives correct results down to 10 Hz, where the loop gain is very close to -200 dB. Below this point, the simulation accuracy becomes poor probably because of numerical stability issues at such high attenuations.

B. AC Simulation: Noise Floor

In this simulation, the noise floor of the DS-22 was simulated in its *flat region* (10 Hz to 300 Hz) with a PSpice noise analysis, ran at a temperature of 300 K. In Fig.3, the schematic used in this simulation is reported. As shown, only the analog circuitry was simulated, thus no quantization noise as well as no contribution from the logic net is included. An important contribution to the overall noise is given by the circuit generating the reference voltages ($\pm V_{REF}$). This is obtained with the state-of-the-art ultra-low noise voltage reference (*LTZ1000*) and a conditioning system to scale it to ± 5 V. This was simulated separately and demonstrated to be properly modelled by a white noise generator of roughly $40\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, equivalent to a $100\,\mathrm{k}\Omega$ resistor in series with the signal path, and a buffer, needed in order not to modify the loop gain. Finally, the noise obtained at the output node (Y) has to be scaled with respect to the full scale. This is done by multiplying it by the factor $\frac{70\,\mathrm{k}\Omega}{20\,\mathrm{k}\Omega}$.

The result of this test shows a noise floor in the *flat region* of about $-134.4\,\mathrm{dBV}/\sqrt{\mathrm{Hz}}$ ($\approx 191\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$), in very good accordance with the measurements carried out on a real DS-22 unit (blue curve in Fig.5) showing $-134.6\,\mathrm{dBV}/\sqrt{\mathrm{Hz}}$ ($\approx 186\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$). This is an important result which allows to verify with very quick simulations the impact of individual components on the noise floor. As an example, experimental tests on the real device showed that scaling down all the gain resistors (R_3, R_7, R_8, and R_9) by a factor of 8 would lower the noise floor to about $150\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Coherent results were reproduced in simulation with the above-mentioned model.

C. Transient Simulation: Noise Power Spectral Density

The aim of this DC simulation is to reproduce the noise performance of the actual device. Thus, the more complete (and complex) simulation model reported in Fig.2 was used. The input of the DS-22 is shorted to ground and the output of the modulator is saved and used to calculate the PSD of the noise. It is worth noting that the first ms of data obtained in PSpice are not saved in order not to consider the initial transients of the $\Delta\Sigma$ modulator. In particular, the stream of bits out of the modulator is scaled back to *Volts* considering the modulation factor of 80 % when the DS-22 is fed with 10 V; this is equivalent to having an analog $FS \approx 16.5$ V (it must be noted that DC gain of the whole loop shown in Fig. 1 is equal to $1/G$).

The PSD of the simulated DS-22 with shorted inputs is then calculated and compared with the one produced by an acquisition of a real unit opportunely scaled (blue curve in Fig.5). This has been done for different values of the maximum step size. As it can be observed, when the maximum step size is set to 10 ns (black curve), the simulation results

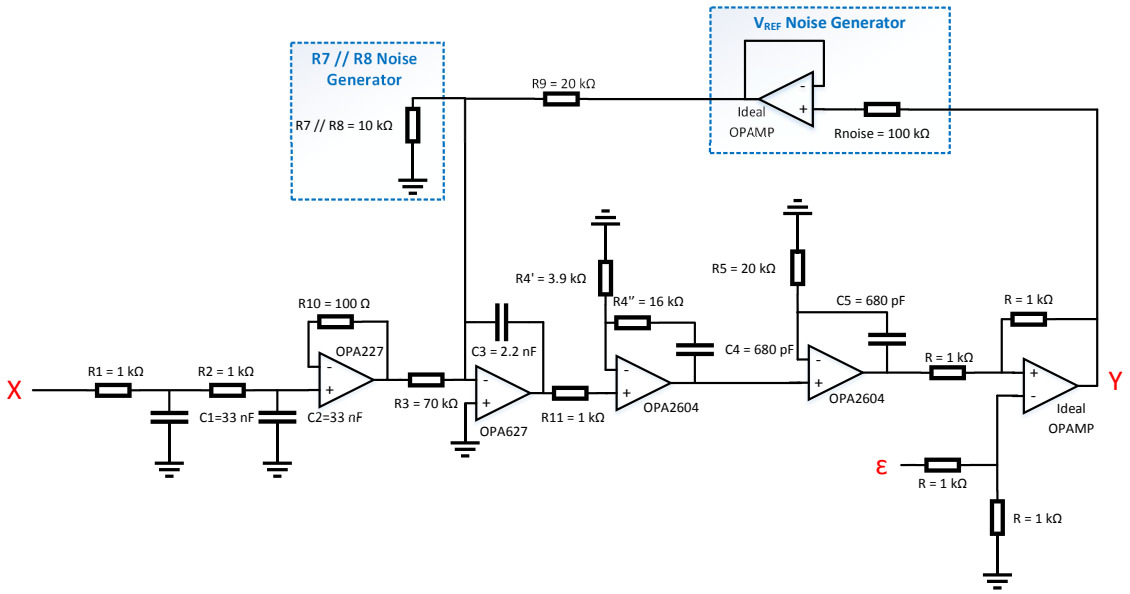
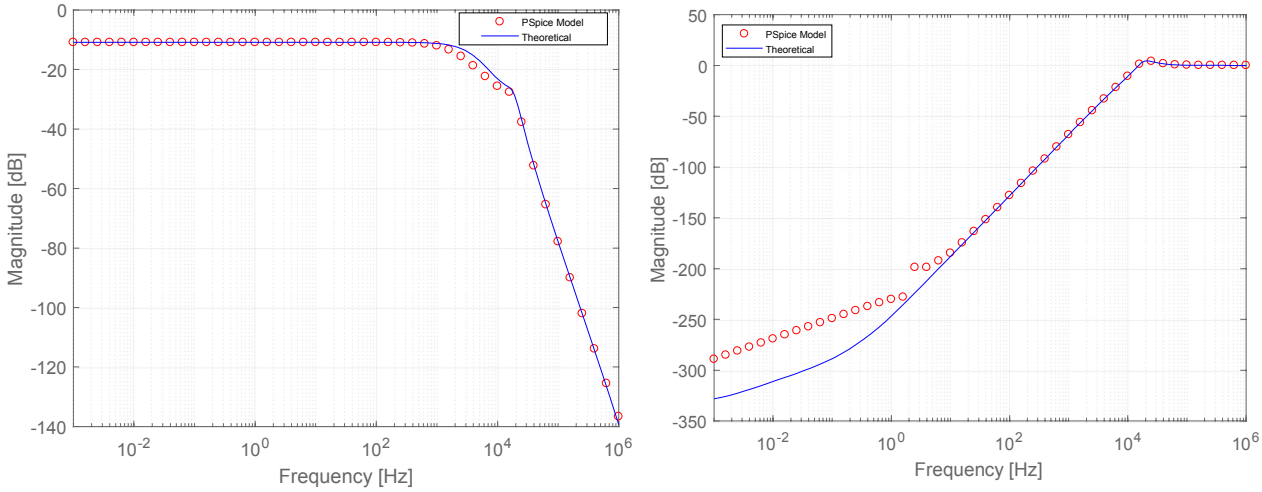


Fig. 3: DS-22 Schematics for PSpice AC simulations.



(a) (b)

Fig. 4: DS-22 Signal and Noise Transfer Functions: (a) Signal Transfer Function and (b) Noise Transfer Function.

are affected by numerical errors which have the effect of increasing the noise floor of about $35\,dB\,V/\sqrt{Hz}$ with respect to the real modulator. This gap reduces as the maximum step size is reduced but clearly the simulation becomes slower and slower. With a maximum step size of $500\,\mathrm{ps}$ (red curve) the simulation gives results compatible with respect to the real case highlighting a noise floor of roughly $-134.6\,dB\,V/\sqrt{Hz}$ ($186\,nV/\sqrt{Hz}$). The circuit was also simulated with a time step of $250\,\mathrm{ps}$ but the simulator ran into convergence issues. The simulation parameters used are summarized in Table II (except for the default ones).

It is worth noting that, given the switched nature of a $\Delta\Sigma$ modulator, roughly $10\,\mathrm{h}$ were needed to simulate $75\,\mathrm{ms}$ with a maximum step size of $500\,\mathrm{ps}$ (red curve in Fig.5).

PSpice TRAN Simulation Parameters	
Maximum step size	500 ps
Run to time (TSTOP)	75 ms
Relative accuracy of V and I (RELTOL)	10^{-4}
Best accuracy of voltages (VNTOL)	100 nV
Best accuracy of currents (ABSTOL)	1 pA
Best accuracy of charges (CHGTOL)	1 fC
Default I/O level for A/D interfaces (DIGIOLVL)	2

TABLE II: Simulation Parameters for DC Analysis

This is an important practical limit for PSpice simulations. As an example, if one more decade is needed for the noise PSD, in the low frequency range, the time required by the simulation would increase by a factor of 10 which is, practically, unacceptable. However for noise floor estimation

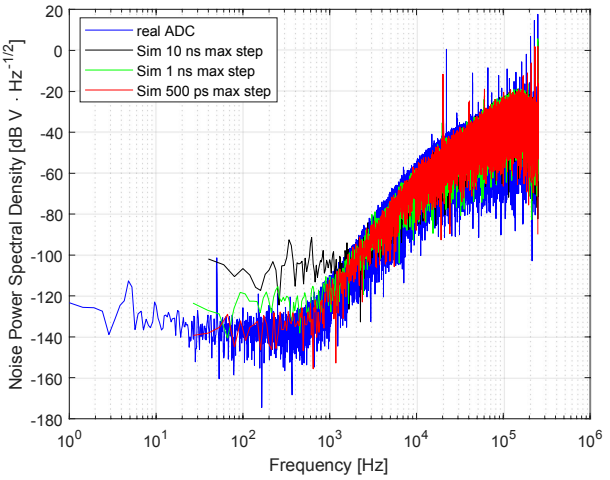


Fig. 5: Noise Power Spectral Density for Different Max Step Size (shorted inputs).

Simulink Idle Tones Simulation Parameters	
Maximum step size	50 ns
Stop time	10 s
Relative tolerance	10^{-6}
Solver	ode23t (mod. stiff/Trapezoidal)

TABLE III: Simulation Parameters for Idle Tones Analysis.

down to some tens of Hz PSpice remains a powerful and accurate simulation tool which allows assessing the impact of different design choices (components update, resistors scaling, etc.).

V. Simulink Model for Idle Tones

Idle tones are known to affect $\Delta\Sigma$ modulators [17]. An idle tone is a repetitive noise pattern generated inside the $\Delta\Sigma$ modulator loop when fed by a DC input. It is known that the frequency of the produced idle tone is directly proportional to the input DC level. In particular:

$$f_i = x \cdot f_s \tag{4}$$

where f_s is the sampling frequency and x is the normalized input with respect to full scale, defined as:

$$x = \begin{cases} 0, & \text{if negative full-scale input} \\ 1, & \text{if positive full-scale input} \end{cases} \tag{5}$$

As an example, when the input of the $\Delta\Sigma$ modulator is very close to 0 V ($x \approx 0.5$), an idle tone at $f_i \approx 250\,\mathrm{kHz}$ is expected to be produced. The 2^{nd} harmonic of this tone will therefore be at $\approx 500\,\mathrm{kHz}$ which, after being sampled at $500\,\mathrm{kS/s}$, will be aliased back very close to DC. In this simulation, the mechanism of idle tones in the DS-22 is studied by means of a simplified Simulink model which has the advantage of being way faster than PSpice. In Table III, the simulation parameters used for this analysis are reported (except for the default ones).

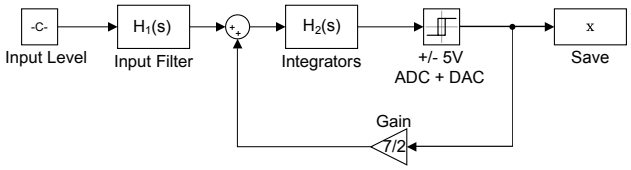


Fig. 6: Simulink Model for Idle Tones Tracking with Negative DC Gain of H_2.

However, the Simulink model does not take into consideration all the noise sources in the PSpice model circuit in Fig.2; in fact, it is built from the transfer functions detailed in equations (2) and (3) and sketched in Fig.6. The results of these simulations are reported in Fig.7. For these simulations, the noise power is considered and depicted (instead of its spectral density) for different input DC levels to correctly estimate the amplitude of the idle tones. As for the simulations in section IV-C the noise floor level is very dependent on the simulation maximum step size which, in these simulations, was 50 ns. Given the low-complexity of the Simulink model compared with the PSpice one, simulating 10 s in a reasonable amount of time (couple of hours) is possible. For each simulation an idle tone (plus its harmonics) is produced at a given frequency. This result was also reproduced with different combinations of the simulation parameters(not reported hereafter). The simulation results showed that, even if the level of the noise floor is strongly dependent on the particular set of parameters, the frequency and amplitude of the idle tones do not change. In the same figure, it is shown that all the peaks belonging to the same order harmonic (highlighted with a star) are aligned on a $60\,\mathrm{dB/dec}$ slope. This means that the amplitude of these tones is shaped by the NTF in the same way of the quantization noise. They should then be negligible in the typical band of interest of some hundreds of Hz, seen the level of attenuation introduced by the NTF in that region.

As it can be observed in Fig. 5, the actual device shows an idle tone at roughly 5 Hz, whose amplitude is well above the noise floor of $\approx -136\,dB\,V/\sqrt{Hz}$ (ADC fed by an input voltage of about 0 V). This cannot be explained by means of the NTF. It is an unmodeled dynamics, probably due to stray capacitive couplings allowing high-frequency idle tones to couple to neighbor lines (cross-talk) and find alternative ways to enter in the signal path, hence, bypassing the NTF and then folding back to base-band after being sampled. However, this is only an hypothesis whose verification outgoes the scope of this work.

VI. Conclusion

In this work, models and method have been presented for the simulation of the DS-22, a high–resolution $\Delta\Sigma$ ADC designed at CERN in operation in the main LHC power converters. PSpice transient simulations are shown to reproduce correctly the switching behavior of the actual device featuring a very–low noise floor of $186\,nV/\sqrt{Hz}$. However, the duration of

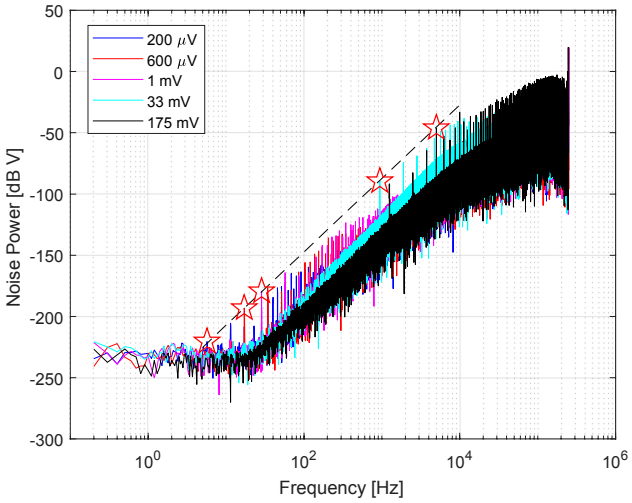


Fig. 7: Noise Power for Different Input Levels.

such simulations is prohibitive especially for studying low frequency effects.

Thus, a simplified PSpice noise model was also proved to reproduce accurately the noise level of the actual device overcoming the duration limitations of the model used for transient simulations. This is very useful for exploring the margins of improvement the DS-22 in terms of components upgrade and replacements due to obsolescence.

For the very low frequency effects, such as the idle tones mechanism for which longer simulations are needed (up to 10 s), a Simulink model was used. This, allowed confirming that the amplitude of such tones should be shaped by the NTF. Thus, no idle tones below few hundreds of Hz (where the noise floor intercepts the NTF) are expected to be visible. However, idle tones have been seen at few Hz with amplitudes well above the noise floor on the real device; thus other unmodeled mechanisms are at play which will be the object of further studies and developments.

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References

[1] R. Schreier, G. C. Temes *et al.*, *Understanding delta-sigma data converters*. IEEE press Piscataway, NJ, 2005, vol. 74.

[2] J.-N. Lin, H.-C. Chu, Z.-Y. Chen, and C.-C. Hung, "A continuous-time delta-sigma modulator with novel data-weighted averaging algorithm for audio application," in *Electron Devices and Solid-State Circuits (EDSSC), 2015 IEEE International Conference on*. IEEE, 2015, pp. 281–284.

[3] L. Bettini, T. Christen, T. Burger, and Q. Huang, "A reconfigurable dt $\Sigma\Delta$ modulator for multi-standard 2g/3g/4g wireless receivers," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 525–536, 2015.

[4] S. Pavan and R. Rajan, "Simplified analysis and simulation of the stf, ntf, and noise in continuous-time $\Sigma\Delta$ modulators," *IEEE Transactions on circuits and systems II: Express briefs*, vol. 61, p. 9, 2014.

[5] M. Joseph and S. Sreelal, "End to end simulation of sigma delta adc," in *Annual International Conference on Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR)*, 2013.

[6] J. Talebzadeh and I. Kale, "Design and simulation of a 3rd-order discrete-time time-interleaved delta-sigma modulator with shared integrators between two paths," in *Proc. Iranian Conf. Electrical Engineering (ICEE)*, May 2017, pp. 197–200.

[7] Z. Zhao, Q. Huang, Q. Peng, and J. Xu, "Performances of front-end electronics based on sigma-delta modulation — a simulation study," in *Proc. IEEE Nuclear Science Symp. and Medical Imaging Conf. (NSS/MIC)*, Oct. 2015, pp. 1–2.

[8] K. Kang and P. Stubberud, "A comparison of continuous time sigma delta modulator simulation methods," in *IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2014.

[9] L. Rossi and O. Brning, *The High Luminosity Large Hadron Collider. The New Machine for Illuminating the Mysteries of Universe*, ser. Advanced Series on Directions in High Energy Physics. World Scientific Publishing Co Pte Ltd, 2015, vol. 24.

[10] G. Apollinari, I. Bejar Alonso, O. Brning, P. Fessia, M. Lamont, L. Rossi, and L. Tavian, "High-Luminosity Large Hadron Collider (HL-LHC). Technical Design Report V.0.1," CERN, CERN Yellow Reports: Monographs, Vol.4/2017, 2017.

[11] J. Pett, "A High Accuracy 22 bit Sigma-Delta Converter for Digital Regulation of Super-conducting Magnet Currents," in *Advanced A/D and D/A Conversion Techniques and their Applications*, 1999.

[12] J. Pickering, "Developing the Sigma-Delta A-D for precision DC&LF metrology," in *IMEKO-TC4*, 2002.

[13] Z. Tan, R. Maurino, R. Adams, and K. Nguyen, "Subtractive dithering technique for delta-sigma modulator," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2017, pp. 1–4.

[14] P. Arpaia, C. Baccigalupi, and M. Martino, "Metrological Characterization of High-Performance Delta-Sigma ADCs: A Case Study of CERN DS-22," in *accepted by I2MTC 2018*, 2018.

[15] J. Candy, "A Use of Double Integration in Sigma Delta Modulation," in *IEEE Transactions on Communications, Vol 33, Issue 3*, 1985.

[16] A. Devices, "AN-283 Sigma-Delta ADCs and DACs," application Note.

[17] F. Rizzo, S. S. Somayajula, D. Zito, R. Saletti, and R. Becker, "Audio Telecom ADC Featuring Click-Free Gain Control Technique, Dithering Insertion, and Idle Tone Shifting," vol. 61, no. 11, pp. 2879–2887, Nov. 2012.