The CENAM Programmable Josephson Voltage Standard

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***Abstract* — A Programmable Josephson Voltage Standard (PJVS) was developed at CENAM, based on a NIST 10 V chip. The bias source and the control software were developed at CENAM. The cryoprobe was modified to increase the bandwidth. In this paper we describe the main features of the standard.**

***Index Term* — Programmable Josephson voltage standard, voltage measurement standards, measurement techniques, measurement uncertainty, precision measurements.**

I. Introduction

The first Programmable Josephson Voltage Standards (PJVS) were developed in the late nighties [1, 2]. These standards can generate accurate and stable DC voltage levels that can be programmed to produce staircase approximations of any waveform. Of particular interest, for AC power and energy applications, is the generation of staircase approximation of 50-60 Hz sine-waves [3, 4]. The frequency of the staircase approximations that can be generated with ppm accuracy in the RMS value is limited to some kHz.

There are several technologies available for the PJVS; the NIST technology, based on SNS (superconductor-normal metal-superconductor) Josephson junctions, which works between 18 GHz and 20 GHz and produces large operating margins; the PTB technology now based on SNS Josephson junctions, which can generates 20 V, works around 70 GHz, and is compatible with the microwave system used for the conventional JVS; and the AIST technology, based on SNS Josephson junctions, which works at 16 GHz.

The bias source is a key element for the development of PJVS applications. It was decided to design and built a bias source to have the possibility of modifying it to obtain the necessary performance for each application. The bias source should be very stable, low noise and fast to cover the general performance for many applications.

In this article the CENAM PJVS is described, including the bias source, the microwave system and the software. Some information about the performance of the standard is given.

II. PJVS DESCRIPTION

The 10 V chip contains two groups of ternary-divided least significant bit sub-arrays with 4374, 1458, 486, 162, 54, 18 and 8 Josephson junctions each, and 15 sub-arrays of 16800 Josephson junctions. If one group of ternary-divided Josephson junctions is biased together, 24 channels are required to bias the entire chip.

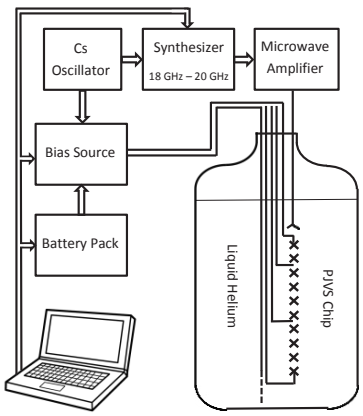

Fig. 1. Block diagram of the PJVS

The standard uses a homemade voltage bias source. The output voltage interval of the bias source is ± 12 V, and the voltage resolution is 0.3 mV. The output current interval is ± 30 mA and the current resolution is 7 μA. The frequency can be adjusted from DC to 10 kHz. The frequency resolution is the number of steps per cycle, multiplied by the master clock resolution (1μHz). Any waveform can be generated having up to 2048 steps per cycle. The short term stability is 10 μV/h and the low frequency noise is 50 μV peak to peak. The bias source has current limiters at the outputs, to protect the PJVS chip. The rise and fall times of step transitions at the source outputs are 20 ns as is shown in Fig. 2.

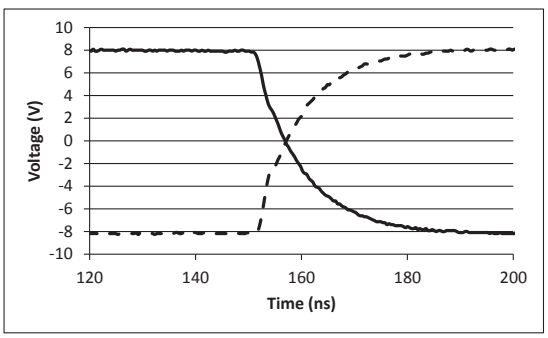

Fig. 2. Rise and fall waveforms of the step transitions, measured at the output of the bias source, without the PJVS chip connected.

To avoid dangerous transients that can be generated when the bias source is switched on and off, a turn on and off sequence was developed. The bias source can be operated on batteries, continuously during 8 hours, or connected to the mains. The battery operation allows the standard to work floated and connected to any instrument, avoiding ground problems and having a small noise level. The bias source is controlled using a laptop by means of isolated USB interfaces.

Control software was developed under Labview platform. The software allows calculating and controlling the voltage levels in each channel, to generate any waveform, considering the chip configuration. By using a nano-voltmeter, the margins of the chip can be measured automatically.

The 10 MHz output of a Cs oscillator is connected as external frequency reference of the microwave synthesizer and the bias source. The synthesizer generates a stable sinusoidal wave, with frequencies up to 20 GHz. This signal is applied to a microwave amplifier that can provide an output power up to 1 W.

The standard uses a cryoprobe made by High Precision Devices. The original cryoprobe wiring was made of magnet wire, but it was changed to increase the bandwidth. Twisted pair and micro-coaxial cable were tested. The bandwidth of the micro-coaxial cable was 2.3 GHz, but the liquid helium consumption was too high. The bandwidth of the twisted pair was 450 MHz, that is high enough, and the liquid helium consumption was not too high. Therefore the twisted pair was retained. The output wires do not have filters to maintain the fast response of the standard.

III. BIAS SOURCE DESCRIPTION

The bias source is composed by 24 programmable voltage sources to be connected to the nodes of the PJVS chip by 50 ohm resistors. The programmable voltage sources are based in a SRAM memory, which stores the binary codes corresponding to the waveform to be generated. The codes are calculated in a laptop and transferred to the memory by using a USB to parallel interface. Once the codes are in the memory, the source operates independently of the laptop in the automatic mode. A circular counter, connected to the memory address pins, scans the memory locations and the binary codes pass to a DAC (digital to analog converter). Between the SRAM and the DAC there is an isolator to avoid interference from the digital part into the analogic circuit. The output voltage is connected to a high frequency amplifier which provides enough current to bias the Josephson junctions. In the automatic operation, when the waveform is generated, the source runs independently of the laptop. The bias source uses a master clock which frequency can be adjusted between 1 mHz and 20.48 MHz.

IV. PJVS PERFORMANCE

In DC applications it is possible to generate very stable voltage levels between -10 V and + 10 V. The step widths are between 0.7 mA and 2 mA. The smallest number of junctions is eight, but by adjusting the microwave frequency, with a 2 mHz resolution, it is possible to have a very high voltage resolution at the output voltage (1pV/10V).

Any waveform can be generated (Fig. 3). The steps quantization in the AC generation was confirmed by reducing the frequency, measuring each step with a DVM and comparing the measurements with the calculated values. The rise time of the step transitions measured at the chip output is about 50 ns.

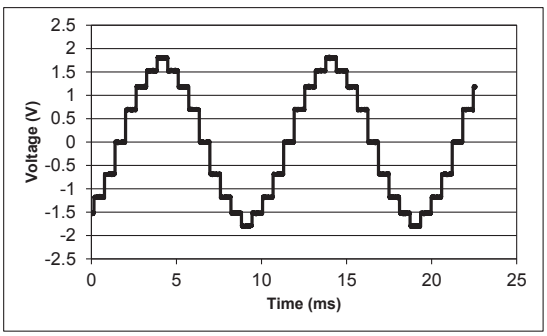

Fig. 3. Measurement of a staircase approximation of a sinusoidal wave, generated with the PJVS, having a frequency of 100 Hz and amplitude of 1.8 V.

V. CONCLUSION

The CENAM PJVS is now in use. In the next months some additional work will be done to optimize its performance. The standard will be used to develop AC, power and impedance applications.

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