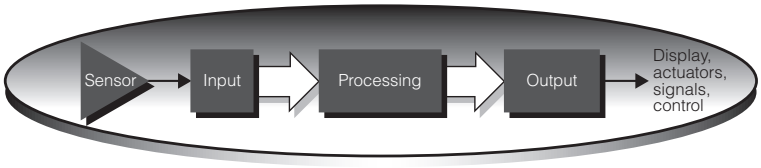

High Accuracy Current Measurement in the Main Power Converters of the Large Hadron Collider: Tutorial 53

Part 53 in a series of tutorials on instrumentation and measurement

Miguel Cerqueira Bastos, Gunnar Fernqvist, Gregory Hudson, John Pett, Andrea Cantone, Francis Power, Alfredo Saab, Björn Halvarsson, and John Pickering

In the Large Hadron Collider (LHC) at CERN, the powering of the main dipole and quadrupole circuits is divided into eight separate powering sub sectors due to the very high magnetic energy stored in these circuits and to protection constraints of the superconducting magnets [1]. As a consequence, individual sector currents must be controlled with very high accuracy in amplitude and time to ensure that the beam of particles sees the same magnetic field in all sectors. This results in a requirement for current tracking between the different sectors of better than ± 5 ppm and short term stability of better than ± 2 ppm [1], at 13 kA currents.

The LHC power converters are current sources employing digital control to ensure a given reference function to the magnet current. The current measurement transducer and the Analog to Digital Converter (ADC) are key elements in achieving the required performance. This tutorial will describe the main aspects of ADC and current transducer design, evaluation and integration in the LHC main power converters.

System Overview

Fig. 1 shows the current measurement and calibration chain of the LHC main power converters and its integration in the control and calibration structure. Each converter is equipped with two 13-kA Direct-Current Current Transformers (DCCTs) and two CERN-designed Delta-Sigma ADCs. The ADCs convert the signal from the DCCTs with a range (0, 10) V – corresponding to (0, 13) kA – into a digital signal used by the digital regulation loop implemented in the power converter controller unit, the Function Generator Controller (FGC).

A complete *in-situ* calibration system including an extremely accurate programmable current source, the CERN DCCT Calibrator (CDC) [7], allows the complete current measurement chain to be calibrated remotely by memorizing digital calibration values in the FGC. These

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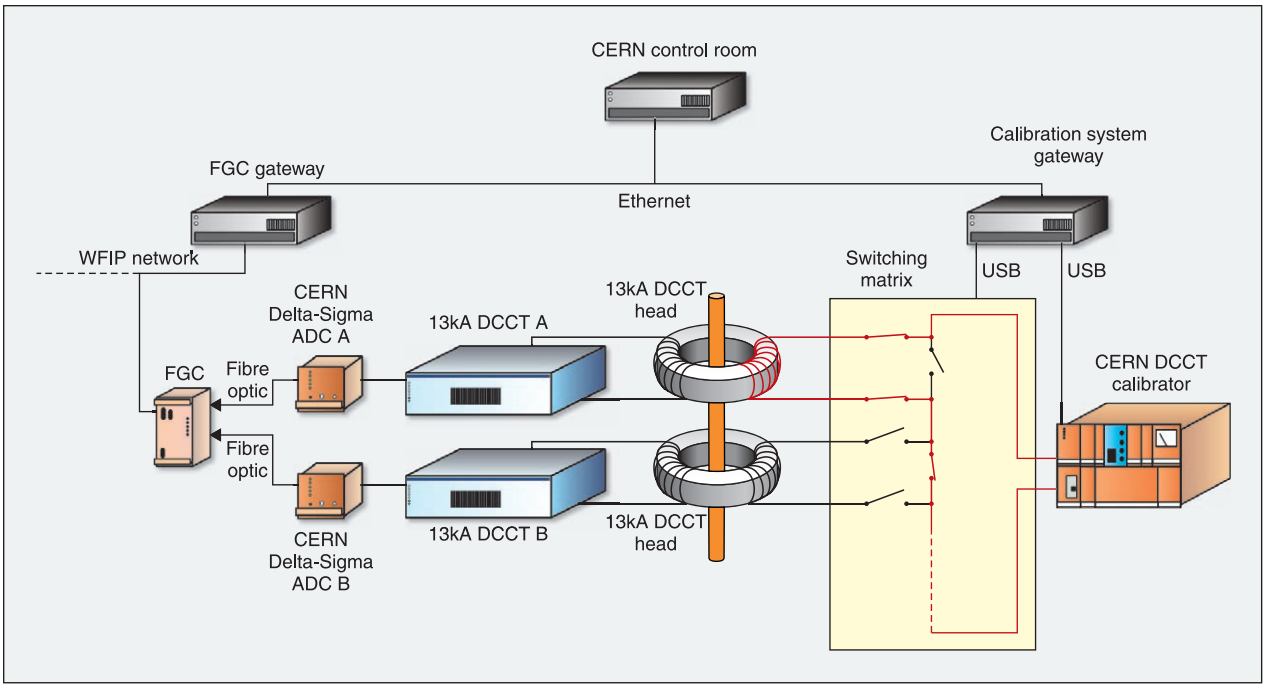

Fig. 1. Current measurement, acquisition, and calibration chain for the LHC main power converters.

correction factors are associated with each individual device through an identification number contained in a chip included in the DCCT and ADC electronics. An image of the calibration data is stored in a central database, and a synchronization scheme ensures that the data in the database remain a faithful image of the FGC data at all times.

DCCT Theory

A DCCT is a magnetic type dc current transducer based on the principle of zero flux and capable of measurement uncertainties on the order of ppm, for currents ranging from some Amperes up to some tens of kA. The DCCT theory is well known and described in detail in [3]. The working principle of a DCCT using a balanced peak detector is illustrated in Fig. 2.

If a voltage output is required, the DCCT compensation current is passed through a current-sense resistor, normally referred to as the DCCT burden resistor, and the resulting voltage is amplified by a precision amplifier stage. The DCCT frequency behavior can be described by three basic modes of operation: low frequency/zero flux dominated by the

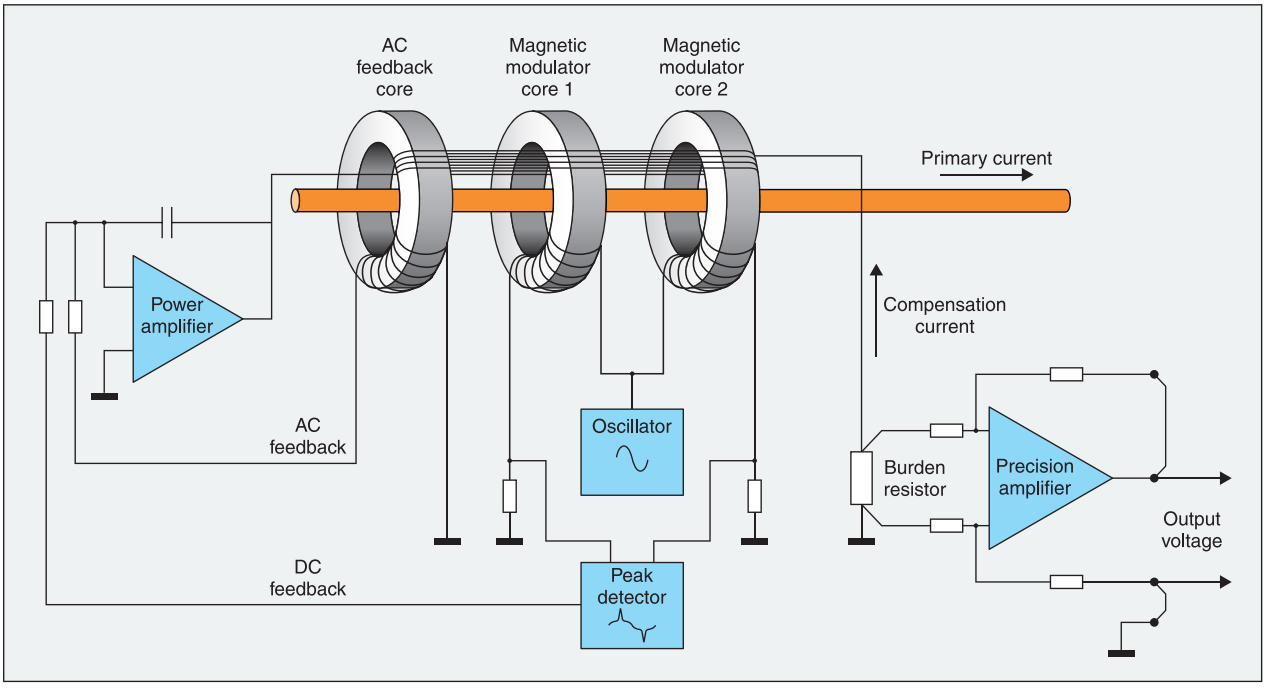

Fig. 2. DCCT working principle (peak detector type).

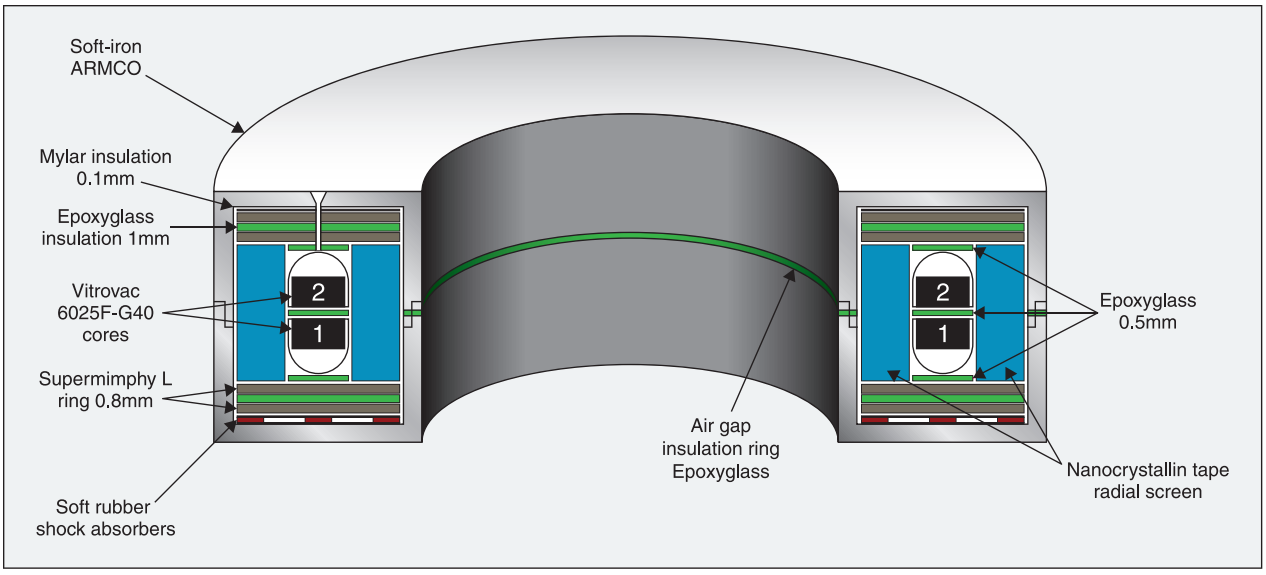

Fig. 3. CERN DCCT calibrator magnetic head cross-section.

magnetic modulator (bandwidth is normally limited to half of the modulation frequency to avoid aliasing [4]), medium frequency/zero flux dominated by the DCCT ac feedback, and high frequency/current transformer mode where the feedback loop is no longer effective and the power amplifier is bypassed, meaning that the DCCT works as a current transformer [3]. The response of the DCCT at higher frequencies can therefore be described using the well-known current transformer equivalent model. Analysis of the model shows that the high frequency performance of the DCCT is limited by leakage inductance and parasitic capacitance of the windings.

DCCT Design Aspects

The main challenges in DCCT design are related to the magnetic head and the current-to-voltage conversion. The magnetic circuit design should aim at increasing sensitivity to the primary magnetic field, while minimizing remanence, noise, and sensitivity to external magnetic fields, as well as sensitivity to head centering and return bus-bar configuration. This involves choosing magnetic materials with very high permeability, high electrical resistivity, low coercivity, and low magnetostriction [4]. Amorphous alloys are among the most widely used magnetic materials. Degradation of permeability with frequency and imperfections in permeability uniformity must also be considered.

The magnetic shielding normally consists of multiple layers of shielding composed of different materials. Its role is to protect the cores from the influence of external fields and from leakage flux resulting from winding distribution asymmetry. Although low coercivity is desirable for all shielding layers, permeability values can be quite different to avoid saturation. A common practice is to have a high-saturation, low-permeability material in the outer layer, such as iron.

An example of head design, used in the CERN DCCT Calibrator, is shown in Fig. 3.

For voltage output DCCTs, additional challenges arise in the choice of burden resistor and design of the amplifier stage. Well-known effects, such as those due to ambient temperature and ageing, can introduce significant errors. Other effects such as humidity, hysteresis under power cycling, and power coefficient of resistance (PCR) [5] must also be considered. PCR reflects the fact that changes in resistance with respect to ambient temperature variations are not the same as those caused by self-heating due to internal power dissipation. In the first case, temperature gradients inside the resistor are driven by heat flow coming from the outside while in the latter case, the heat originates in the resistive element and spreads to the other layers of the resistor resulting in different thermal gradients. This difference can be significant.

DCCTs for the LHC Main Power Converters

From the early days of the LHC design, it was realized that if the DCCTs had an extra winding with enough turns, an accurate current of a few Amps could be used to simulate 13 kA primary current, providing an easy *in-situ* verification and calibration method. The basic assumption is that 13 kA in 1 turn (13 kAT) is equal to 5 A in 2600 turns (13 kAT) [5]. Following this idea, a 2600 turn *calibration* winding, designed for 5 A nominal current, was added to the DCCTs.

While long-term stability is affected by factors such as component ageing, humidity absorption, and stress relaxation and can be improved by calibration, short-term stability depends mostly on 1/f noise and thermal effects. The choice of burden resistor is, therefore, of utmost importance. The CERN 13 kA DCCTs use a four-wire Zeranin wire resistor, specially processed and heat-treated to improve stability, achieving better than 1 ppm/ °C and 1 ppm/W. Forced ventilation ensures the necessary airflow to limit temperature variations to a minimum, avoiding air turbulence, which can be the cause of increased noise. In addition, the DCCT electronics are installed

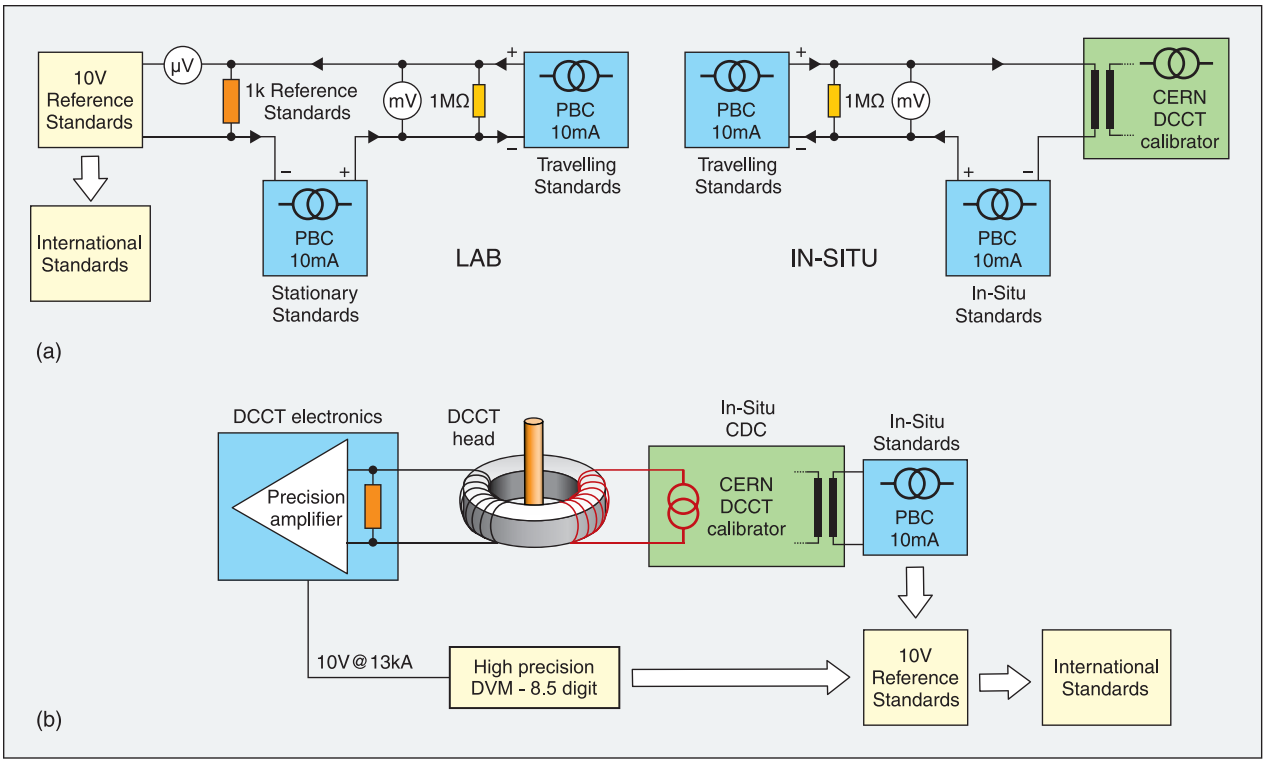

Fig. 4. PBC calibration transfer, DCCT calibration and reference DCCT test method.

in dedicated air-conditioned racks where temperature is kept constant to within ± 1 °C.

DCCT Testing and Calibration

A defining aspect of the LHC DCCTs test and calibration infrastructure is the fact that it works in current rather than in voltage. This aims at taking advantage of the better noise immunity of current signals and the fact that DCCT current outputs are extremely accurate.

Following this strategy, the LHC DCCTs test and calibration infrastructure includes a 10 mA transportable current reference (PBC), designed for CERN and traceable to national standards via 1 kΩ and 10 V standards [6], a 20 kA DCCT test bed with two specially built reference DCCTs, tracking each other to 0.2 ppm at 20kA nominal current [7], [8], and the CDC: a 0 to ± 10 A programmable reference current source with sub ppm resolution and ppm uncertainty, designed at CERN [2].

Fig. 4a shows how reference current traceability is achieved: primary 10 mA is calibrated using 10 V and 1 kΩ standards. Calibration transfer to a travelling 10 mA reference is achieved by connecting it in series with the stationary reference and concurrently with the standard resistor. The use of the reverse connection (back-to-back method) with a high resistor value to measure the error current between two PBCs has the advantage of producing voltages in the mV range for sub ppm (nA) current errors, avoiding problems with thermal EMFs and contact resistances. The 10 mA standard in the CDC can be calibrated using the same method, with similar uncertainty. Fig. 4b depicts the *in-situ* calibration of a DCCT. The CDC is used to inject a reference current of 5 A into the DCCT calibration winding. The output error of the DCCT is measured with a calibrated precision DVM. As the CDC is itself based on a traceable 10 mA reference, the resulting measurement is fully traceable to international standards.

DCCT Field Results

Table 1 shows the LHC 13 kA DCCTs' long term drift results for the first three years of LHC operation (2010-2012) for 48 installed units. The requirement for one-year stability is +/−50 ppm.

The CERN Delta-Sigma ADC

Delta-Sigma (DS) ADC theory is widely covered in the literature, and this tutorial assumes the reader is familiar with the concepts of oversampling, decimation, noise shaping, and digital filtering. This section will only briefly describe the application of these concepts in the case of the CERN 22-bit DS ADC.

A third-order integrator and a fourth-order digital filter based on cascaded SINC filters were selected for their capability of delivering the required performance with limited

Table 1 – DCCT yearly drifts

	Average	Standard deviation	Maximum
Offset	0.3 ppm	0.4 ppm	0.9 ppm
Gain	2.2 ppm	1.5 ppm	5.2 ppm

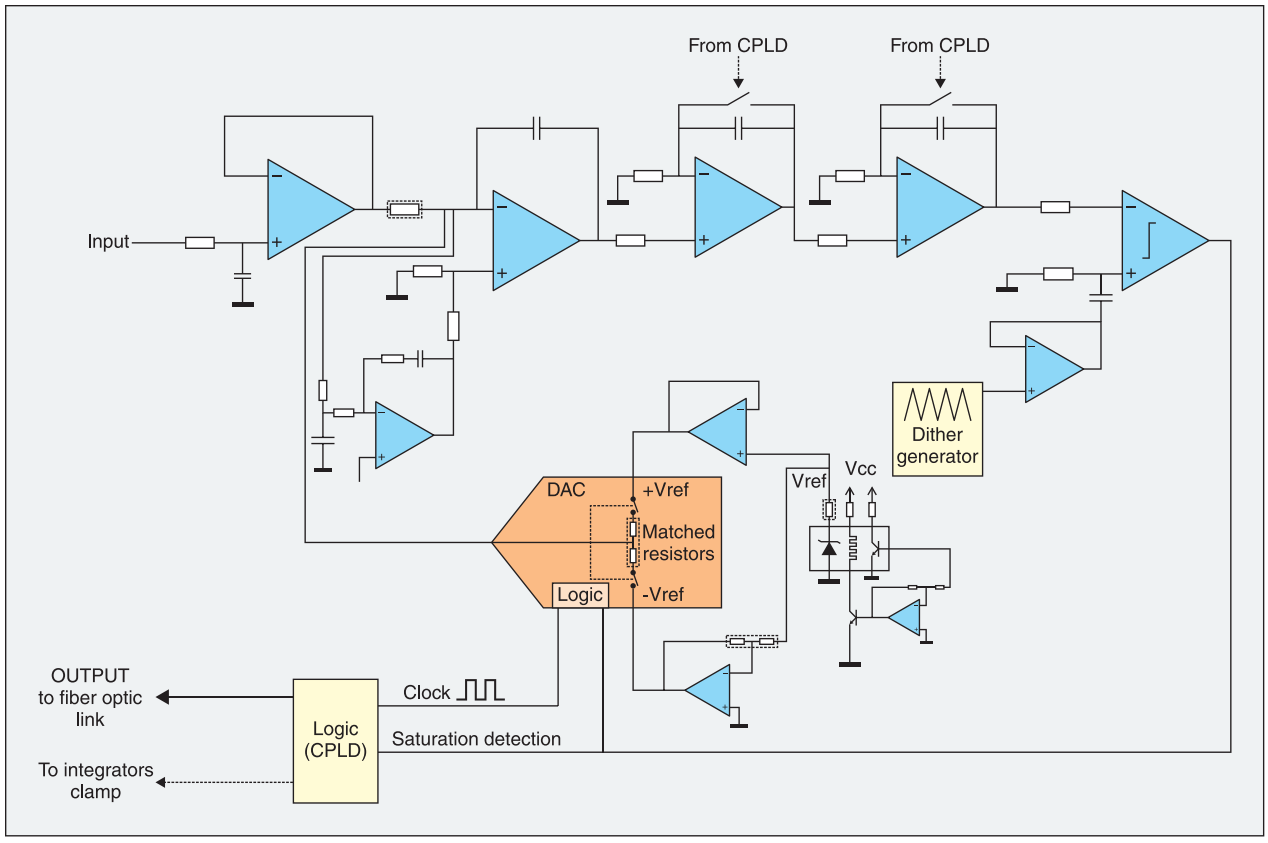

Fig. 5. CERN DS ADC implementation – simplified schematics.

complexity. The system clock runs at 500 kHz. The digital filter is composed of two interleaved filters displaced by 500 samples, each with an output rate of 500 S/s, resulting in a complete conversion rate of 1 kS/s [9]. The oversampling ratio is 500. As it is known, oversampling has the effect of spreading the total quantization noise power over a wide frequency range. As quantization noise power has a fixed value [10], the spreading results in reduced noise in the band of interest. Further reduction in quantization noise is given by the noise shaping action of the integrators. The theoretical total noise reduction in rms value of quantization noise for a third-order integrator with an oversampling ratio of 500 would amount to 167 dB! Unfortunately in real applications there are other factors and noise sources that limit SNR and resolution. In practice, the resolution obtained with the CERN design was shown to be just about 22-bit for frequencies below 50 Hz.

Some of the limiting factors are related to the non-linear nature of the quantizer. In particular, quantizer overload (and therefore instability) can occur even if the input amplitude is kept within the quantizer input range. In the case of the CERN DS ADC, this motivated the introduction of an integrator clamping mechanism. In fact, the second and third integrator stages in the CERN DS are both configured as non-inverting integrators and can be clamped in case of saturation, thus giving unity gain from input to output of the integrator pair and ensuring an *always stable* first-order form until the overload is removed.

Nonlinearity of the quantizer is also responsible for limit cycles, which refer to the appearance of repeating sequences in the output bit stream for some dc inputs. Idle tones refer to the appearance of overtones in the output spectrum, seen as clearly distinguishable frequency lines above the noise floor which are not present in the input signal. A distinct characteristic of idle tones is that their frequency depends on the amplitude of the dc input [11]. A known technique to suppress limit cycles and idle tones is to add a dither signal to the input of the quantizer in the form of a noise source. This ensures that the signal at the input of the quantizer frequently crosses the decision threshold thus randomizing quantization noise and ensuring it is uncorrelated with the input. In the case of the CERN DS, a 480 kHz triangular wave is used for dithering.

ADC Design Aspects

Some of the key aspects considered in the CERN DS ADC development were [12]: minimization of output noise, in particular limit cycles and idle tones; minimization of component drift and temperature dependency; easy calibration and immunity to EMI. Fig. 5 shows a simplified schematic of the CERN DS implementation.

Some of the main blocks in Fig. 5 are described below:

- The ADC high-input impedance buffer amplifier is preceded by a two-pole anti-alias filter ensuring negligible amplitude of aliased components from input signals at 500 kHz ± 500 Hz.
- A chopper stabilized amplifier is added in parallel to the first integrator to decrease offset drift. The key design point is to roll off the gain of the chopper amplifier before

Table 2 – CERN DS ADC yearly drifts			
	Average	Standard deviation	Maximum
Offset	1.3 ppm	1.2 ppm	3.7 ppm
Gain	2.0 ppm	0.6 ppm	4.2 ppm

the cross frequency at which its noise becomes higher than the noise of the main amplifier.

- The basic precision-voltage-reference design is based on the LTZ1000A buried zener and uses a modified Spreadbury circuit [13]. Before installation, the LTZ goes through a *burn-in* process to remove initial zener drift. Temperature stabilization is provided by a local control loop using a Peltier element to keep the temperature of an aluminum block containing the LTZ to a stable 25 ºC.
- The reference voltage is switched by a set of precision switches controlled by the output of the comparator. The 1-bit DAC circuit is thermally connected to the temperature controlled block containing the zener reference.

Digital Filter Design

The 1-bit stream from the CERN DS modulator is transmitted via a fiber optic link from the ADC to the power converter's Function Generator Controller (FGC). In the FGC, an FPGA implements the digital filter used to produce the 22-bit effective resolution output from the 1-bit stream. The basic design uses two interleaved, fourth order FIR filters, each composed by four cascaded windowed SINC filters. The length of each filter is 1000, which at a rate of 500 kS/s produces an output each 2 ms. The two filters are displaced by 500 samples in order to produce an output rate of 1 kS/s. The digital filter is carefully designed to provide attenuation of the system's idle tones. The CERN DS ADC idle tones were found to be aliased replicas of real idle tones at multiples of the 20 kHz beating frequency between the dither (480 kHz) and the sampling (500 kHz).

EMC and Integration Aspects

The whole of the CERN DS modulator circuit is floating with respect to ground and contained within a guard box. The guard box is connected to the DCCT local ground via the input cable shielding. This eliminates capacitive common mode coupling between the signal wires and the local ADC ground, resulting in a common-mode rejection ratio greater than 150 dB at 50 Hz. This has been shown to provide > 2.5 kV burst immunity. The CERN DS ADCs are installed in the same EMC, temperature controlled racks as the DCCTs. Transmission of the signal to the converter electronics is done via optical fiber.

ADC Field Results

Table 2 shows the CERN DS ADCs long term drift results for the first three years of LHC operation (2010-2012) for 80 installed units. The requirement for one-year stability is ±50 ppm.

The CERN DCCT Calibrator

The CDC is a 0 to ±10 A, 24-bit programmable reference current source with ppm level uncertainty, designed at CERN [7]. The working principle of the CDC is depicted in Fig. 6.

The heart of the system is the toroidal core-assembly, which resembles a classic DCCT but is used to multiply, rather than

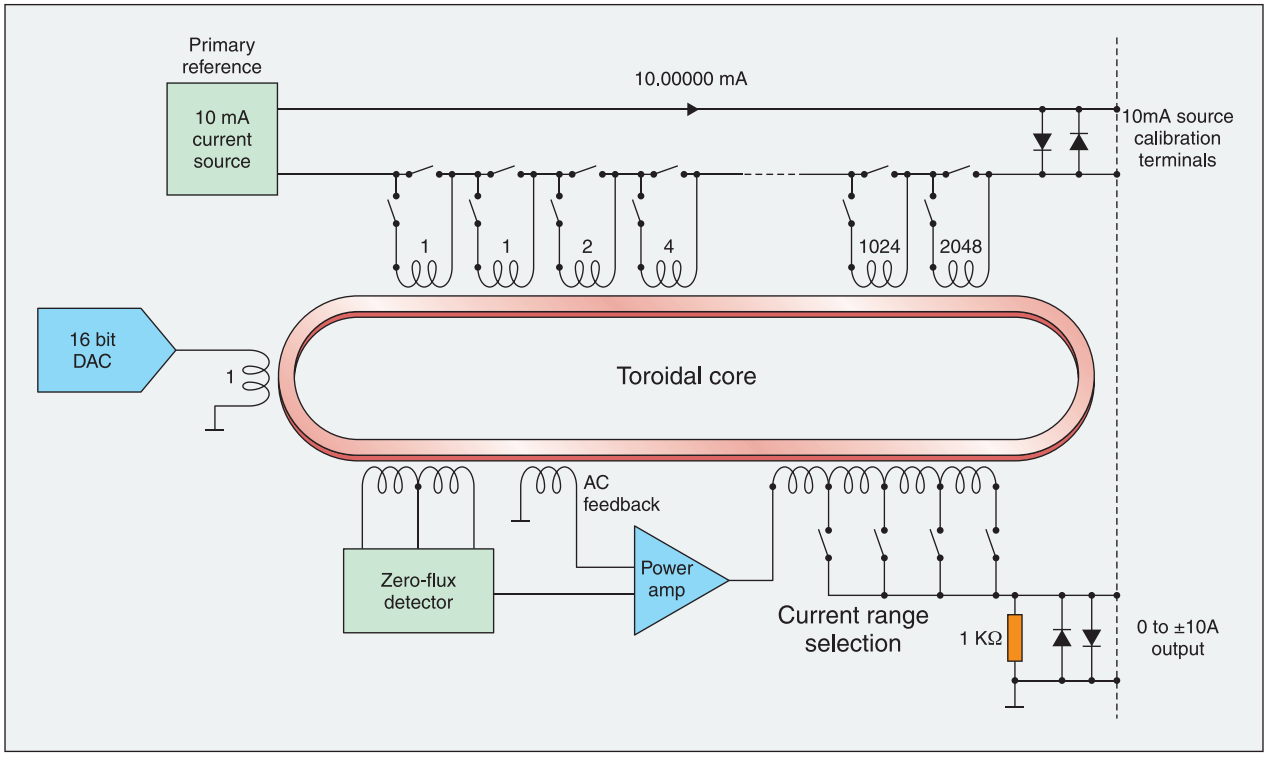

Fig. 6. CERN DCCT Calibrator working principle.

divide, the primary current. The CDC toroidal core assembly consists of two matched amorphous cores shielded by a nanocrystalline radial assembly with mumetal end caps, all enclosed within a thick soft-iron case, as Fig. 3 shows. The primary current is provided by a PBC, which is switched into 12 primary core windings with a binary increase in the number of turns. This gives 12 bits of resolution with the Least Significant Bit being 10 mAT. An increase in resolution is obtained by producing *fractional turns*: a transconductance amplifier controlled by a 16-bit DAC is used to drive a (0,10) mA current into an additional single turn winding. This gives about 12 bits effective extra resolution setting the CDC resolution to about 24 bits.

Conclusions

The LHC current measurement chain measures multi kA currents with unprecedented accuracy. The requirements for the LHC stimulated improvements in dc current measurement and led to the development of new, unique, and high performance measurement and calibration instruments.

Acknowledgments

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ERRATUM

In the December 2014 issue of the *IEEE Instrumentation and Measurement Magazine*, the tutorial by Charna R. Parkey and Wasfy B. Mikhael, "Time Interleaved Analog to Digital Converters: Tutorial 44," was numbered incorrectly on pg. 2, and pg. 42. It should appear as "Tutorial 45."

"Time Interleaved Analog to Digital Converters: Tutorial 45"

We apologize for any inconvenience this may have caused.
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