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A Zener-Based Voltage Reference Design Compensated Using a ΔV_{BE} Stack

Viorel Bucur[1,2], Gabriel Banarie[1,2], Stefan Marinca[2], Mircea Bodea[2]
[1] Analog Devices International, Limerick, Ireland
[2] SD-ETTI, UPB, Bucharest, Romania
viorel.bucur@analog.com, gabriel.banarie@analog.com, marinca.stefan@gmail.com, mirceabodea@yahoo.com

***Abstract*—Two temperature insensitive voltage reference types are widely used today, namely buried Zener and bandgap voltage. Reference voltages based on buried Zener diodes are less sensitive to stress and have lower Long Term Drift (LTD) (approx. 3ppm/1kh), but require a minimum supply voltage of at least 6.5V. Bandgap-type voltage references can operate off supply voltages as low as 1V. However, they have larger LTD compared to buried Zener type references (typically <30ppm/1kh). Further enhancements to the architectures presented in [1] and [2] are discussed in this paper. By using a high performance monolithic deep buried Zener and replacing the embedded one, further performance enhancements in the form of lower Re-Flow drift, reduced LTD , better noise and improved linearity characteristics are obtained. Maintaining the overall circuit performance achieved in [1] and [2] of *TC* approx. 1.5ppm/°C, and max non-linearity better than ~1mV over the full temperature range from -40 to 125°C are two critical requirements.**

***Keywords*—Zener; PTAT; Charge Pump; Ripple; Embedded Reference, ΔV_{BE}, Co-packaging, Stack-die**

I. Introduction

At the heart of our architecture resides the Zener diode as Proportional to Absolute Temperature (*PTAT*) [3] voltage generator. The performance associated with this device, will ultimately decide the overall specifications and the figure of merit of the new proposed architecture. Proof of concept and functionality were initially required for the new proposed compensation technique named *DeltaV_{be}* [4]. As the Zener diode was already available as a supported device in the selected process, it was the obvious choice at the initial development stage. Unfortunately, the overall characteristics of the Zener diode itself, developed initially for ESD Clamping protection didn't provide us with the state of art status performance required as per Table I.

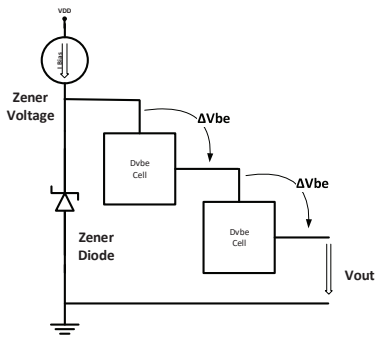

Fig. 1. New proposed block diagram

We are therefore proposing a family of related architectures that will provide the required figure of merit associated with each variant Zener_TC1 to TC4 as presented in Table I.

II. Re-flow and Hysteresis Zener_TC1 Silicon Drift Performance

Silicon chip parameters are impacted differently by package induced stress, depending of the type of package the die was packaged into [5]. Contributors to the Long Term Drift characteristic of the chip are thermal induced stress created by temperature variation at PCB soldering stage, temperature cycling, and humidity variation to mention only the main contributors [6]. The Pre and Post Re-Flow tests are used to mimic the thermal profile of the Printed Circuit Board soldering procedure [7]. Minimal output voltage differences were observed between packaged die, prior and post Re-flow test measured from -40 to 125°C on the tester as shown in Fig. 2, furthermore confirming the reduced package stress influence of the new proposed architecture. On closer inspection and upon calculation the ~1mv drift at 5V Zener Voltage will yield a ~200ppm drift. Even though not the worst soldering induced drift presented in Table I, the relatively large value is one parameter that will require further attention in order to increase the overall architecture performance. The initial silicon test-chip Zener_TC1 developed in [1], did not have accessible test points in order to determine the individual functional blocks contribution to the overall Re-Flow and hysteresis drift. Identifying the main drift contributor was possible by careful design and layout techniques implemented in the next test-chip Zener_TC2 [2]. Each bonding pad, Pad1 to Pad7 was connected to the PCB by individual bond wires as presented in Fig. 3.

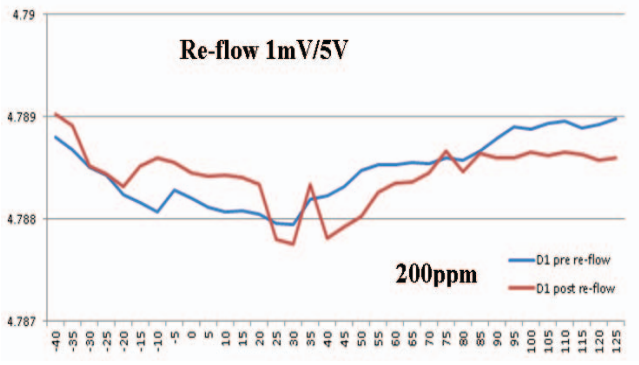

Fig. 2. Pre and Post Re-Flow test for Zener_TC1 reference from -40 to 125°

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TABLE I.
STATE OF ART PERFORMANCE FOR DIFFERENT VOLTAGE REFERENCE IC ARCHITECTURES

Part ID	Supply Requirements	Vout (Volts)	I quiescent (mA)	Tempco typ (ppm/DegC)	Post-reflow drift ppm	Noise uVpp 0.1-10Hz	Initial Accuracy	Reference Principle
Non-heated Voltage reference								
ISL60002	2.7 to 5.5	1 to 3.3	0.0009	20	100 to 1k	11.5	±0.04%	Floating Gate Analog
ISL21090	7 to 36	1 to 7.5	1.28	7	100 to 1k	0.76	±0.02%	Bandgap + Trim
REF102	11.6 to 36	10	1.4	2.5	100+	5	±0.025%	Buried Zener + Trim
LM723	9.5 to 40	2 to 37	1.5	150	NA	86	NA	Buried Zener + Compensation
LTC6655	1.75 to 13.2	1.2 to 5	7	2	100+	0.25	0.03%	Bandgap
LT1027A	8 to 40	5	3.1	2	100+	0.6	±0.02%	Buried Zener
ADR440	3 to 18	2 to 5	3.75	3	NA	0.49	±0.05%	LDO XFET
ADR45XX	3 to 18	2 to 5	0.95	3	100+	0.5	±0.02%	Bandgap
AD586	7 to 35	5	2	2	NA	1 to 4	±0.04%	Buried Zener + Trim
MAX6325	2 to 5	2 to 5	2.7	1	NA	0.6	±0.04%	Buried Zener
MAX6126	2.7 to 12.6	2.048	0.55	3	NA	0.63	±0.02%	Bandgap
LM4140	1.8 to 5.5	1 to 4	0.32	3	NA	2.15	±0.1%	Bandgap +EEPROM DACs
Zener_TC1	6.5	4.5	0.1	<3	~200	40	TBD	Zener + Delta Vbe
Zener_TC2	3	4.5	0.4	<3	~200	TBD	TBD	Zener + Delta Vbe
Zener_TC3	7.5	5.5	0.1	<4	~50	~20	TBD	Buried Zener + Delta Vbe
Zener_TC4	7.5	5.5	0.6	<2	~50	~4	TBD	Buried Zener + Delta Vbe
Heated Voltage reference								
LTZ1000	10 to 35	7.2	300+	3	NA	0.2	4%	Buried Zener + PCB
LM199	9 to 40	6.95V	450+	5+	NA	7 to 20	2%	Buried Zener +PCB

TBD – To be decided
NA – Not available

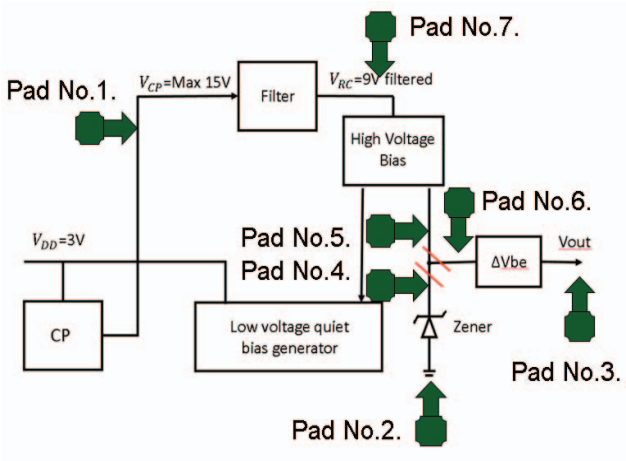

Fig. 3. Block diagram details for Zener_TC2 proposed architecture

We were able to separate the functional blocks of the design and perform individual measurements that enable us to analyse the different components contribution to the overall Re-Flow and hysteresis drift. Silicon measurements were performed on plastic LFCSP packaged Zener_TC2 test chip for 30 random devices. Re-Flow and thermal hysteresis silicon measured values are presented in Fig. 4. From the measured data we were able to calculate the mean distribution of 138uV and a standard deviation of σ = 173uV for the uncompensated Zener diode and respectively a mean distribution of 160uV and a standard deviation σ = 150uV for the Zener post compensation as presented in Table II.

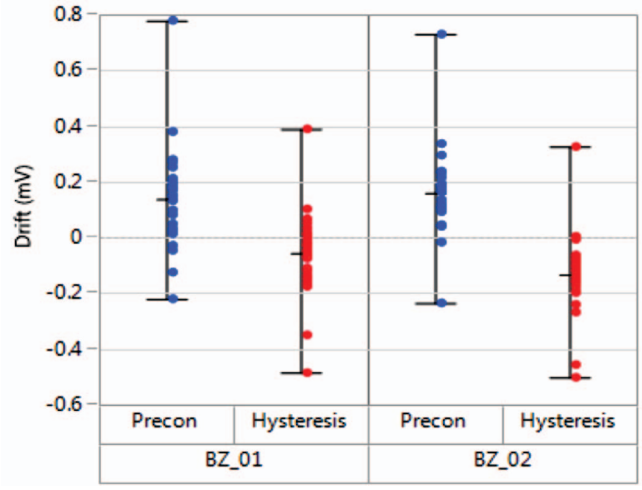

Fig. 4. Re-Flow and hysteresis drift Zener only and compensated Zener

TABLE II.
ZENER ONLY & COMPENSATED ZENER DRIFT MEASUREMENTS (30 PARTS)

	Voltage Delte Vbe (mV)				
Voltage Type	Mean	StdDev	Min	Max	Range
Zener only	0.1384	0.1732	-0.2319	0.7794	0.999
Vref Compensated	0.1606	0.1507	-0.2346	0.7303	0.965

We were also able to measure the overall contribution of the $DeltaV_{be}$ compensation cell in the Re-Flow and hysteresis drift. $DeltaV_{be}$ drift contribution based on the same sample of 30 random devices is presented in Fig. 5. From the measurements,

we were able to calculate a mean distribution of 22uV and a standard deviation of σ = 5uV. Based on these measurements we can conclude that a large proportion of the overall Re-Flow and hysteresis drift can be attributed to the Zener diode itself and a small proportion can be actually associated with the *DeltaV*$_{be}$ compensation circuit.

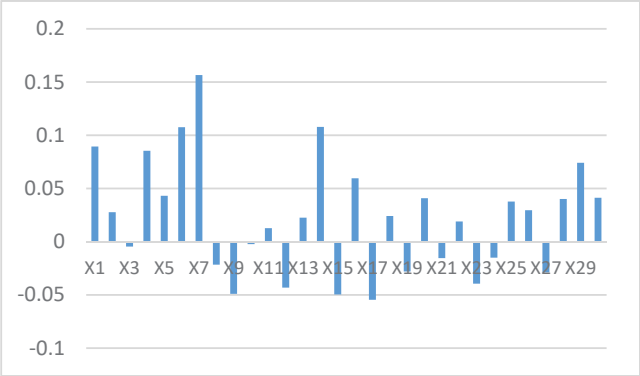

Fig. 5. DeltaVbe only Re-flow and hysteresis drift in mV per device

III. Noise (Zener_TC1 Silicon Measurements)

As expected, the overall noise performance of the initial proposed circuit [1] could not be classified as state of art. This was part due to the low current utilized to bias the Zener Diode [8] and part to the Zener diode itself native available in the 0.6µm BiCMOS 16V HV process. Flicker noise measurements were performed on 5 parts with 2 different packages, PLCC and LFCSP to establish a base line for the noise circuit performance. The average flicker noise or 1/f noise performance for the two used packages for Zener_TC1 and Zener_TC2 was 22.84uVpp for the PLCC package and 34.68uVpp for the LFCSP respectively as presented in Table III. It is apparent from the measurements that the overall circuit noise performance will need to be enhanced [8] to be in line with the different figure of merit voltage reference architectures presented in Table I.

TABLE III.
Noise measurements for Zener_TC1 and Zener_TC2

Diodes	D1	D2	D3	D4	D5	Average (uVp-p)
Output Voltage Noise (uVp-p)						
PLCC Package	39.36	34.52	48.46	20.46	22.84	33.13
LFCSP Package	40.22	35.06	58.2	39.88	34.68	41.61

IV. New Architecture Approach

Based on the silicon measurements performed on Zener_TC2, we concluded that the limiting factor in the overall circuit performance from the Re-Flow and hysteresis drift, noise and nonlinearity point of view, is the embedded Zener diode itself. It had become apparent, based on measurements performed, that as attractive as monolithic single die solution initially was for its advantages in reduced cost, simplicity and good performance it cannot provide the high performance and optimal figure of merit required.

The single chip solution has its advantages as earlier stated and can still be suitable for certain applications. As we are requiring state of art overall performance, we are left with only one available solution, co-packaging a high performance Zener Diode as per Fig.6., manufactured in a suitable technology node, i.e. Analog Devices, Inc. proprietary 10um BIPOLAR technology node and maintaining the *DeltaV*$_{be}$ compensation cells and rest of the support circuit on the same high performance Analog Devices, Inc. proprietary 0.6µm BiCMOS 16V HV process as used for Zener_TC1. This solution provides the best of both worlds approach by merging a deep buried Zener performance with a new compensation temperature technique provided by the *DeltaV*$_{be}$ circuit [1].

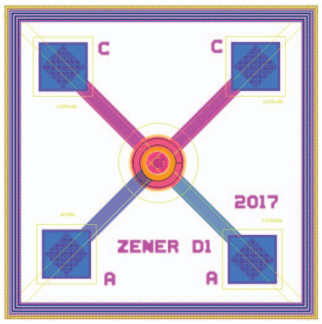

Fig. 6. Deep buried Zener diode implemented on a 10um Bipolar technology

V. New Co-packaged High Performance Solution

As stated previously, we are proposing a family of related architectures with enhancements and features such as:

- Zener_TC1: Fully embedded solution [1] with specifications per Table I.
- Zener_TC2: Fully embedded solution with a front-end Charge Pump [2] to reduce the power supply requirements with specifications per Table I.
- Zener_TC3: Co-packaged solution replacing the embedded Zener with a high performance deep buried Zener diode with specifications per Table I.
- Zener_TC4: Co-packaged solution with a front-end Charge Pump [2] to reduce the power supply requirements with specifications per Table I.

Furthermore to [1] and [2], now that we have available a high performance Zener diode we can explore a bias current increase from the initial 5uA used in [1]. We are able to generate onboard bias currents for low 5uA, medium 50uA and high 500uA options. The new active region of the new Zener diode is significantly larger when compared to the embedded one from Zener_TC1. This area increase should provide an improvement in flicker noise reduction in line with the theoretical values [9]. The new high performance buried Zener diode should achieve improved LTD and TC [10] and as a bonus of operation at higher bias currents, we should achieve a better temperature dependent nonlinearity as per [11]. We were able to simulate the nonlinearity vs bias current associated with the new buried Zener diode. The simulation results showed a good correlation with the Zener theoretical results [11] and are presented in Fig. 7.

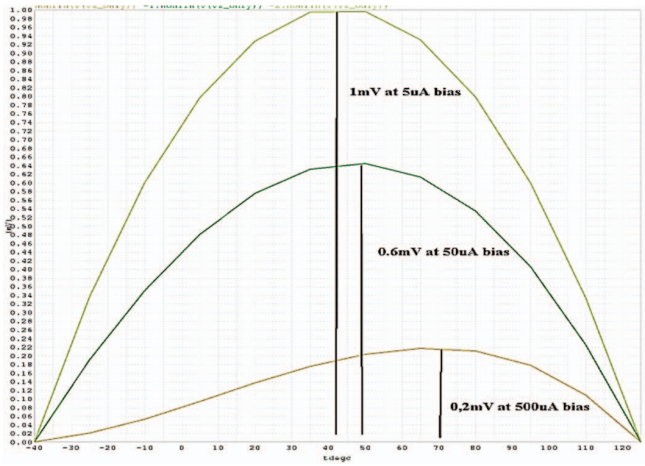

Fig. 7. Temperature nonlinearity dependency at different bias currents

VI. New Co-packaged Measured Performance

As we had all the silicon building blocks needed already manufactured and available from Zener_TC2 test chip, we were able to implement the new Zener_TC3 without any technical difficulties. We were able to co-package the 2 silicon die, the new deep buried Zener and the *DeltaV*$_{be}$ plus the adjacent circuits in a plastic package Shrink Small Outline 150mil body QSOP as per Fig. 8 in a very short turnaround time.

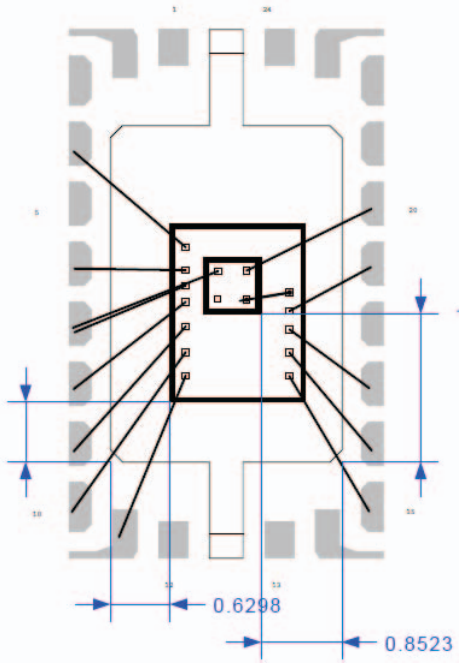

Fig. 8. Co-packaged die details for 150mil body QSOP

Measurements for Zener_TC3 compensated *Vref* were performed at 25 DegC for 100 random samples post optimal trim. A histogram associated with these measurements is presented in Fig. 9. Measurements for Zener_TC3 TC were performed from -40 to 125°C without gain calibration. Based on 50 samples measured in oil bath, we were able to plot the compensated Zener Vout vs temperature as per Fig. 10.

Using the industry standard box method for calculation the temperature coefficients (TC), we were able to determine the Zener_TC3 min-max TC of 1.37 - 3.51ppm. TC result performance histogram is presented in Fig. 11. Initial Re-Flow silicon measurements were performed on 30 samples of the Zener_TC3. Drift histogram associated is presented in Fig. 12. A reduced drift was observed vs Zener_TC1 due to the new high performance buried Zener diode used in Zener_TC3.

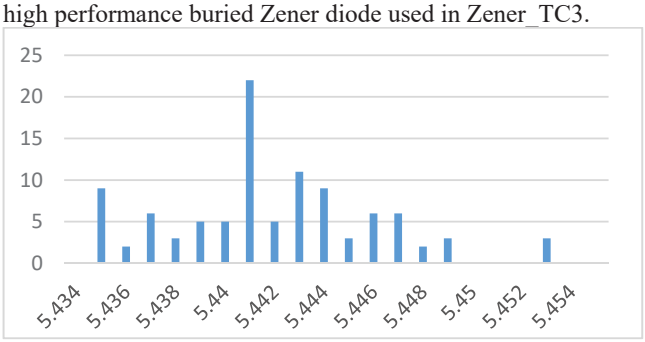

Fig. 9. Standard deviation at 25°C of 4.18mVwith a mean value of 5.44V

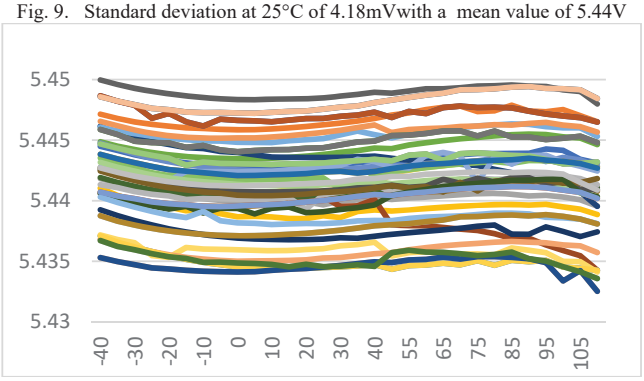

Fig. 10. Reference voltage temperature dependancy from -40 to 125°C

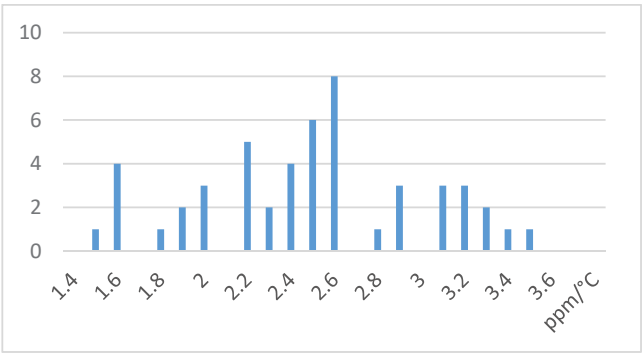

Fig. 11. TC Histogram based in 50 random samples from -40 to 125°C

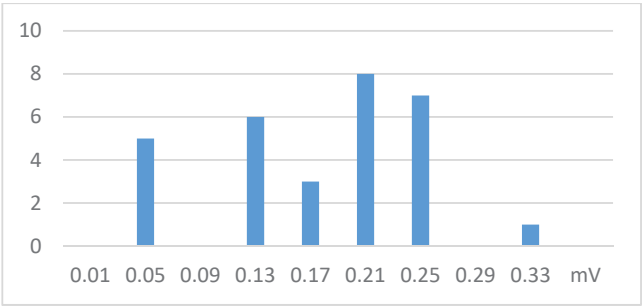

Fig. 12. Measured compensated Zener Vref Re-Flow drift for Zener_TC3

This measured drift represent a reduction of more than 80% when compared with the initial embedded Zener_TC1 original proposed design [1].

VII. Conclusion

We are proposing a family of non-heated Zener based voltage reference architectures featuring the same temperature compensation method $DeltaV_{be}$ [1]. Performance and figure of merit associated with each variant Zener_TC1 to TC4 are presented in Table I.

The main advantages over the existing Zener references are:

- Low TC with non-heated silicon with min-max TC of 1.37 - 3.51ppm for 50 random sample parts.
- Temperature compensation circuit is based on current ratios of BJT area which is less susceptible to drift.
- Simple, flexible & effective trimming circuit.
- Small dispersion values and predictable trim codes.
- Charge Pump front end for reduced supply requirements (Min 2.7V).
- High performance Zener Co-Packaged solution for reduced ReFlow (<50ppm) and improved LTD.
- Flexible Zener bias currents setup, (Low 5uA/Med 50uA/High500uA) for increased silicon performance.
- Small silicon footprint of 0.9*sqmm* for Zener_TC1 and 2.4*sqmm* the Zener_TC2 respectively.

Current indicators based on preliminary silicon results show improved performance for the new proposed architecture versus classical Zener reference voltages designs. The proposed architecture can provide best of both worlds solution: Low power supply requirements specific of the bandgap voltage type references and extremely low LTD specific of the buried Zener type references.

Acknowledgments

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