

# Development of a PJVS Based Primary AC Power Standard

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**Abstract** — This paper describes the development of a primary single-phase sampling ac power standard, which uses a programmable Josephson voltage standard (PJVS) in its core. Magnetic transducers are used to scale down to low levels the ac signals to be compared with the PJVS by digital sampling. Independent digital adaptive regulators in form of algorithms in a control software guarantee stable and accurate phase alignment of the ac signals up to some nano radian.

**Index Terms** — Adaptive signal processing, digital signal processing, electronic circuits, Josephson effect, precision power measurements, signal analysis.

## I. INTRODUCTION

In recent years, many National Metrology Institutes (NMIs) endeavored efforts towards the development of ac power standards based on quantum standards [1]-[3]. The PTB (Germany) system calibrates the digitizer by direct measurements against a PJVS. The corrections so obtained are then applied on sampled data of the ac signals at the output of magnetic transducers. The NRC (Canada) system employs a single PJVS to calibrate the ac voltage over a shunt (for current measurement with a current-comparator-to-voltage converter - IVC) and later compares it with the voltage replica at the secondary of an inductive voltage divider (IVD). The NIST (USA) system [3] employs two PJVS generators working with voltage and current amplifiers to generate the ac quantities for the device under test (DUT) and scale them down (with an IVD and an IVC) to be compared with each PJVS.

Some years ago, we developed the technology to synchronize and phase align signals to a very high precision and accuracy with digital regulation. This lead to the development of an original PJVS based ac voltage calibration system. Its operation is described in detail in [4]. Our system uses a PJVS developed at NIST in its core and is being expanded to measure ac power. The rationale to invest efforts in this endeavor was the sensible reduction of the measurement uncertainties for ac power at INMETRO.

## II. HARDWARE DESCRIPTION

Apart from the small filled up square in the middle of Fig. 1 containing amplifiers, DUT, magnetic transducers (VT and CT) and shunt ( $Z$ ), the system and its operation around that block was thoroughly described in [4]. A brief description on the hardware components follows next for the sake of consistency.

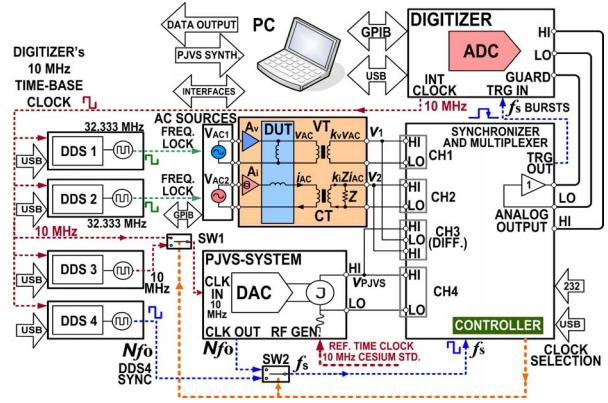


Fig. 1. Schematics of a PJVS based ac power standard (see text).

The NIST-PJVS (at the bottom) is synchronized with the 10 MHz time-base of the system (from the ADC) via switch SW1. A similar 10 MHz synchronization signal can be produced by a direct digital synthesizer (DDS3) to allow a precise phase shifting of the PJVS signal  $v_{\text{PJVS}}$  (a stepwise approximated waveform with  $N$  plateaus and of fundamental  $f$ ) with respect to the ac sources  $V_{\text{AC}1}$  and  $V_{\text{AC}2}$ , also frequency locked to the digitizer's 10 MHz reference clock via DDS1 and DDS2. The PJVS signal  $v_{\text{PJVS}}$  (from a data table loaded into the PC) is generated using the 10 MHz time-base of a primary cesium frequency standard that locks the PJVS' microwave generator. The sampling frequency  $f_s = Nf$  may be generated by the PJVS itself (CLK OUT output) or by DDS4, selected through SW2. DDS4 allows shifting of the sampling point over each plateau of  $v_{\text{PJVS}}$  (by slight step changes of  $f_s$  over a small time-interval  $\Delta t$  [4]). The synchronizer and multiplexer, interfaced to a PC, provide  $MN$  clock bursts of  $MNT_s$  seconds to the ADC to sample  $M$  integer periods of the direct voltages  $v_{\text{PJVS}}$ ,  $v_1$  and  $v_2$ , or the differential voltages  $v_{\text{PJVS}} - v_1$  and  $v_2 - v_1$  [4]. The signals  $v_1$  and  $v_2$  are replicas of the higher magnitudes signals  $v_{\text{AC}}$  and  $i_{\text{AC}}$  applied to device under test (DUT).

VT is a two-stage IVD with ratio errors smaller than  $10^{-6}$  in amplitude and phase and with a nominal voltage ratio  $k_v$  equal to 20. For a  $v_{\text{AC}}$  of 120 V in magnitude,  $v_1$ 's magnitude is 6 V. The CT under construction is a highly accurate comparator-like transducer [5]-[6] (of errors smaller than  $10^{-6}$ ) comprising a high permeability core and magnetic shields to handle currents of 1 A to 10 A. Its nominal current ratio  $k_i$  ranges from 100 to 1000. The shunt  $Z$  is a Vishay VHP series high stable resistor of  $600 \Omega$  and of small time constant (to be calibrated with a digital sampling bridge as described in [7])

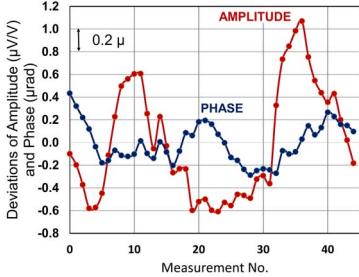


Fig. 2. Short-term stability in amplitude and phase of one ac source.

resulting in a  $v_2$  of 6 V in magnitude (as that of  $v_1$ ). Present investigations concentrate on the best configuration for CT. More details about CT will be available at the conference.

Amplifier  $A_v$  is of the type described in [8], and  $A_i$  is a modified version of the transconductance amplifier described in [9].

The sampling processes are fully described in [4] and ac power is calculated as described in [10] using either sampled data from direct or those from differential sampling. The expected ac power uncertainties are of the order of 2  $\mu\text{W}/\text{VA}$ .

### III. THE AC SOURCES

The ac sources are two identical audio sinewave generators with high amplitude stability and total harmonic distortion lower than -110 dBc. The short-term voltage amplitude and phase stability of one source is smaller than about 1.6  $\mu\text{V}/\text{V}$  and 0.5  $\mu\text{rad}$  respectively, for a set of 45 single measurements taken over 10 minutes (see Fig. 2).

Their internal clocking circuitry operating at 32.333 MHz was modified in house to allow their external synchronization through DDS1 and DDS2. However, these sources slightly truncate their signal output frequency  $f$ , resulting in ac signals not commensurate with the required ADC sampling frequency  $f_s$ . Their 32.333 MHz reference clocks need adjustment to counteract this truncation before meaningful measurements can be done. This adjustment is made by an independent digital regulator in the control software to strictly attain  $f_s = Nf$ . Starting with the DDSs' output reference clocks set to 32.333 000 MHz, the regulator [4] ends up at the sixth iteration (after some 60 seconds) with an output frequency set to 32.333 695 531 06 MHz in both DDSs (see Fig. 3). The correction applied to the reference clocks was at the end thus  $-9.1 \cdot 10^{-12} \text{ Hz}/\text{Hz}$ , i.e., smaller than the user's predefined threshold of  $1.0 \cdot 10^{-11} \text{ Hz}/\text{Hz}$ . This made the regulator to stop, and the reference frequency remained at that end value for the signal frequency  $f$  equal to 96 Hz.

### VI. CONCLUSION

Experimental evidences from preliminary investigations done with some components of the system look very

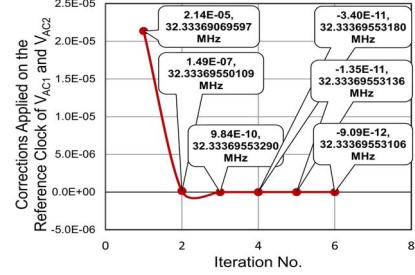


Fig. 3. Iterations done by the digital regulator to correct for  $V_{AC1}$ 's and  $V_{AC2}$ 's truncation error on their output signal frequency  $f$  in order to make  $f$  commensurate with the sampling frequency. The inserts show the corrections applied and the resulting updated reference time-base frequency.

promising towards attaining the goals of reducing measurement uncertainties of ac power. Additional information about the system under development will be made available at the conference.

### ACKNOWLEDGEMENT

This work is being conducted in the frame of the project Pronametro, contract no. 52600.057476.

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