# Fast Digital Post-Processing Technique for Integral Nonlinearity Correction of Analog-to-Digital Converters: Validation on a 12-Bit Folding-and-Interpolating Analog-to-Digital Converter

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***Abstract*—The semiconductor industry tends to constantly increase the performances of developed systems with an ever-shorter time-to-market. In this context, the conventional strategy for mixed-signal component design, which is based only on analog design effort, will no longer be suitable. In this paper, a digital correction technique is presented for analog-to-digital converters (ADCs). The idea is to use a lookup table (LUT) for the online correction of integral nonlinearity (INL). The main challenge for this kind of technique is the cost in time and resources to estimate the actual INL of the ADC needed to load the LUT. In this paper, we propose to extract INL with a very rapid procedure based on spectral analysis. We validate our technique on a 12-bit folding-and-interpolating ADC and we demonstrate that the correction is efficient for a large range of application fields.**

***Index Terms*—Analog-to-Digital Converter (ADC), Integral Non-Linearity (INL), lookup table (LUT), nonlinearity correction.**

## I. Introduction

CURRENT design trends not only reduce circuit surface by increasing integration rate and decreasing gate transistor width, but are also driven by system performance and shorter time-to-market. This induces a constant need to increase analog- and mixed-signal component performances and constantly shorter time for development. Conventional design strategy based only on analog design effort will no longer be suitable. Either the direct cost of this effort is prohibitive, if time limits are respected, or the production yield is low because of the tight design margins.

An attractive solution to help designers move into the challenging increase of mixed-signal circuits, which also offers a short development time, consists in using the power of the digital core to compensate the lack of performance of the analog part. This kind of "digital" correction is more easily transferable onto subsequent designs and can be adapted very easily to the specific constraints of targeted applications.

In heterogeneous systems, the key components are the converters and especially the analog-to-digital converters (ADCs). The context previously presented also forces the performances (resolution, sampling frequency, and linearity) of converters to increase rapidly and the ADC is going to become the crucial element, as much as the RF transceiver design was for the software-defined radio [1].

Thus, to combine ADC performance with short design time, an alternative solution is the correction of integral nonlinearity (INL). Many published papers address this research topic. For instance, in [2], the authors proposed to calibrate the internal capacitances of a pipelined ADC to correct nonlinearity. There also exist adaptive digital correction techniques for $\Delta\Sigma$ converters [3], [4]. A well-known technique called dithering consists in adding noise to reduce the effect of quantization and nonlinearity [5]. None of these solutions for correction is generic and none is suitable for our application, the INL correction of a 12-bit folding-and-interpolating ADC. The first two solutions are not suitable for this kind of architecture and our ADC will be used in telecommunication applications. For this kind of application, we cannot add noise because noise level is as much a critical characteristic of the ADC as the level of harmonics.

Another solution consists in using a post-processing correction table, also called lookup table (LUT). The efficiency of this technique is obviously based on the quality of the table used to correct the nonlinearity. The table is usually computed using measurements of the INL of the ADC. INL is a conventional test parameter generally measured using a histogram-based method. This method has demonstrated its effectiveness for long periods but its main drawback is the huge amount of sampling required to compute the INL. As ADC resolution increases, test time also increases. With the rapid increase of ADC resolution, it is going to be difficult to implement this method. This is why we propose alternative techniques to avoid the need for a histogram-based method to measure INL, which can present a lack of accuracy that could be a significant

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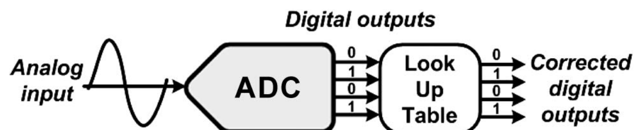



Fig. 1. Post-processing correction of ADC nonlinearity with LUT.

drawback for testing. In the present case, the accuracy of the extremes is not a critical constraint; we consequently adapt one of these estimation methods.

The first section presents the published LUT-based correction techniques, and the approach that we have chosen to develop. The alternative rapid procedure technique chosen for INL estimation is detailed in Section III. The last section describes the experimental validation of the method. It gives the results of comparison between corrections, first using the conventional histogram-based technique to extract INL, and then using our extraction method. Finally, the robustness of the method is precisely presented.

## II. LUT-Based Correction

### A. State-of-the-Art

We can find in the literature several publications that propose the correction of ADC nonlinearity using LUTs [6]–[12]. As shown in Fig. 1, the basic principle consists in using current or previous output codes to address a correction table that gives the corrected codes. We can distinguish two approaches: static and dynamic correction.

The static correction of an $n$-bit ADC uses $2^{\mathrm{n}}$ words of an $n$-bit LUT. Addressing the LUT is made by the current code value [6], [7]. According to published results [8], the correction is effective for input frequencies close to the frequency used to complete the correction table. In other words, these methods are only effective if the harmonics created by the ADC (or the ADC transfer functions) are relatively insensitive to input frequency variation.

Dynamic correction has been developed to overcome the limitations of static correction [7]. To consider dynamic nonlinearity, the authors use not only the current output codes, but also previous ones, or additional computed data. We can distinguish two different approaches.

First, there is the phase-plan technique [6]. Authors use the computation of the input signal slope as additional addressing data. The resulting table has two dimensions. There is a constraint induced by the computation of the input signal slope. Indeed, to obtain a good estimation of the slope, the two samples used should be very close. But the smallest gap between two samples is given by the sampling frequency, which is too large to obtain a good estimation of the slope.

The second dynamic correction method is called state-space correction [6], [9]. The authors propose the intuitive solution of considering variations of the input signal using K previous samples. The size of the correction table is related to the number of previous samples used: K previous samples plus the current sample gives a space of dimension $\mathrm{K}+1$, and consequently a $\mathrm{K}+1$ dimension table of $2^{\mathrm{n}}$ samples. The drawback of this method is the huge size of the table and the long time to address it using $(\mathrm{K}+1)^{*}\mathrm{n}$ bits for an $n$-bit ADC. Solutions have been proposed to reduce addressing complexity. Previous samples can be under-sampled and truncated [10], [11] or certain bits can be masked after a learning phase. Several different addressing techniques have been compared in [12]. According to the authors, for the case where complexity is close to the static correction, the effectiveness of the correction is similar to the effectiveness of the static correction. Although dynamic correction is a promising technique, the benefit is insufficient compared to the increase of complexity. We therefore decided to use the static correction approach.

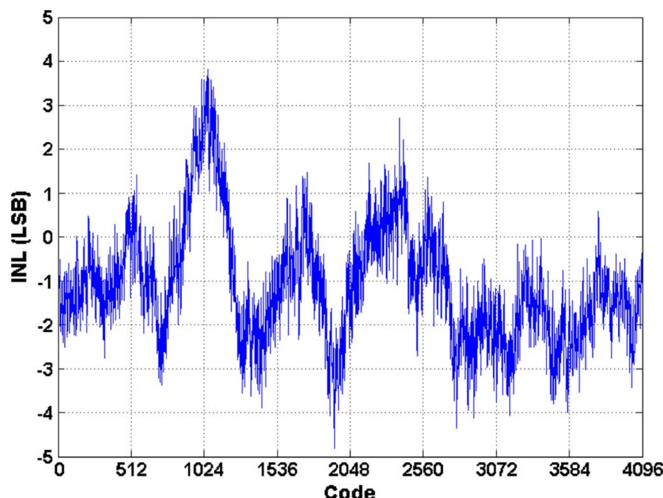



Fig. 2. INL curve of a 12-bit ADC.

### B. Completing the LUT

The histogram-based method is a conventional test method mainly used to measure the INL of the ADC under test [13], [14]. The INL curve, such as the one shown in Fig. 2, is measured by a histogram-based test. The abscissa of the graph is the expected output codes and the ordinate is the deviation expressed in least significant bit (LSB) between the ideal and the actual output code. Then, the extremes of the INL curve are computed to measure the INL test parameter defined in the datasheet.

The table used to complete the LUT is made up of the corrected codes computed using the INL curve previously presented. The computation consists in rounding off the previously measured INL curve, as shown in Fig. 3, and subtracting the result from the ideal transfer function.

This correction table should enable the correction of the static nonlinearity of the ADC with $\pm$ 0.5LSB accuracy.

## III. Methods for INL Measurement

### A. Conventional Method for INL Measurement

As previously mentioned, a histogram-based method is widely used to measure the INL curve of ADC. The advantage of this method is its accuracy. The main drawback is the quantity of samples required and consequently the testing time. Indeed, the higher the ADC resolution, the higher the number

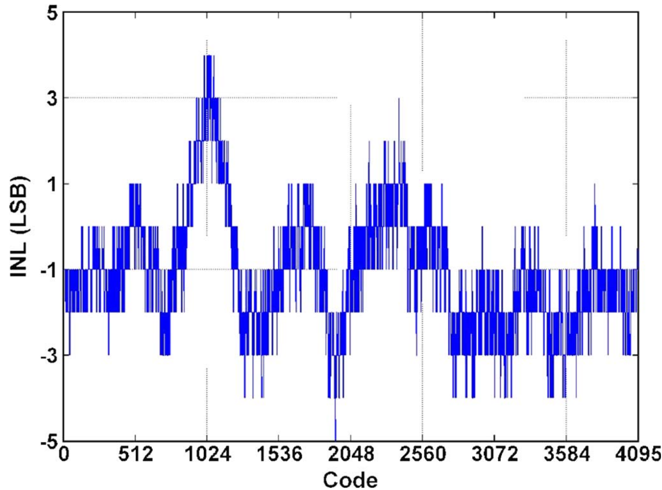



Fig. 3. Rounded-off INL.

of samples for the test, and for middle or high resolution conversions the associated test time can be prohibitive. For instance, the histogram-based test for a 14-bit ADC required at least 8 M samples [13], [14].

### B. Alternative Method for INL Measurement

We can find in the literature several publications that address this time-consuming drawback of the histogram-based test technique. Several methods have been developed to achieve a low-cost test of static parameters such as INL.

Some recent techniques are based on the modeling of the INL with complementary components: the low frequency component (LFC) and high frequency component (HFC) [15], [16]. It is also possible to extend the model to the dynamic INL (DLFC) to take into account the variation of the INL according to the signal or sampling frequency [17], [18]. Each INL component can be extracted with a specific test technique (generally based on histograms) with a reduced and optimal number of samples. For compensation purpose, only the LCF component (static and dynamic) is needed and the technique could be interesting. Unfortunately, the number of required samples remains relatively high (for instance $10^7$ samples for a 16 bit ADC).

An alternative approach consists is using the strong link between static and dynamic parameters. In other words, INL significantly influences dynamic performance by the generation of harmonics. Because dynamic parameters are extracted from the spectral analysis, the INL can be estimated from the same spectrum. The advantage of using a Fast Fourier Transform (FFT)-based INL estimation method instead of a conventional histogram-based method is the reduced number of samples required. Practical experiments show that the FFT-based test requires at least 64 times fewer samples than the histogram-based test using coherent sampling.

Two very different approaches can be used to evaluate the relationship between static and dynamic specifications.

1) A statistical approach proposed in [19] consists in detecting devices for which one of the functional parameters overruns specifications, but this kind of statistical method cannot be used for a post-processing correction because it is only a go/no go test without estimation of the actual INL value.
2) An analytical approach that consists in identifying the Fourier coefficients obtained with the classical FFT, with the parameters that describe the INL curve. Most of the proposed techniques are based on the polynomial interpolation of INL [20]–[24], although there is also a method [25]–[27] based on the Fourier series expansion of the INL.

The advantage of these alternative analytical methods is the smaller number of samples required to perform the FFT. Using the many harmonic values created by the ADC under test, they give a good estimation of the INL curve shape.

Unfortunately, the statistical approach cannot give a value of the INL; this is only suitable for test procedures dedicated to detect faulty devices. The analytical approach gives the value of INL but the estimation of the sharp variations of the INL curve requires the extraction of high order parameters in the series expansion involving a very large matrix and a complex computation which could be a significant drawback to compute the INL parameter in a production test context. On the other hand, we can imagine that, to compensate the nonlinearity, an estimation of the smooth shape of INL estimated with few parameters of the series expansion might be sufficient.

## IV. INL Estimation Method for Compensation

We want to use the solution that gives the best compromise between speed and lack of precision in the specific context of post-correction. As previously explained, these techniques try to describe the INL curve from a spectral analysis. This analysis is made directly on the distorted signal and requires fewer samples than the usual histogram-based method, but INL description is needed to link the spectral parameters to the coefficients of the model used for the description of the INL curve.

### A. Model of the INL Description

The usual model is polynomial, but a recent paper [26] has proved that better accuracy is achieved with a technique based on discrete Fourier series expansion [25]–[27].

The following mathematical developments, first presented in [25]–[27], demonstrate the theoretical link between the INL curve and the harmonics induced by an ADC. Our objective is to summarize here the major theoretical developments needed to understand the paper. The details of the method are given in [25]–[27]. To begin with, certain mathematical requirements must be fulfilled to use such an expansion. For these requirements, we consider a periodic extension $\phi(x)$ of the INL curve, associated with an ADC of resolution $res$ bits and defined by

$$\begin{cases} \phi(x) = INL(x), 0 \leq x \leq 2^{res} - 1 \\ \phi(x + p.2^{res}) = INL(x), p \in \mathrm{Z} \end{cases} \quad (1)$$

where $x = 0, \ldots, 2^{res} - 1$ is the digital output code of the converter. The truncated discrete Fourier series expansion of

this function leads to the well-known expression given by

$$\phi(x) \approx \frac{a_0}{2} + \sum_{k=1}^{K_{MAX}} (a_k \cos(k\omega x) + b_k \sin(k\omega x)) \text{ with } \omega = \frac{2\pi}{2^{res}}. \tag{2}$$

To avoid huge computation, we deliberately limit the order of expansion to the $K_{MAX}$ first parameters; this means that the INL curve is described with only $2.K_{MAX} + 1$ parameters. The value of $K_{MAX}$ is set in function of the accuracy needed and will be specified in a further paragraph.

### *B. Relationship Between Parameters of the INL Description and Spectral Bins*

The following matrix product links the coefficients of the INL model to the power spectrum harmonic amplitudes $S_h$ of the distorted signal.

$$\begin{bmatrix} a_0 \\ \vdots \\ b_{K_{MAX}} \end{bmatrix} = T_{KMAX}^{-1} \cdot \begin{bmatrix} S_0 \\ \vdots \\ S_{H_{MAX}} \end{bmatrix}. \tag{3}$$

Consider an input sine wave defined by

$$u(t) = V_0 . \cos(2\pi f_0 t + \theta_0) + V_{DC} \tag{4}$$

where $V_0$ is the amplitude, $F_t$ its input frequency, $\theta_0$ its initial phase, and $V_{DC}$ its DC component. Its digitized expression is then

$$u(n) = 2^N \left(\frac{V_0}{V_{FS}}\right) \cos(\theta_n) + 2^N \left(\frac{V_{DC}}{V_{FS}}\right) + q(n) \tag{5}$$

where $q(n)$ is the quantization uncertainty (or noise) term that will be neglected due to the high resolution of the kind of converter targeted.

$$\theta_n = 2\pi \frac{M}{N} n + \theta_0 \tag{6}$$

where $M$ and $N$ are, respectively, the number of periods and samples taken and $n$ is the index of the sample. $M$ and $N$ respect the fundamental equation of coherent sampling

$$\frac{M}{N} = \frac{f_s}{f_0} \tag{7}$$

where $f_s$ is the sampling frequency.

Matrix $T_{KMAX}$ is fully determined by

$$T_{K_{MAX}} = \begin{pmatrix} 1/2 & A_1^0 & \cdots & A_{K_{MAX}}^0 & B_1^0 & \cdots & B_{K_{MAX}}^0 \\ 0 & A_1^1 & \vdots & A_{K_{MAX}}^1 & B_1^1 & \vdots & B_{K_{MAX}}^1 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & A_1^{H_{MAX}} & \cdots & A_{K_{MAX}}^{H_{MAX}} & B_1^{H_{MAX}} & \cdots & B_{K_{MAX}}^{H_{MAX}} \end{pmatrix} \tag{8}$$

In the case of $V_{DC} = V_{FS}/2$, there results

$$\begin{aligned} A_k^0 &= (-1)^k J_0(k\alpha_1) \\ A_k^{2p+1} &= 0 \\ A_k^{2p} &= (-1)^{p+k} 2 J_{2p}(k\alpha_1) \\ B_k^{2p} &= 0 \\ B_k^{2p+1} &= (-1)^{p+k} J_{2p+1}(k\alpha_1) \end{aligned} \tag{9}$$

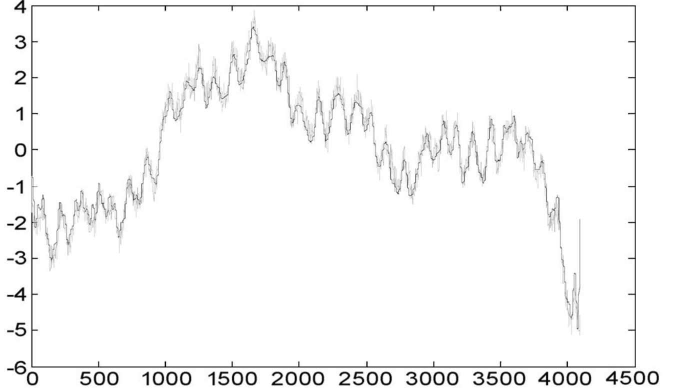


Fig. 4. INL estimation for $H_{MAX} = 200$ and $K_{MAX} = 100$.

where $\alpha_1 = 2\pi V_0/V_{FS}$ and $J_p(x)$ is the Bessel function of the $p$th order.

As the matrix is not directly invertible, we use a singular value decomposition algorithm (SVD) to invert it. The inversion of the matrix $T_{KMAX}$ via an SVD algorithm gives rise to the computation of the $a_k$ and $b_k$ parameters of the INL from the measurement of the $S_h$ spectral parameters.

The estimated curve fully succeeds in giving a description of the nonlinearities of the converter, as shown in Fig. 4.

## V. Experimental Validation

### *A. Experimental Setup*

In an industrial context, the post-correction method would consist in measuring the INL and computing the LUT during the test time. The instrumentation would be the automated test equipment (ATE) traditionally used to achieve dynamic testing. The INL measurement and LUT computation would obviously be done for every ADC, as far as the INL curve of each ADC is unique.

The experimental validation vehicle is a 12-bit ADC. This ADC features folding-and-interpolating architecture. This ADC is designed to play in under-sampling mode or in classic sampling mode. The input bandwidth is up to 175 MHz and the sampling frequency bandwidth is up to 90 MHz. The specified thermal range is from −40 °C to +85 °C. An FPGA has been used to catch the ADC output codes and to store the LUT. The choice of an FPGA enables a greater flexibility to use the method.

### *B. Comparison of INL Curve Estimation Methods*

Table I presents the measurements of five dynamic parameters [13], [14]: signal-to-noise ratio (SNR), spurious free dynamic range (SFDR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), and the time required during the trimming phase to apply INL correction. The parameters have been measured three times: without correction, with correction using the histogram-based method to measure the INL curve, and with correction using the spectral-based method to measure the INL curve. The number of samples used for the histogram-based method and the number $H_{\max}$

TABLE I
TEST PARAMETERS BEFORE AND AFTER CORRECTION

| Parameter | w/o correction | w/ correction ( histogram-based estimation) | **w/ correction (spectral-based estimation)** |
|---|---|---|---|
| SNR (dB) | **61.07** | **65.37** | 66.53 |
| SFDR (dB) | **66.59** | **84.44** | 84.90 |
| THD (dB) | **-74.44** | **-82.62** | -83.42 |
| SINAD (dB) | **60.87** | **65.28** | 66.88 |
| **ENOB** | 9.82 | 10.58 | 10.72 |

of harmonics used for the spectral-based method are important, as it is necessary to have the best estimation possible. We used 262144 samples for the histogram-based technique, 16384 samples for the FFT computation, and 200 harmonics ($H_{\max} = 200$) for the spectral-based computation of the INL curve.

With regard to these experimental results, we can extract three positive conclusions:

1) For both corrections, we have a great improvement of all parameters. The ENOB is improved by at least 0.7 bit and the increase for the other dynamic parameters is between 5 and 18 dB.
2) The correction using the rapid extraction of INL gives better results than the correction using the histogram-based extraction of INL.
3) As expected, correction with the FFT-based method is faster than with the histogram-based approach.

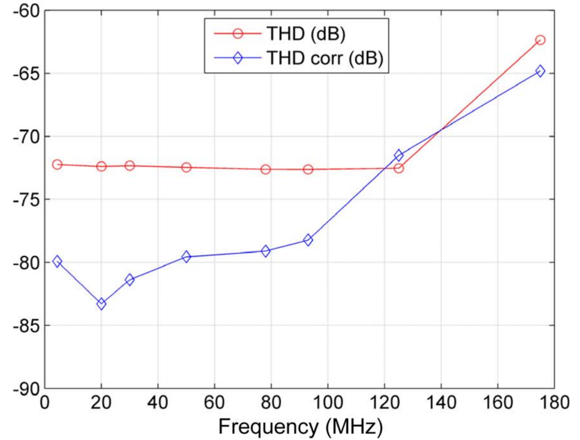
To summarize, the results show that the correction of nonlinearity using a LUT is very effective, increasing both the ENOB of at least 0.7 bit and the dynamic range of 5 to 18 dB. The spectral-based method is more efficient and significantly faster than the histogram-based method to estimate the INL curve for correction.

Obviously, these results are obtained in specific test conditions. As explained in Section II-A, we must know if this static correction remains viable for the complete application field of the ADC.

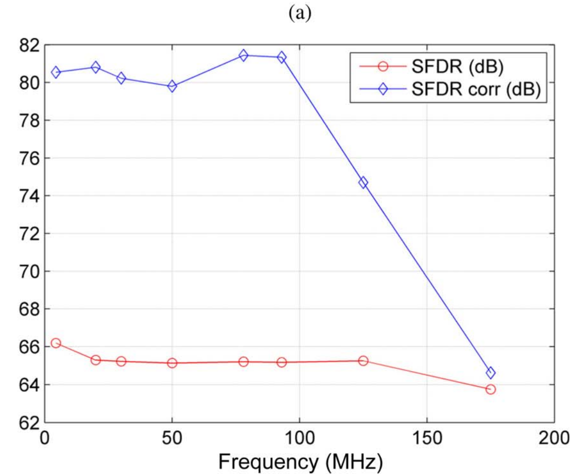
### C. Robustness of the Compensation

As previously mentioned, the correction table is loaded in the LUT once during the manufacturing process. This correction table is based on the measurement of the INL curve of the DUT. As a consequence, this INL curve is measured once for one given input frequency and one given sampling frequency. Nevertheless, the product must ensure good conversion performances for a large input bandwidth, different sampling frequencies, and a relatively large temperature range. In other words, the compensation method should be effective for both frequency bandwidth and temperature range.

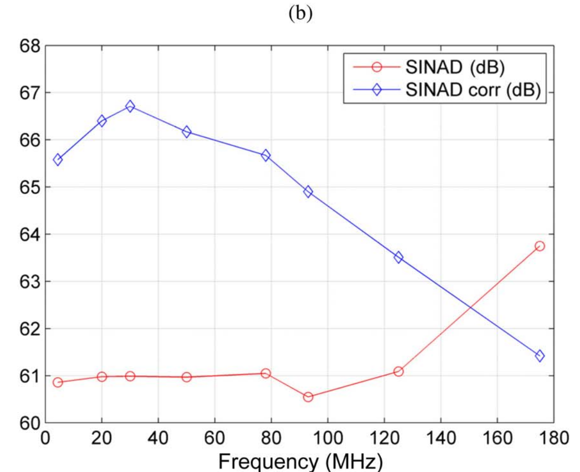
*Sensitivity to Input Frequency:* The INL curve was measured once at $\mathrm{Fs} = 80$ MHz and $\mathrm{Fin} = 78$ MHz using the spectral-based method. Three dynamic parameters, THD, SFDR, and SINAD, were measured with and without correction for an input frequency varying from 4.43 MHz to 175 MHz. Fig. 5 shows the results obtained.



(a)



(b)



(c)

Fig. 5. (a) THD. (b) SFDR. (c) SINAD vs input frequency.

According to Fig. 5, the correction is effective for input frequencies lower than that used to measure the INL. Above 78 MHz, the dynamic parameters approach the uncorrected values. This limitation can be explained by the fact that the gain and offset errors are not taken into account in the INL curve measurement. These two errors are very sensitive to input frequency variation, particularly because a sample-and-hold input stage is used in this architecture. Nevertheless, we can say that a single table can achieve an efficient correction on a large input bandwidth. Within the application field of the targeted ADC, the correction is very efficient, with a gain of 8 dB on THD [Fig. 5(a)], 14 dB on SFDR [Fig. 5(b)], 4 dB on SINAD [Fig. 5(c)], and 0.4 bits on the ENOB.

*Sensitivity to Sampling Frequency:* The next experiment focuses on the effect of sampling frequency variation on the effectiveness of correction. The INL curve used for later corrections was measured at Fs = 60 MHz and Fin = 93 MHz. Then, the three dynamic parameters were measured with and without correction for sampling frequencies varying from 20 to 90 MHz. The results are presented in Fig. 6.

The best correction is obtained for sampling frequencies close to that set for the INL curve measurement. When the sampling frequency moves away from the frequency set for the INL curve measurement, correction efficiency decreases. Nevertheless, the correction allows us to gain 3 to 10 dB of THD, 3 to 11 dB of SFDR and 0.4 to 1.2 dB of SINAD for a sampling frequency from 20 to 80 MHz.

It is important to notice that an ADC embedded in an application usually operates at a constant sampling frequency. To optimize the efficiency of the post-processing correction, the LUT has to be completed with an INL curve close to the sampling frequency of the targeted application. This is coherent with the current trend in the semiconductor industry, where circuits are more and more dedicated and ADCs are generally a very small part of a larger system, SiP (System-in-Package) or SoC (System-on-Chip).

*Sensitivity to Temperature:* The final experiments consisted in using the circuit over a wide temperature range (from −40 to 80 °C) and evaluating the influence of this temperature on correction efficiency. The correction table was computed at 27 °C, with a sampling frequency of 40 MHz and an input frequency of 4.43 MHz (see Figs. 7–9).

As sampling frequency and temperature increase, performances decrease. Close to the sampling frequency and temperature used to compute the correction table, performances are very good. Indeed, we observe SFDR and THD between ±80 and ±85 dB, and the SINAD reaches 64 dB. The improvement of test parameters is not always at its maximum; nevertheless, it is always significant: between 5 and 25 dB for THD and SFDR, and between 2 and 4 dB for SINAD

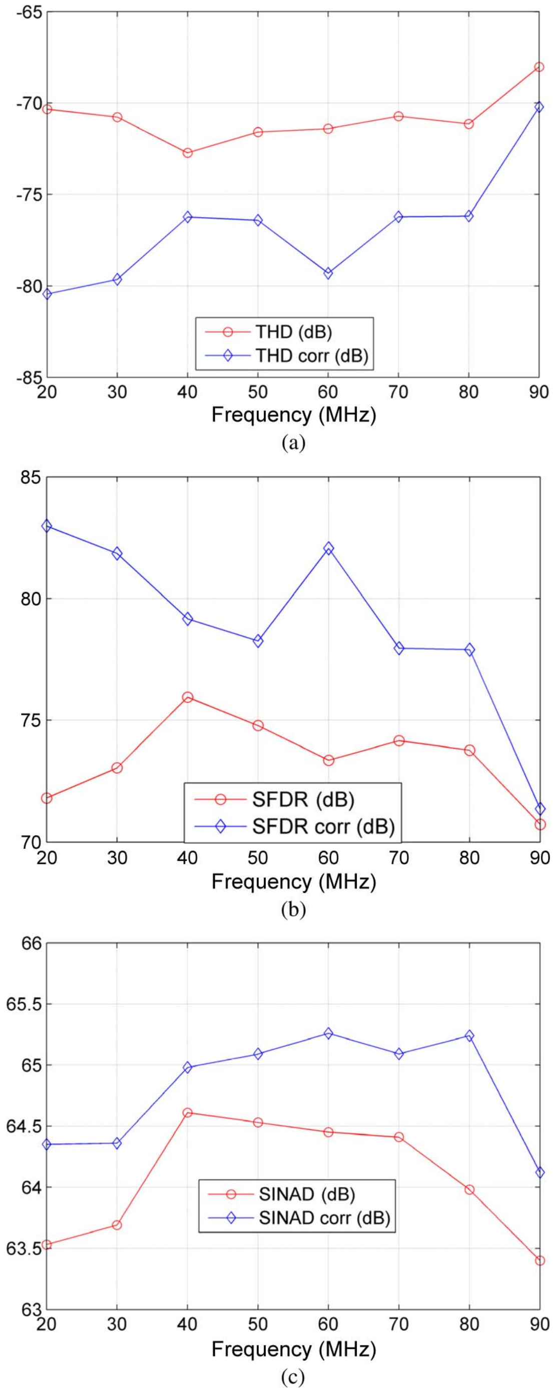



Fig. 6. (a) THD. (b) SFDR. (c) SINAD vs sampling frequencies.

## VI. Conclusion

Based on our test vehicle, a 12-bit folding-and-interpolating ADC, we have successfully validated a static correction table. The study of the robustness of the proposed technique has showed that the domain of validity is very large and covers the ADC application field. Moreover, we have validated that, to compute the correction table, it is not necessary to use a conventional histogram-based technique. We have used a low-cost technique using only spectral bins. This technique allows us to estimate the INL curve with a time at least 64 times shorter than the conventional histogram-based method. It is clear that these results cannot be generalized to any kind of ADC architecture or application. In some cases, the dynamic part of the INL is not negligible and a static correction could then be ineffective.

These encouraging results and the system design trends promise an interesting future to the digital post-correction of

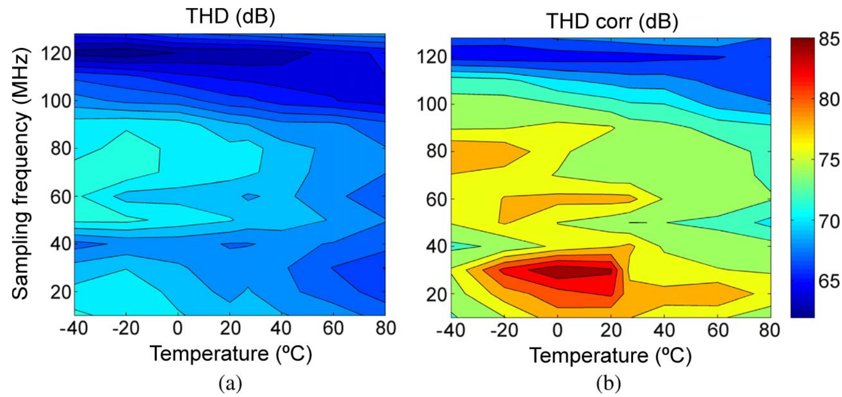



Fig. 7. (a) THD without correction (b) THD with correction Vs temperature and sampling frequency.

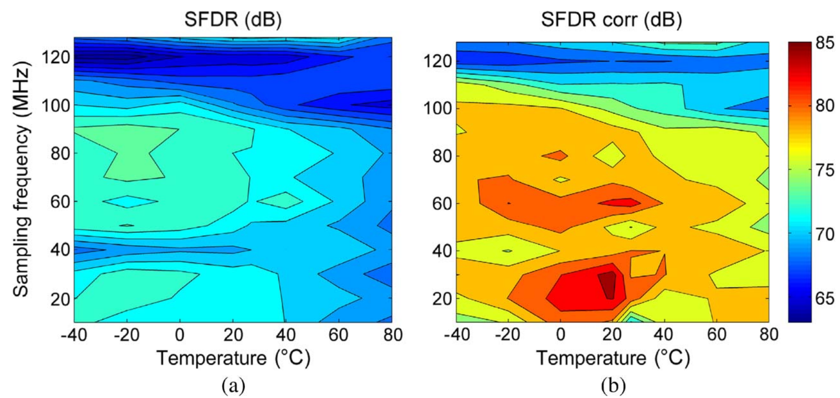



Fig. 8. (a) SFDR without correction (b) SFDR with correction Vs temperature and sampling frequency.

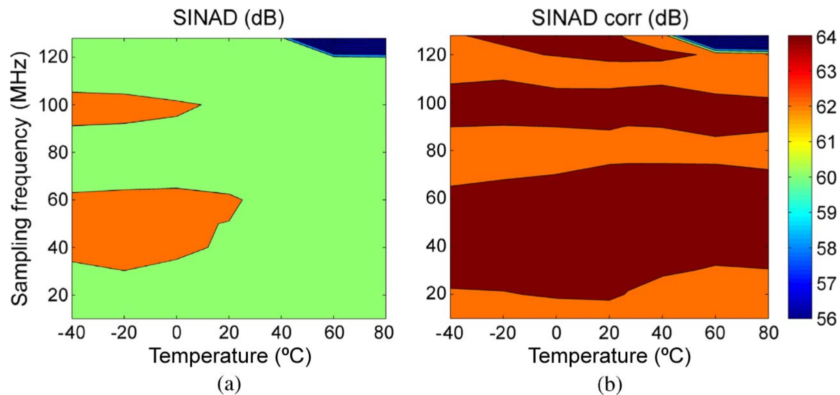



Fig. 9. (a) SINAD/ ENOB without correction (b) SINAD with correction Vs temperature and sampling frequency.

ADC. Indeed, as mentioned in the introduction, the design of RF transceivers tends to software-defined radio. As a consequence, higher speed and resolution will be required for ADCs. However, the design of an ADC is a tradeoff between its development time and its performances. By using digital post-correction, we could relax design constraints on linearity and focus on design for speed.

Additionally, because it requires few resources, the correction technique approach can be implemented within the chip. This perspective is exciting because it offers the possibility of computing the correction table not only during the production or trimming stages, but also during the circuit's life, which would allow ageing of the chip to be compensated for, or adaptation to new application characteristics.

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