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Highly integrated front-end electronics for spaceborne fluxgate sensors

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Abstract
Scientific instruments for challenging and cost-optimized space missions have to reduce their resource requirements while keeping the high performance levels of conventional instruments. In this context the development of an instrument front-end ASIC (0.35 μm CMOS from austriamicrosystems) for magnetic field sensors based on the fluxgate principle was undertaken. It is based on the combination of the conventional readout electronics of a fluxgate magnetometer with the control loop of a sigma-delta modulator for a direct digitization of the magnetic field. The analogue part is based on a modified 2–2 cascaded sigma-delta modulator. The digital part includes a primary (128 Hz output) and secondary decimation filter (2, 4, 8, . . . , 64 Hz output) as well as a serial synchronous interface. The chip area is 20 mm^2 and the total power consumption is 60 mW. It has been demonstrated that the overall functionality and performance of the magnetometer front-end ASIC (MFA) is sufficient for scientific applications in space. Noise performance (SNR of 89 dB with a bandwidth of 30 Hz) and offset stability (< 5 pT $^\circ$C^{-1} MFA temperature, $< \pm 0.2$ nT within 250 h) are very satisfying and the linear gain drift of 60 ppm $^\circ$C^{-1} is acceptable. Only a cross-tone phenomenon must be avoided in future designs even though it is possible to mitigate the effect to a level that is tolerable. The MFA stays within its parameters up to 170 krad of total ionizing dose and it keeps full functionality up to more than 300 krad. The threshold for latch-ups is 14 MeV cm^2 mg^{-1}.

Keywords: fluxgate magnetometer, sigma-delta modulation, space instrumentation, miniaturization

1. Introduction

One possibility of reducing costs of planetary exploration and hence allowing for more frequent missions is to reduce the spacecraft size in order to bring required launch masses down. Scientific instruments for such missions, including their front-end electronics, consequently have to reduce their resource requirements such as volume, mass and power, while at the same time achieving at least the same performance as conventional instruments.

The read-out electronics of state-of-the-art fluxgate magnetometers (incl. analogue-to-digital conversion but without excitation circuit) for scientific measurements of dc and low ac magnetic fields ($<$100 Hz) in space (dynamic range $> \pm 1000$ nT, signal-to-noise ratio > 90 dB and total ionization dose hardness > 70 krad) is normally placed on an approx. 100 cm^2 large printed circuit board with a total mass of $>$100 g. The power consumption is greater than 500 mW. Although the comparison of different instrument designs is not simple and dependent on the application, instrument data for comparison can, e.g., be found in Anderson *et al* (2007), Auster *et al* (2008) and Carr *et al* (2007).

There are a number of limitations which prevent higher integration and miniaturization. The harsh environmental conditions in space with particle radiation and extended temperature ranges is one reason, but there also exist export restrictions as well as long lead times and high costs for highly integrated, space-qualified components.

Digital circuitry can be integrated by means of field programmable gate arrays (FPGAs). Most recent radiation tolerant FPGAs allow for high performance and complex digital circuitry being implemented within a single chip. There are no equally efficient solutions for analogue or mixed signal applications available off the shelf. In addition, the trend obviously goes to a signal conversion from the analogue to the digital domain as close as possible to the sensor(s). Nevertheless the *real world* is analogue and hence most of the readout and control signals for sensors are analogue as well, with the consequence that the integration and miniaturization of sensor readout and signal conditioning circuits require instrument specific and mixed signal application specific integrated circuits (ASICs).

The concept of a magnetometer front-end ASIC (MFA) for magnetic field sensors, which are based on the fluxgate principle (Acuña 2002, Auster 2008, Primdahl 1988, Ripka 2000), was elaborated in 2004. It is based on a combination of the readout electronics of a conventional fluxgate magnetometer with the control loop of a delta-sigma modulator (Magnes *et al* 2003) in order to get a further miniaturized, robust (especially in terms of radiation hardness) and highly sensitive near sensor electronics for a triaxial sensor. Since then a first test chip (MFA-1, Magnes *et al* 2007) followed by a redesigned MFA-2 with an improved analogue part have been developed and carefully checked for performance compliance and radiation hardness. Both ASICs were fabricated in a 0.35 μm 2P4M (two poly and four metal layers) CMOS technology from austriamicrosystems. The overall power dissipation of all four channels in the MFA-2 is 60 mW (16 mW per fluxgate channel and 12 mW for the voltage channel) at a supply voltage of 3.3 V digital and 3.5 V analogue, respectively. The chip area including pad ring is about 20 mm^2 (see figure 1) and the die is mounted to a CQFP-100 package with a size of 14 $\times$ 14 mm^2.

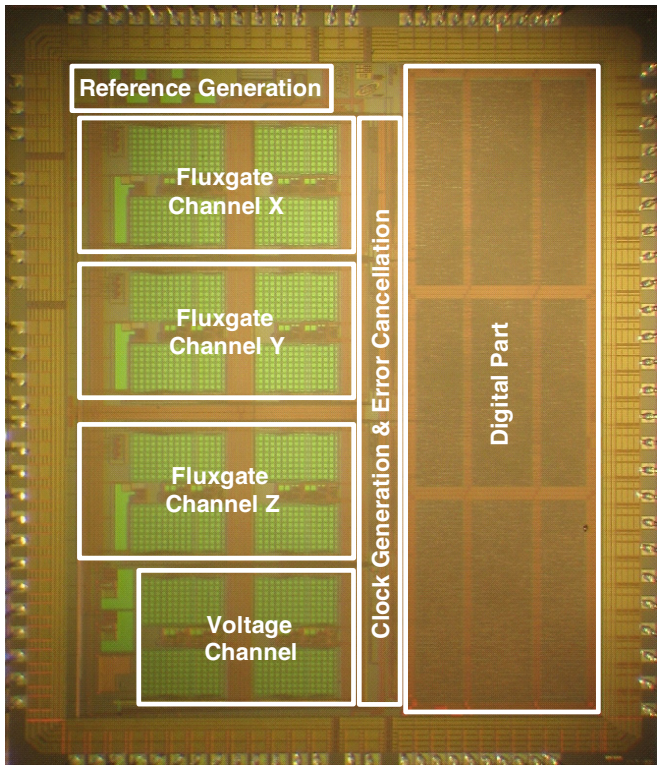

Figure 1. Chip micrograph of the magnetometer front-end ASIC (version 2).

2. System design

2.1. Principle of a sigma-delta fluxgate modulator

Figure 2 shows in which way the traditional control loop of a fluxgate magnetometer can be combined with the control loop of a second-order $\Sigma\Delta$ modulator. It was first introduced by Magnes *et al* (2003) and then successfully implemented in the THEMIS ground-based instruments (Russell *et al* 2008). Commonly, a fluxgate sensor is made of a soft-magnetic core (e.g. ring or double rod) placed in the centre of a solenoid pick-up coil (Primdahl 1988). The core is wrapped with a single layer of drive windings in order to saturate the magnetic material periodically by driving a pulse-shaped current with frequency f_0 (5–20 kHz) through the windings. The output signal of the pick-up coil therefore contains induced even harmonics of f_0 which are proportional to the external magnetic field. The readout electronics extracts the magnetic field information by synchronously converting and integrating the second harmonic ($2f_0$). Normally, the fluxgate sensor operates as a zero detector since the output voltage is fed back via a resistor into the pick-up or a separate feedback coil in order to increase the overall linearity. When combining the fluxgate control loop with a second-order sigma-delta modulator, the input junction point can be placed directly in the fluxgate sensor and the integrator which helps to demodulate the field information can be merged with the first integrator of the $\Sigma\Delta$ modulator.

2.2. Overview of analogue and digital design

The redesigned magnetometer front-end ASIC (MFA-2), see the block diagram in figure 3, comprises an analogue part with approx. 14 000 transistors and a digital part with approx. 25 000 logical gates.

The basic block of the analogue part is a 2–2 cascaded $\Sigma\Delta$ modulator which was originally designed for digitizing the output signals of wireless sensors (Hartmann *et al* 2004). It consists of two second-order switched-capacitor (SC) modulators with single-bit quantization in a fully differential architecture. It is an attractive option for high-resolution analogue-to-digital conversion (Boser and Wooley 1988) when considering potential instabilities, gain matching constraints of different modulator building blocks, proper shaping of quantization noise and robustness. In the MFA case it especially enables the merging with the fluxgate sensor.

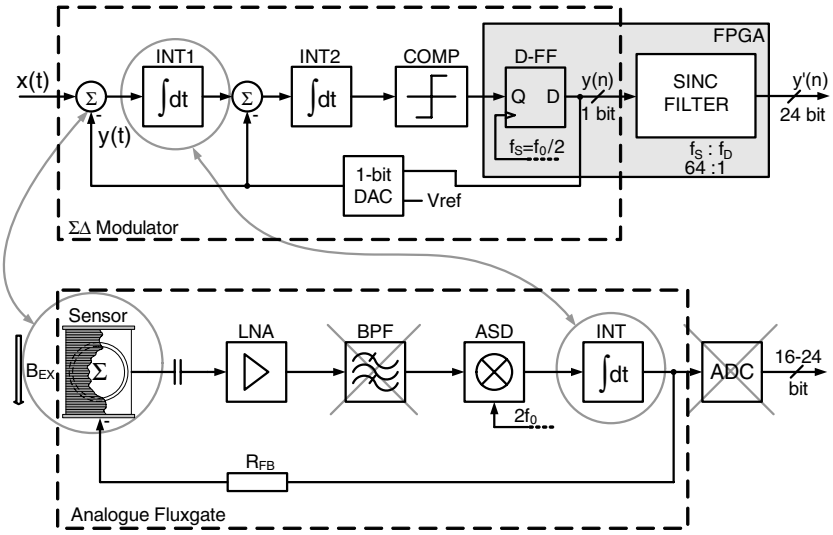

Figure 2. Merging of a second-order sigma-delta modulator with the fluxgate control loop.

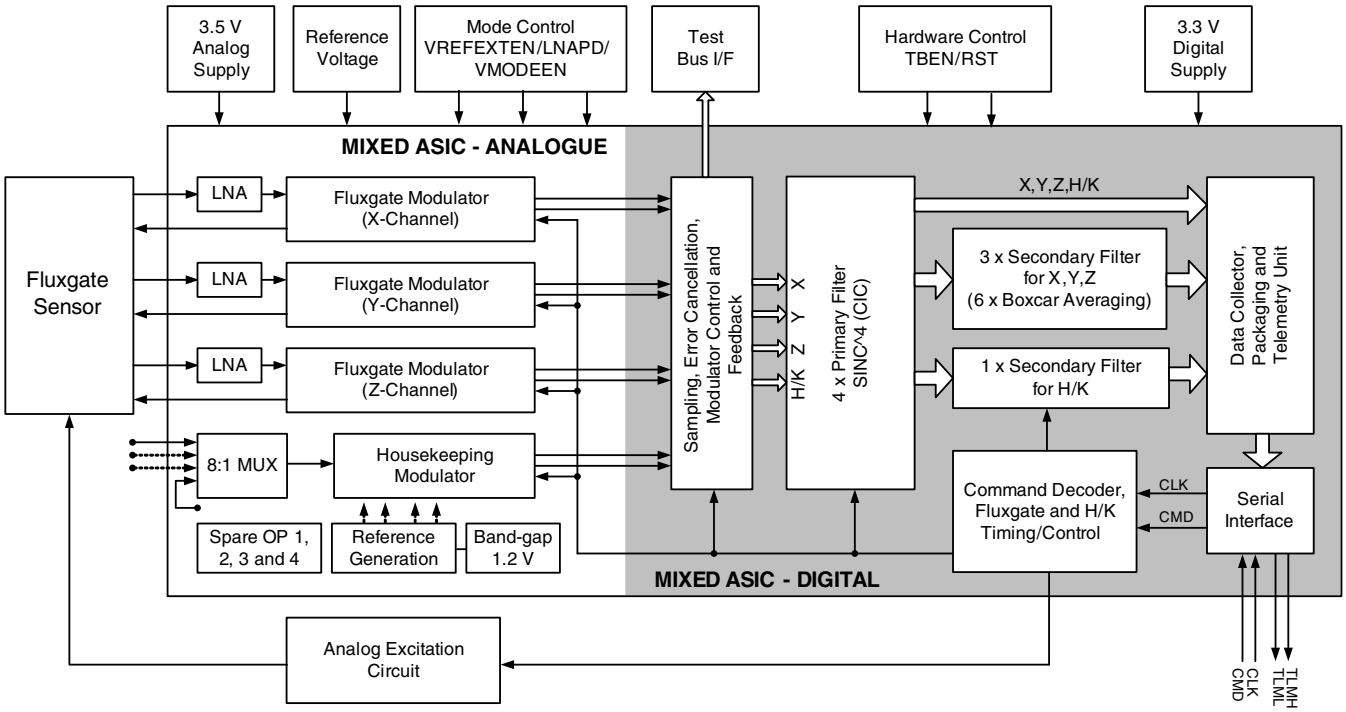

Figure 3. Block diagram of the redesigned magnetometer front-end ASIC.

The analogue part contains altogether four 2–2 cascaded modulators, three of which are connected to the fluxgate sensor and have modified first stages (see the block diagram of the *fluxgate modulator* in figure 4) for a precise vector measurement of the magnetic field. The fourth modulator (also called *housekeeping modulator*) is unmodified and connected to the output of an eight-to-one multiplexer for housekeeping measurements (e.g. temperature of MFA and fluxgate sensor).

The single-bit outputs of the cascaded modulators are processed by the error cancellation (EC) logic for generating a fourth-order noise shaped and digitized output signal with 6-bit data width at a sampling rate of 8192 Hz when the chip is clocked at 2^{22} Hz (about 4.2 MHz).

Apart from the four modulators, the analogue part contains three low-noise input amplifiers (LNA) for the fluxgate channels, a voltage reference generation unit, four spare op-amps which can be used for a proper conditioning of the signals measured by the housekeeping channel as well as two sensor elements for a chip internal measurement of the temperature and the analogue supply voltage.

The reference generation unit consists of an integrated bandgap reference with an amplifier (an external reference voltage can be selected via the mode control pin VREFEXTEN), a current reference and a resistor network with buffer amplifiers. The latter derives all required external (2.4 V and 0.4 V for driving a precise feedback current through

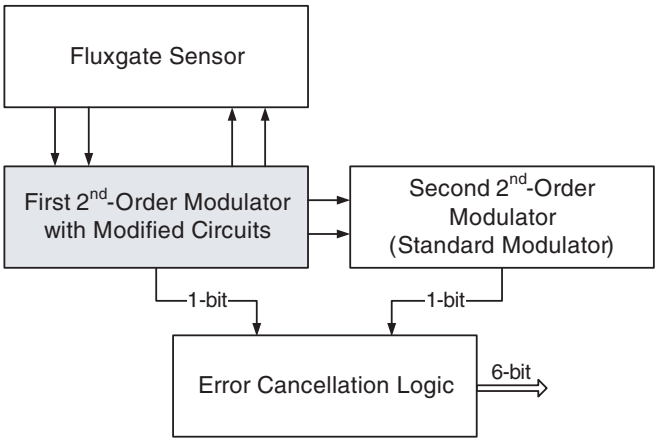

Figure 4. Block diagram of the 2–2 cascaded fluxgate modulator.

the feedback coils set by external resistors) and internal reference voltages (2.275 V and 1.025 V are used as standard internal switched-capacitor voltage references which results in a differential internal voltage reference of ±1.25 V).

The LNA was designed for the MFA-2 from scratch, since the single-ended pre-amplifier within the MFA-1 did not work properly. The new LNA has a PMOS input stage and is fully differential. Both inputs and outputs are connected to pins in order to allow for a flexible amplification with band-pass characteristics (centre frequency at $2f_0$) by a resistor–capacitor network outside the chip. The chip internal LNA in stand-alone configuration features a dc gain of 97 dB, a gain bandwidth of 4 MHz, an input noise density at $2f_0$ Hz of 8.6 nV $\mathrm{Hz}^{-1/2}$ and a power consumption of only 4.6 mW.

The digital part includes data processing in the primary (an oversampling ratio of 64 and an output data rate of 128 Hz) and secondary decimation filter blocks (output data rates: 2, 4, 8, ..., 64 Hz), a serial synchronous interface as well as the generation of all necessary control signals (e.g. $f_0 = 16\,384$ Hz). Furthermore, the 6-bit wide error cancellation outputs of the analogue part as well as a number of clock and status signals of the digital part can be checked out via an 8-bit wide test bus which is controlled with a 4-bit address bus and enabled via the mode control pin TBEN. Each MFA chip can be addressed by a unique address (3 bits) which is set externally. The hardware reset (RST) is used for resetting the MFA chip on power-up or if a hardware reset option is required by the system. The MFA design also includes a synchronization possibility via a dedicated synchronization command which resets the control clocks. It allows for a synchronization of one or more MFA chips to other science instruments which are operated by the same master clock with a precision of better than 122 μs.

A standard fourth-order sinc filter in a comb-integrator-comb design is used as the primary filter (Norsworthy and Crochiere 1997). The secondary decimation filter contains six identical filter blocks, each of which reduces the input data rate by a factor of 2. It is realized as an averaging filter without overlapping. The output data width of both primary and secondary filters is 24 bit.

2.3. Linearized model and tuning of the fluxgate modulator

The linearized model of the fluxgate modulator implemented on the chip is depicted in figure 5. It consists of the modified second-order ΣΔ modulator (fluxgate sensor, input amplifier, adjustable synchronous demodulator (ASD), integrators 1 and 2, 1-bit quantizer 1) and an unmodified second-order ΣΔ modulator (integrators 3 and 4, 1-bit quantizer 2). Both quantizers sample at half of the excitation frequency ($f_S = f_0/2 = 8196$ Hz). The outputs of the modulators (Y1 and Y2) are connected to an error cancellation (EC) logic. It combines the two 1-bit inputs to a 6-bit output.

In this ΣΔ configuration the input signal (magnetic field B measured by the fluxgate sensor) gets delayed by four sampling periods. The quantization noise (E_2) generated by the quantizer in the second modulator ($Q2$) is shaped with fourth-order characteristics as well as the quantization noise generated in the first modulator ($Q1$) cancels out when the modulator is ideally tuned (Hartmann *et al* 2004). The difference equation of the error cancellation circuit is

$$Y = (Y_2 - Y_1 \cdot z^{-2}) \cdot (1 - z^{-1})^2 + Y_1 \cdot z^{-2} = B \cdot z^{-4} + E_2 \cdot (1 - z)^4. \quad (1)$$

The fluxgate sensor is modelled by its feedback factor S_{FB} (in nT $\mu\mathrm{A}^{-1}$) describing the feedback coil and by its sensitivity S_{SE} (in $\mu\mathrm{V_{rms}}$ nT^{-1} at $2f_0$) representing the pick-up coil and the summing node. The input amplifier is operated as a band-pass filter with a gain of G_{IA} at $2f_0$. The phase adjustable synchronous demodulator (ASD) of the model is a simple gain stage with G_{SD} equal to $2^{3/2}\cdot\pi^{-1}$ (inverted form factor). The feedback resistor R_{FB} sets the current through the feedback coil and thus determines the dynamic range.

On the chip, the combined ASD and first integrator (I1) stage is realized by a switched capacitor (SC-) integrator (Brandt *et al* 1997) with additional input switches (see figure 6) which build the ASD (running at $2f_0$). The ASD clocks (CMOD and CMODX) can be shifted by phase command to maximize the rectified output signal. Integrator 1 is running at a 32 times higher clock rate ($f_I = 16f_0 = 32f_S$ with alternate switching of CP1 and CP2) as normally required for a SC-integrator in such a modulator configuration. Here it is implemented for a proper integration of the rectified ASD output which contains the field relevant information at $4f_0$. This modification shifts the gain of the first integrator from normally

$$G_I = \frac{C_S}{C_I} \qquad \text{to} \qquad G'_{11} = \frac{f_I}{f_0/2} G_I = 32\, G_I. \quad (2)$$

To ensure fourth-order noise shaping (1) and good pattern noise rejection, the gain factors of the first and second stage have to be matched:

$$G_{11} = A_{\mathrm{VREF}} \frac{1}{R_{\mathrm{FB}}} S_{\mathrm{FB}} S_{\mathrm{SE}} G_{\mathrm{IA}} 2 \frac{\sqrt{2}}{\pi} G'_{11} = G_{12} = G_{21} = G_{22} = 0.5. \quad (3)$$

Here A_{VREF} is the ratio between the chip external and chip internal reference voltages (not shown in figure 5). It is 2 for MFA-1 and 1.6 for MFA-2. The gains G_{IA} and G'_{11}

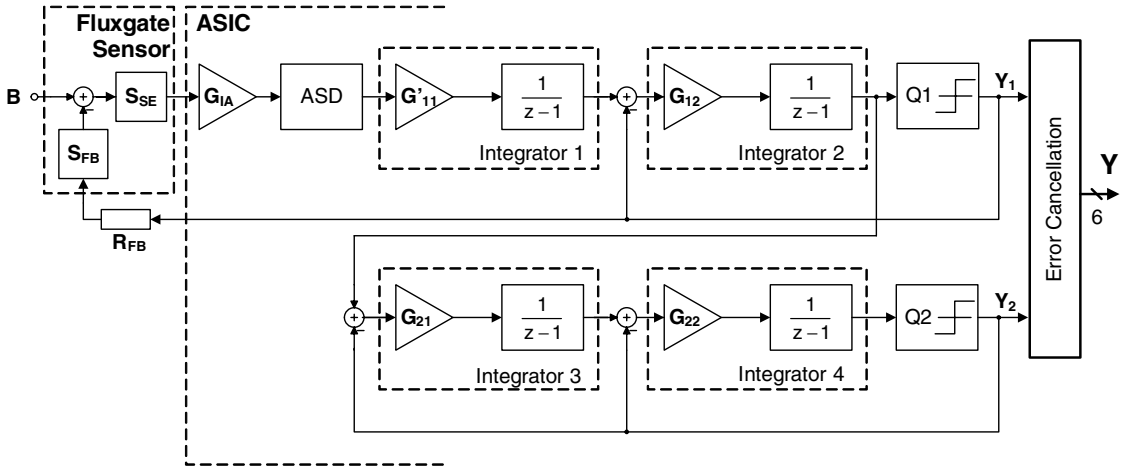

Figure 5. Linearized model of the modified 2–2 cascaded fluxgate modulator.

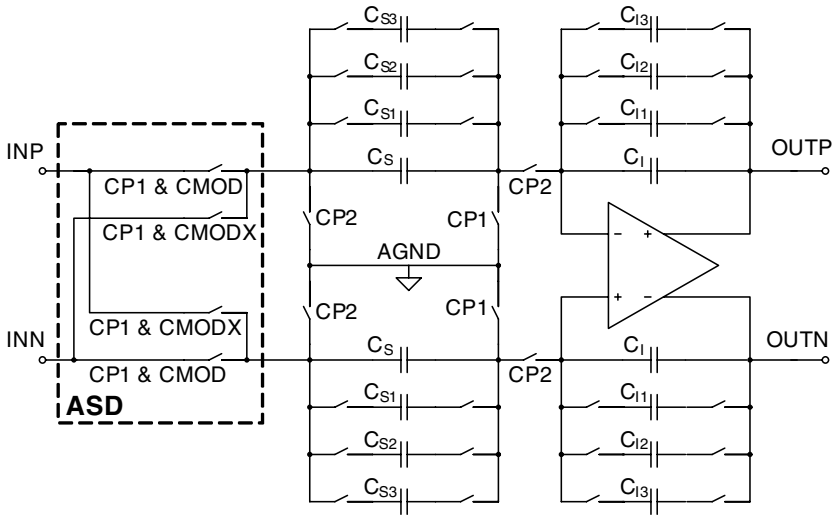

Figure 6. Switched capacitor integrator with an adjustable synchronous demodulator (ASD) and variable gain setting.

as well as the feedback resistor R_{FB} are adjustable. It allows adaption of the MFA to different fluxgate sensors and different dynamic ranges. R_{FB} and G_{IA} are set by external components and G'_{11} by switches in the capacitor network in figure 6. They are controlled by command. With a total sampling (C_S) and integration capacitance (C_I) range of 0.625–10 pF and 15–40 pF, respectively, 12 different gain settings from 0.5 up to 21.33 can be programmed. The gain factors G_{12}, G_{21} and G_{22} are fixed by precise capacitor ratios on the chip.

When tuning a new sensor setup (evaluation of the correct integrator 1 setting), the output voltage (root mean square) of the LNA at $2f_0$ (V_{LNA_RMS}) is measured when the external differential feedback voltage is set permanently high (+2 V) or low (−2 V), respectively, producing a full scale feedback field in the fluxgate sensor. The correct integrator gain setting can then be calculated with

$$G'_{11} = \frac{\pi}{8 \cdot \sqrt{2}} \cdot \frac{V_{REF\_INT}}{V_{LNA\_RMS}} = \frac{\pi}{8 \cdot \sqrt{2}} \cdot \frac{1.25}{V_{LNA\_RMS}}. \quad (4)$$

The correct gain setting can be visually checked when evaluating the increase of the quantization noise in the output data of the error cancellation (via the test bus). An 80 dB dec^{-1} increase (as shown for both curves in figure 10) confirms the correct tuning. A gain mismatch of G'_{11} by about 10% is indicated by the dashed line. It does not affect the SNR in the signal bandwidth which is limited to about 30 Hz by the primary decimation filter but it can amplify the amplitude of disturbing tones (also called pattern noise; see section 3.4) which are kept below the noise floor in the case of proper tuning and gain setting (Ledzius and Irwin 1993).

2.4. Correlated double sampling

Since one of the key problems of the MFA-1 is f^{-1}-noise caused by flicker noise in the CMOS input stage of the integrator 1 amplifier, correlated double sampling (CDS) has been implemented in the first integrators of all four MFA-2 channels (Enz and Temes 1997).

Figure 7 shows the basic principle of CDS. During the sampling phase (upper plot), C_{CDS} is charged to the current offset voltage of the amplifier so that exactly this value can be subtracted during the integration phase (lower plot). Sampling and integration alternate at 262.1 kHz which enables an

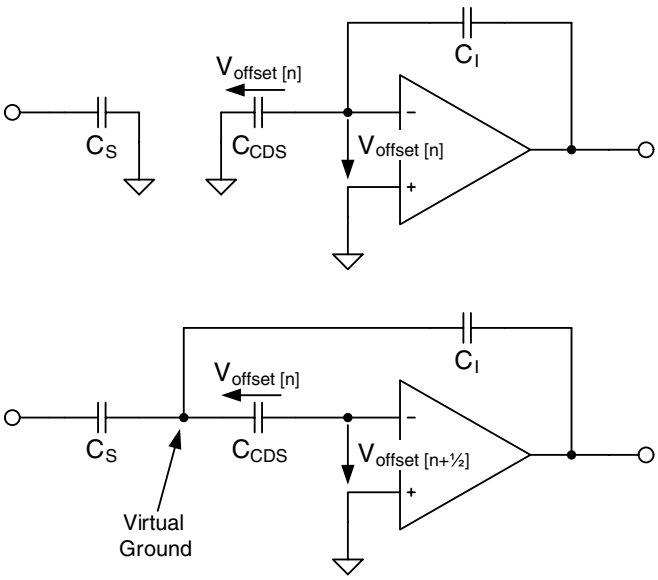

Figure 7. Principle of the correlated double sampling.

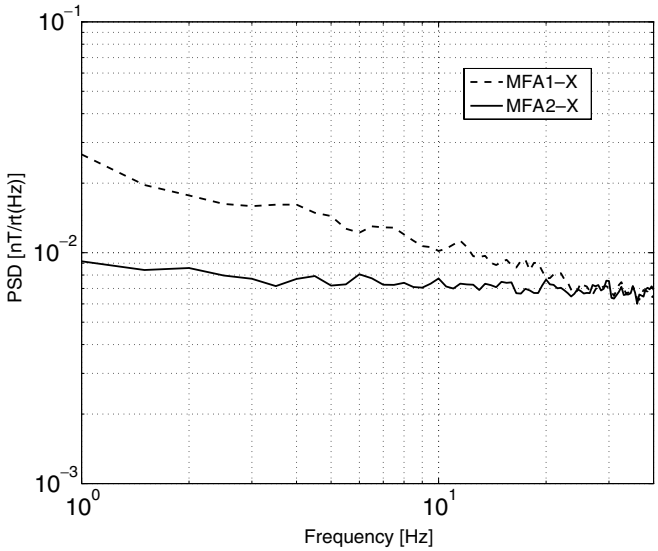

Figure 8. PSD of error cancellation output data from MFA-1 (without CDS) and MFA-2 (with CDS).

excellent cancellation of the f^{-1}-noise in the signal bandwidth. Two additional switches as well as a capacitor (C_{CDS}) were added to the switched-capacitor integrator, as already shown in figure 6. For proper operation of the CDS principle, the CDS capacitance must be as big as the maximum integration capacitance (i.e. 40 pF). The result is shown in figure 8.

The remaining f^{-1}-noise in the PSD of the EC output of the MFA-2 data is due to the intrinsic noise of the fluxgate sensor. This was proved by the fact that PSD measurements with the fluxgate channel configured in an external voltage mode (see below) showed flat noise down to less than 0.01 Hz.

2.5. Operating modes

The MFA can be operated in three different modes: field mode, external voltage mode and internal voltage mode. In all three modes, up to eight housekeeping parameters can be measured with the housekeeping channel, which always operates like a fluxgate channel in an internal voltage mode.

Field mode. The external feedback voltages and the chip internal adjustable synchronous demodulator (ASD) are active for proper measurement of the magnetic field with the three fluxgate channels. The dynamic range is set with chip external feedback resistors.

External voltage mode. The ASD is disabled per command for a classical ADC operation (digitization of voltages) of the three fluxgate channels using the chip external feedback voltages. The voltage range is flexible to some extent, and can be set with chip external gain setting (resistor ratios) at the LNAs.

Internal voltage mode. When pin VMMODEN is set high, the ASD is automatically disabled for a classical ADC (digitization of voltages) operation of the three fluxgate channels using the chip internal feedback voltages. They are connected to the first integrator of the first second-order modulator as in a classical modulator configuration. The voltage range is thus fixed to ± 1.25 V.

3. Performance verification and radiation tests

3.1. Test configuration

The final test bench set-up is shown in figure 9. It includes a support unit (MFA EGSE) containing a XILINX FPGA based interface adapter board as well as a separate power supply and opto-coupler board. The connection between the MFA EGSE and the host PC can be established via USB or Ethernet. A LabView software program manages the immediate or time tagged commanding of the MFA as well as the data visualization, processing and storage in real time. At the beginning all magnetic performance tests were done with the Engineering Model sensor of the magnetometer developed for ESA's Venus Express mission (Zhang *et al* 2006, Auster *et al* 2008; see figure 9). Later on, a prototype sensor developed by the Institute of Geophysics and Planetary Physics, University of California Los Angeles (UCLA) for the Magnetospheric Multiscale mission by NASA was used as well.

The MFA is soldered to the lower right top side of a 6×9 cm^2 wide test board. The board also contains the excitation circuit needed for the fluxgate principle (upper right), passive components for the band-pass configuration of the chip internal pre-amplifiers as well as feedback resistors (left to the MFA), an external voltage reference, jumpers for disconnecting the feedback during tuning activities and finally block capacitors for the MFA supply voltages. Three connectors establish the link to the MFA EGSE box (37-pin MDM; in a flight configuration less than 15 pins are needed), the fluxgate sensor (26-pin high-density SUB-D) and a 3D accelerometer sensor (9-pin MDM) which is measured via the housekeeping channel in this test set-up.

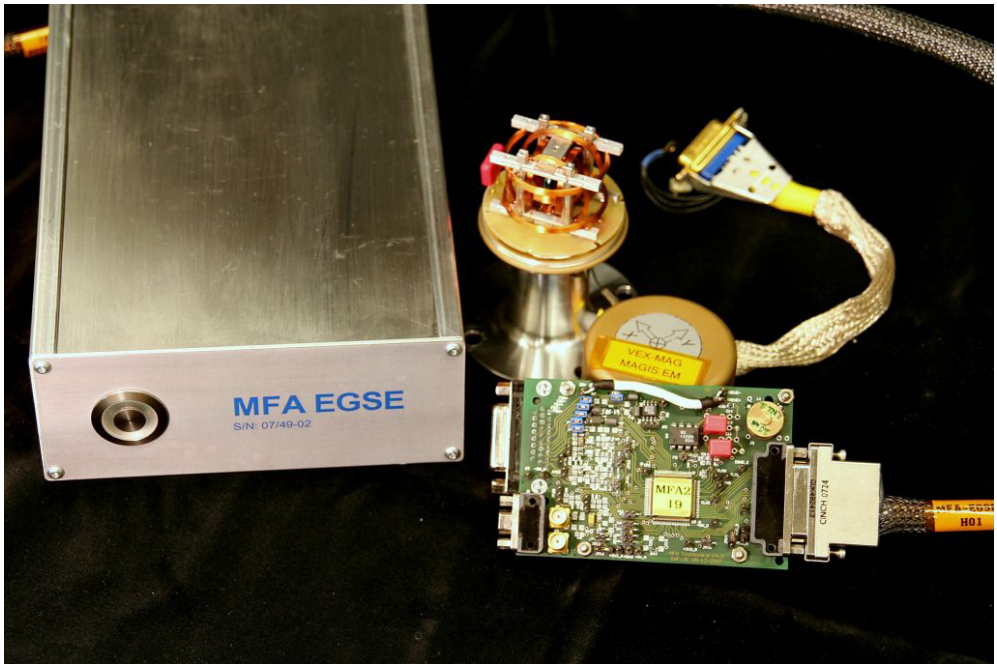

Figure 9. MFA test setup with a Venus Express sensor.

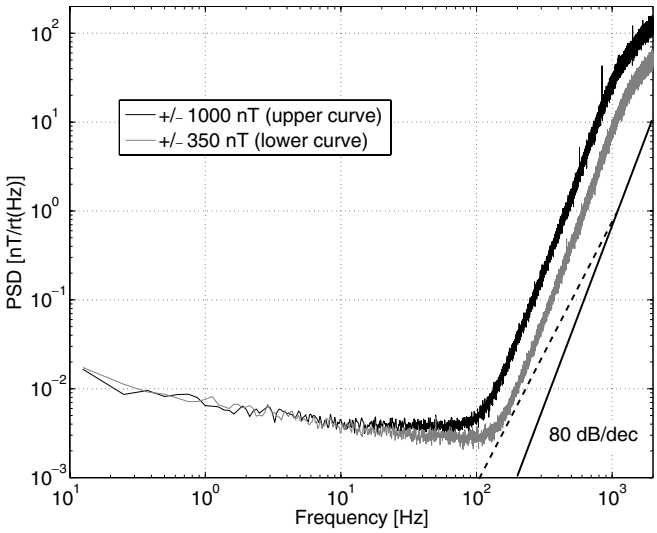

Figure 10. Power spectral density of error cancellation output data.

3.2. Performance tests

This section includes a number of spectra of the error cancellation output data (8192 Hz) which explain the noise and linearity performance of the fluxgate channels. The data still include the quantization noise of the 2–2 cascaded $\Sigma\Delta$ modulator which is digitally filtered by the primary decimation filter.

Figure 10 shows the power spectral density (PSD) of one of the fluxgate channels which is ideally tuned (80 dB per decade noise increase above 100 Hz) for dynamic ranges of $\pm$1000 nT (upper black curve) and $\pm$350 nT (lower grey curve), respectively. Both curves illustrate the superposition of altogether three noise sources. The f^{-1}-noise below 10–40 Hz, independent of the dynamic range, is the intrinsic noise of the fluxgate sensor. Above 70–100 Hz, the noise shaped quantization noise of the fourth-order $\Sigma\Delta$ modulator is dominant (the difference in the quantization noise levels is proportional to the difference in the dynamic ranges). In between, a relatively small white noise band is caused by the input stage of the first integrator and the value of the sampling capacitance (C_S). The root of C_S has an indirect proportional influence on how much thermal noise of the switches is kept within the bandwidth of the modulator (Brandt *et al* 1997). A higher C_S is configured for the lower range (more gain at integrator 1 is needed since less field signal is fed back into the sensor) which automatically decreases the white noise roughly by the root of the ratio of the dynamic ranges.

The measurements were performed with the MFA connected to the prototype MMS sensor. It uses ring-cores with a diameter of 1 inch which enables a noise density of 7–8 pT Hz$^{-1/2}$ at 1 Hz and 4 pT Hz$^{-1/2}$ at 10 Hz.

Figure 11 compares the PSD of the short circuited housekeeping channel (lower black curve) with one of the fluxgate channels when tuned for a dynamic range of $\pm$4000 nT (upper grey curve). Here the unit full scale (FS) per root hertz is used in order to enable a direct comparison of voltage and magnetic field measurements (the dynamic range is $\pm$FS). The noise floor of the field curve (3–4 μFS Hz^{-1} corresponds to 12–16 pT Hz^{-1}) is not dominated by the sensor noise any more. It is now caused by the MFA internal noise, has mainly white noise characteristics and is about a factor of 1.5 higher than that of the housekeeping channel. Taking into account that for $\Sigma\Delta$ modulators the maximum signal-to-noise ratio (SNR) is reached for a sine input signal with a root mean square (RMS) value of FS$\cdot 2^{-3/2}$, the calculated SNR of the housekeeping channel is 91 dB for a bandwidth of 30 Hz (corner frequency of the implemented primary

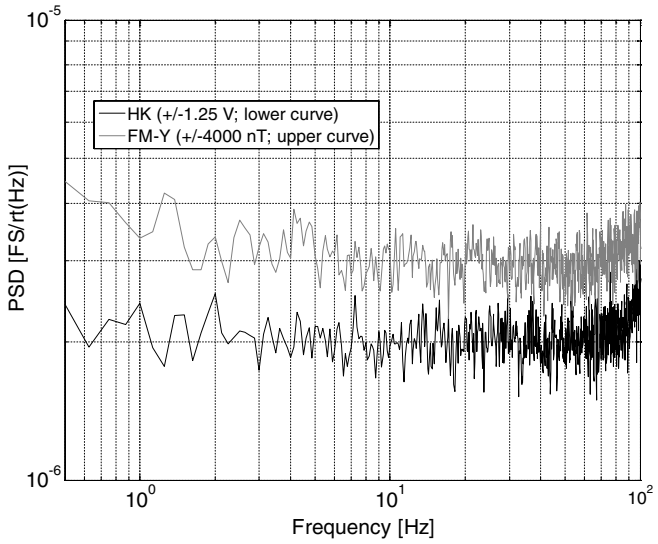

Figure 11. Comparison of the error cancellation output noise floor in field and voltage modes.

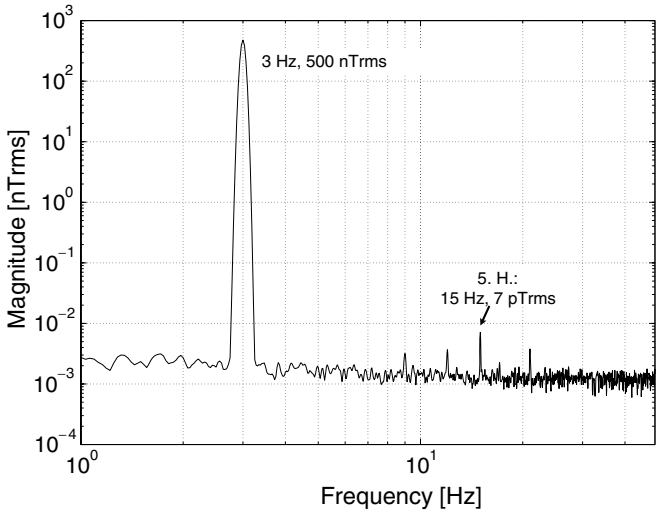

Figure 12. Total harmonic distortion.

decimation filter). Thus, the SNR of the field channel is about 88.5 dB. But, as also outlined in figure 12, for a field channel operation in a ±1000 nT range, the RMS value of the input field can be of the order of FS·2^{-1} without a significant increase of higher harmonics in the output spectra which allows for a definition of the SNR of > 89 dB for a signal bandwidth of 30 Hz (128 Hz output data). The increase of SNR with further filtering and data decimation in the secondary filter stages is very much dependent on the f^{-1}-noise characteristics of the fluxgate sensor.

The total harmonic distortion of the measurement in figure 12 is 94.4 dB, when taking into account all visible higher harmonics.

Figure 13 shows the output of the field channels (a dynamic range of ±1000 nT) in the upper plots during temperature cycling between −7 °C and +39 °C, as shown in the lowest. The fluxgate sensor was located in a reduced field environment in order to make just the offset drift dominant

Table 1. Configuration of the MFA-2 channels during irradiation.

Channel	G_{IA}	G_{INT}	I_{FB} (mA)	Range (V)
X	0.5	0.5	0.125	±7.75
Y	0.425	0.66	0.062	±2
Z	0.13636	2	0.062	±2
HK	N/A	N/A	N/A	±1.25

during the temperature cycling. There is a slight temperature proportional offset drift visible in all components which is in *Y* superposed by a drift of about 0.15 nT. This is most probably caused by a drift of the magnetic shielding can, in which the fluxgate sensor was placed during the test (see also below). The offset drift is less than 0.18 nT during the cycling of the MFA temperature by about 46 °C which gives a maximum offset drift of less than 4 pT °C^{-1}. The offset drift of the housekeeping channel with short circuited input was proved to be less than 0.1 μV °C^{-1}.

A large number of temperature tests was performed in order to study the drift of the static external feedback voltages with different load conditions. It can be summarized that the external differential feedback voltage of the MFA-2 shows a drift of approx. 60 ppm °C^{-1} without any load, about 85 ppm °C^{-1} at 0.4 mA and 200 ppm °C^{-1} at 2.9 mA, respectively. It was also evident that in comparison to the used external reference voltage (<4 ppm °C^{-1}) the chip internal one can either improve or deteriorate this effect with its own drift since it varies a lot from chip to chip. Figure 14 shows the resulting gain drift for the *X* component in the upper plot (a dynamic range of ±1000 nT is generated with a feedback current of ±55 μA). An artificial field of about 500 nT was applied along the *X* component, which shows almost no offset drift in figure 13, in order to make just the gain drift visible. It is −61 ppm °C^{-1} with external and −72 ppm °C^{-1} with internal reference voltage. The difference in *Y* (offset drift measurement) with external and internal voltage reference is due to a slightly different sensor position in the magnetic shielding during these two tests. The difference in *X* (gain drift measurement) is caused by the difference of the reference output voltages.

A 10.5 day long measurement (100 s mean values) with the MMS prototype sensor is depicted in figure 15. The sensor was placed in a three-layer magnetic shielding can with a shielding factor of about 30 000. The maximum variations around the mean values are ±0.15 nT in *X* and ±0.2 nT in *Y*. The remaining variation over such a time frame cannot easily be separated from the remaining drift of the shielding can itself which is of the order of 0.2 nT °C^{-1}. The cyclic temperature variations of the sensor and electronics are due to the temperature regulation in the laboratory during working days.

A summary of the performance characteristics and resource requirements is given in tables 2 and 3.

3.3. Radiation tests

Altogether four radiation tests—three total ionization dose (TID) tests using a Co-60 facility and one single event effect

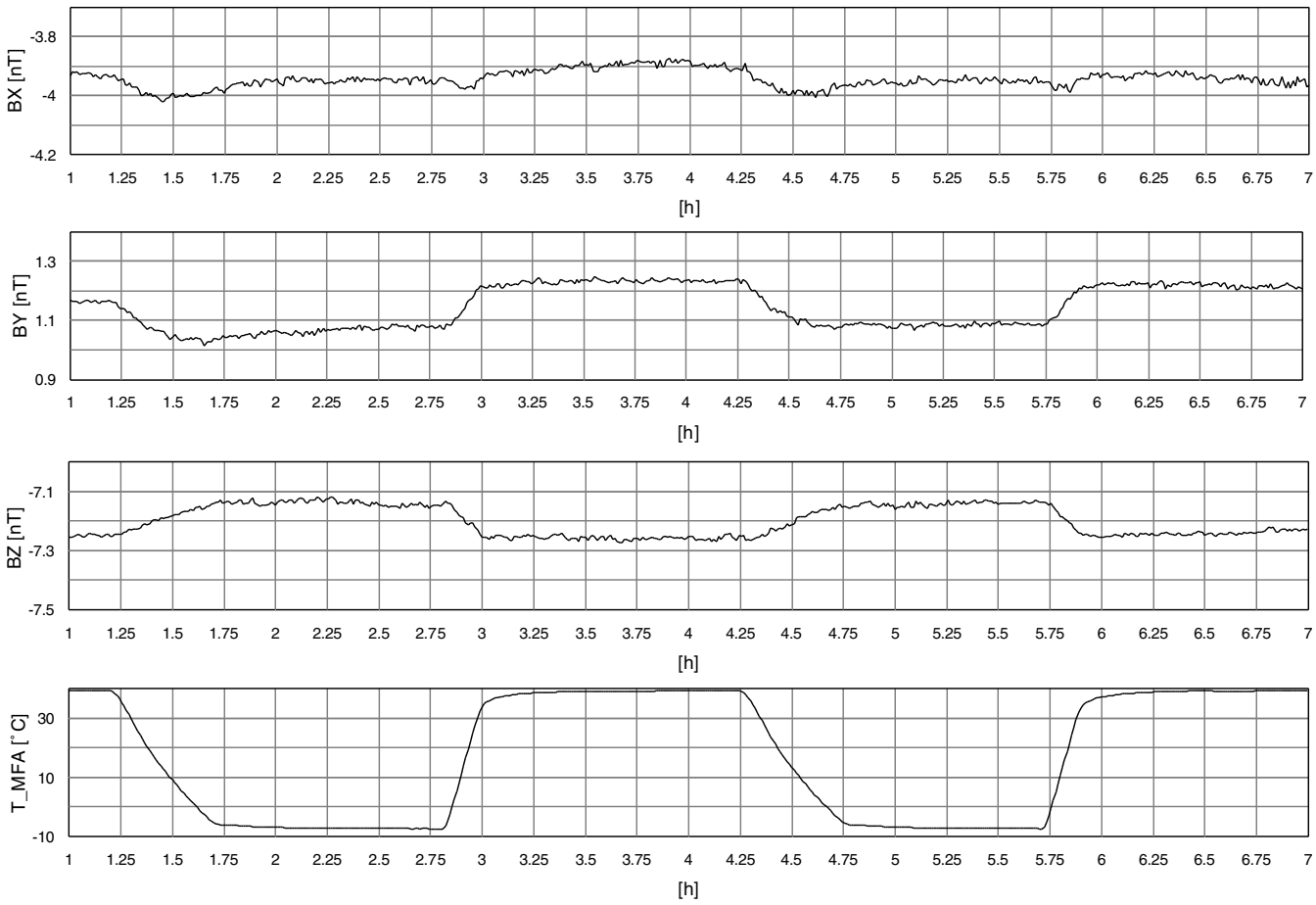

Figure 13. Offset drift of fluxgate channels with MFA temperature.

Table 2. Performance characteristics of MFA-2.

Total dose hardness:	Full specs: $<$ 170 krad
	Functional: $>$ 300 krad
Single event latch-ups:	$>$14 MeV cm^2 mg^{-1}
Field mode	
Dynamic range (128/2 Hz):	92/$>$103 dB ($<\pm$60 000 nT)
SNR (128/2 Hz):	89/$>$99 dB
Internal voltage mode	
Dynamic range (128/2 Hz):	98/114 dB ($\pm$1.25 V differential)
	92/108 dB ($\pm$0.625 V single-ended)
SNR (128/2 Hz):	91/107 dB ($\pm$1.25 V differential)
Digital resolution:	23 significant bits
Offset stability—field mode:	$<$5 pT °C^{-1} MFA temperature
	$<\pm$0.2 nT within 250 h
Gain stability—field mode:	60 ppm °C^{-1} ($\pm$1,000 nT dynamic range)

Table 3. Resource requirements of MFA-2.

Supply voltage:	3.3 V digital
	3.5 V analogue
Power consumption:	10 mW digital
	50 mW analogue
	60 mW total
PCB area:	$<$ 7 $\times$ 6 cm^2
Data interface:	TLMH channel: 128 Hz
	TLML channel: 2, 4, 8, . . . , 128 Hz

(SEE) test—were performed with MFA-1 and -2. Here only the third TID and the SEE tests are described since these two tests cover the most important results.

The primary goal of the third TID test, performed with MFA-2, was to define possible loss of SNR during the first few krads of irradiation. The secondary goal was to characterize the MFA-2 chip up to the maximum TID which could be achieved during the test campaign. The test board used for the test was set up in the so-called external voltage mode which means that the fluxgate channels were used as voltage ADCs but with external feedback. It turned out that no measurable effect in terms of SNR drop up to 26 krad was noticeable during irradiation with a low dose rate (4.8 rad min^{-1}). As far as the secondary goal is concerned, a decrease of SNR was observed with higher TID levels caused by increasing f^{-1}-noise at frequencies below 2–3 Hz (see the X component in figure 16). The power consumption of the chip was almost constant (change $\sim$1%) throughout the test. All four tested channels showed exactly the same f^{-1}-behaviour independent of their different gain and feedback settings (see table 1), which has led to the conclusion that the correlated double sampling performance (leakage currents in the switches) was affected by the irradiation. A performance test after 10 days unbiased annealing at room temperature

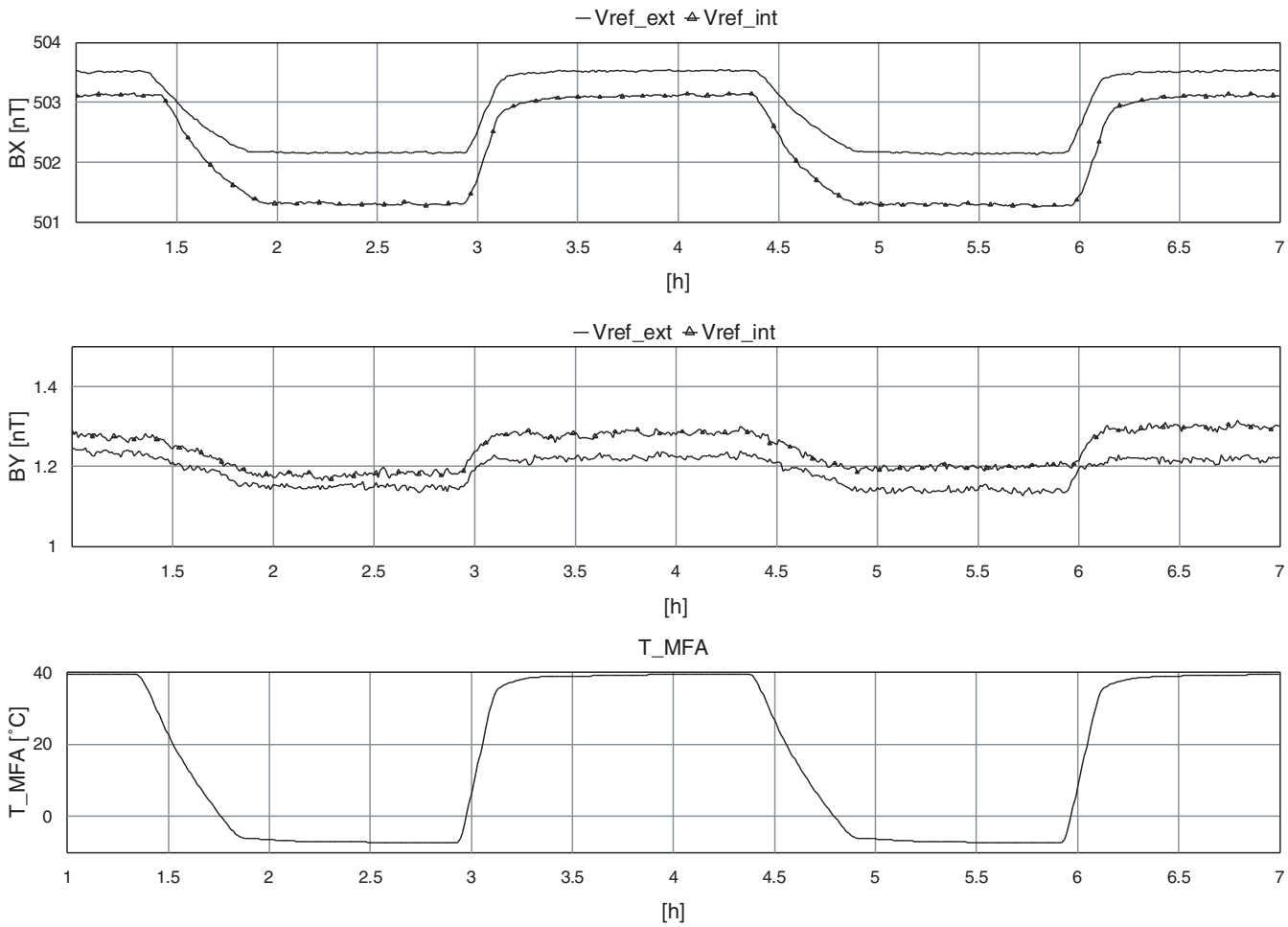

Figure 14. Gain drift of fluxgate channel X and offset drift of fluxgate channel Y with MFA temperature and external and internal voltage reference.

showed that the f^{-1}-noise increase suffered from 299 krad TID had totally disappeared. The chip itself was fully functional during the TID test and never showed any kind of malfunction.

The SEE test with MFA-1 revealed a susceptibility to latch-ups with a linear energy transfer of more than 14.1 MeV cm^2 mg^{-1}. A correct saturation cross-section could not be determined during the test, but it can be estimated to be between 10^{-3} and 10^{-4} cm^2 per device. An offline comparison of all available test data showed that only one real analogue latch-up appeared. All others occurred in the digital part of MFA-1.

3.4. Tone investigation

During testing it turned out that the spectrum of the modulator outputs can include unexpected spectral peaks (also called tones and pattern noise). The existence of tones in $\Sigma\Delta$ modulators (especially when of lower order) is well described in the literature (Norsworthy 1997). Some of the tones occurring in the MFA system are known (defined as tones 1a and 1b below) but the others (tones 2a, 2b and 3) appear only in this current $\Sigma\Delta$-fluxgate configuration, especially when two or three channels are operated in parallel.

With the equations given below it is possible to calculate the exact frequency of all tones, while it is not possible to calculate their amplitudes (f_S is the sampling frequency of the modulators and half of the excitation frequency at the same time, the dynamic range is defined as $\pm$FS, $\mathrm{dc}_{\mathrm{in}\_c\alpha/\beta}$ is the dc input value of channel α/β and FS_$c\alpha/\beta$ is the full scale value of channel α/β of two interfering channels):

$$f_{\mathrm{tone1}a\&3} = \frac{|\mathrm{dc_{in}}|}{\mathrm{FS}} \cdot f_S,\ f_S = f_0/2 = 8196\ \mathrm{Hz} \tag{5}$$

$$f_{\mathrm{tone1}b} = \left(1 - \frac{|\mathrm{dc_{in}}|}{\mathrm{FS}}\right) \cdot \frac{f_S}{2} \tag{6}$$

$$f_{\mathrm{tone2}\_a,\_b} = \left|\left(\frac{\mathrm{dc}_{\mathrm{in}\_c\alpha}}{\mathrm{FS}\_c\alpha} \pm \frac{\mathrm{dc}_{\mathrm{in}\_c\beta}}{\mathrm{FS}\_c\beta}\right) \cdot \frac{f_S}{2}\right|. \tag{7}$$

The spectrum of the Y-channel in figure 17 shows almost all the tones. It is an averaged FFT of about 2 min of error cancellation output data and it was measured with the fluxgate sensor in the magnetic shielding which means that the dc field was constant for the measurement period. Only tone 1a is not visible since its amplitude is well below the electronics noise for low dc input values when the modulator is correctly tuned. In the plotted configuration it is also hidden by the existence of tone 3. Tone 1b sits on top of the quantization noise on the

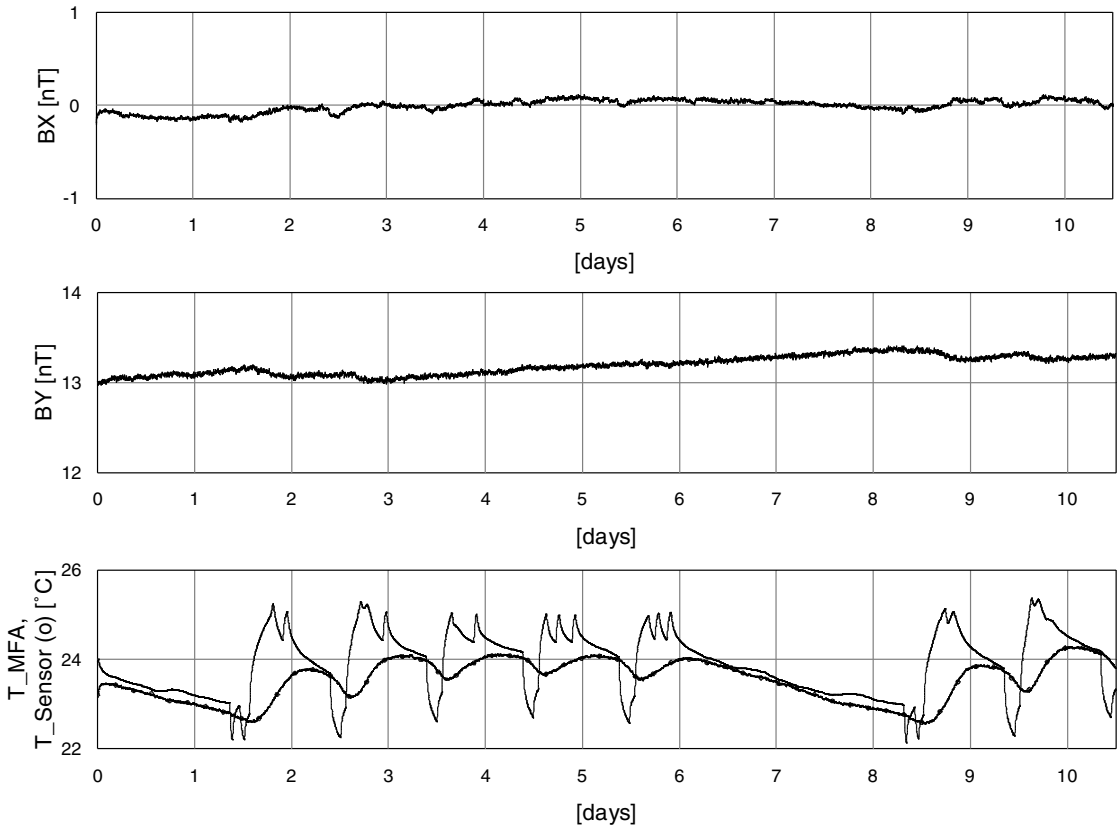

Figure 15. Long-term stability.

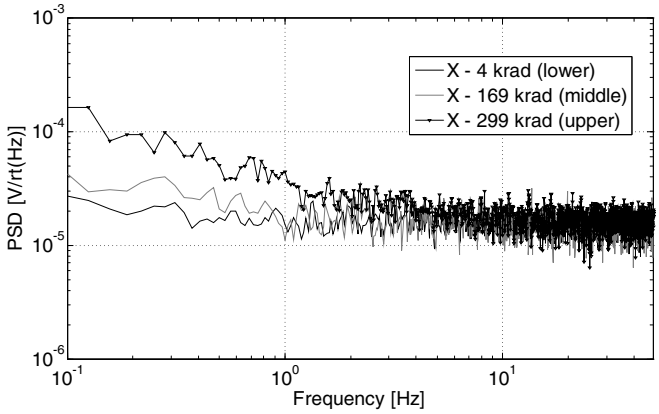

Figure 16. PSD plot of X-channel error cancellation output with short circuited input during irradiation.

far right side of the spectrum, while the tone 2 pairs caused by the interference with the two other channels are visible at frequencies as explained in figure 17.

The amplitudes of tones 1a and 1b are products of a remaining periodicity in the single-bit output of the first 2–2 cascaded modulator and thus shaped like the quantization noise, which means their amplitudes get lower towards lower frequencies. Tones 2a and 2b are generated by interference between the channels. In the case where all three channels are operational as in figure 17, each axis sees two pairs of tone 2 tones caused by the interference with the other two channels. Tone 2 as well as tone 3 amplitude is not shaped, which indicates that the interference occurs in the feedback or the input stage of the system. They stay constant over the complete frequency range and can be in the worst case 5×10^{-4} of FS. The tones are, therefore, clearly visible below 100 Hz and get hidden by the quantization noise above.

The occurrence and amplitude of tones 2 and 3 are dependent on the phase relation between the sampling clock of the modulator (CLKS), which at the same time determines the polarity of the feedback voltages, and the clock with which the first integrator is operated (CLKI). The phase of both clocks is programmable in order to keep full flexibility for the tuning of the fluxgate set-up.

Tone 3 in the external voltage mode is only generated when the negative edge of CLKI (transition from integration to sampling phase) occurs one or two master clocks past the rising edge of CLKS. In this phase configuration the change in feedback polarity disturbs the integration phase at the first integrator of the same axis at the very last moment which is causing a tone 3 error dependent on dc_{in}. The frequency of tone 3 is proportional to $fs \cdot \mathrm{FS}^{-1}$ (5). A tone 2 pair is generated when the above-mentioned phase relation occurs in two different channels (e.g. CLKIy and CLKSx). The frequency dependence of tone 2 (7) is proportional to $fs \cdot (2 \cdot \mathrm{FS})^{-1}$ as for tone 1b (6). This fact has led to the conclusion that an intermediate inter-channel tone 3 is generated which is below the common noise floor but mixes with the very big tone 1b at, e.g., the non-linearity of the first integrator and so becomes visible. The error configuration has been reproduced exactly in a Matlab Simulink model. While in EVM tones 2

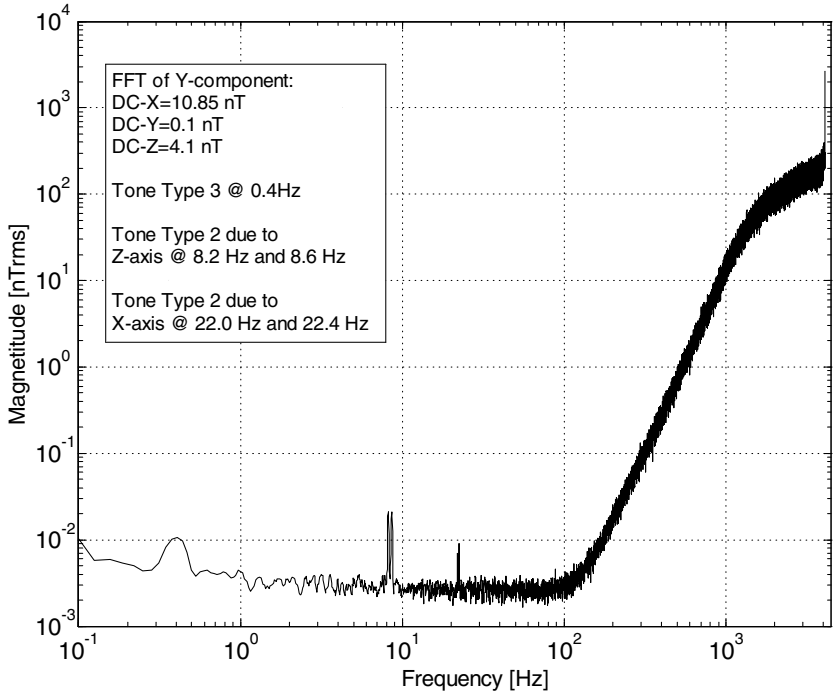

Figure 17. Spectrum of *Y*-channel error cancellation output with tones.

and 3 are only generated at very specific phase relations of CLKI and CLKS, it is different for the field mode. Here the amplitude of those tones is a sine function of the CLKS phase when the phase of CLKI is kept constant at the same time. This fact is linked to the fluxgate principle and not further discussed here. But with the flexibility in the phase setting the tone amplitudes can at least be kept below 10^{-5} of FS. For comparison, the biggest tones in figure 17 have an amplitude of 2×10^{-5} of FS.

4. Discussion

It was the major goal of the described undertaking to develop a radiation tolerant mixed-signal ASIC which includes the active readout electronics for a triaxial fluxgate sensor and which features the performance of conventional designs. Briefly speaking, this aim has been achieved. With two different fluxgate sensors it was demonstrated that the overall functionality and performance of the MFA are sufficient for a scientific application aboard planetary and inter-planetary missions. The developed magnetometer front-end ASIC includes all active circuits needed for the read-out and digitization of the magnetic field vector measured via a fluxgate sensor. Furthermore, all additionally required calibration parameters such as sensor and electronics temperature can be measured with the included housekeeping channel.

The noise performance and offset stability of the MFA-2 are very satisfying (see table 2). Offset stability is an important parameter for a fluxgate magnetometer. An absolute accuracy of the order of ± 0.1 nT is required for many space missions and so with a stable fluxgate instrument too frequent in-flight calibration sequences can be avoided.

The remaining gain drift is acceptable. Due to its linearity and the automatic temperature measurement within the chip it can be calibrated without much additional effort. Only the existence of the described cross-tone phenomenon is something that must be corrected in future designs even though also this drawback can, with certain phase settings, at least be mitigated to a level that is tolerable. Highest tone amplitudes are then 100 dB below full scale and are only measurable when the dc magnetic field does not change more than ± 0.1 nT within a minute and the spectra are calculated and averaged over a similar time period.

In terms of total ionization dose, the process can be declared as radiation hard (300 krad), but the threshold for latch-ups with 14 MeV cm^2 mg^{-1} (mainly a problem of the digital part of the ASIC) is, in principle, not sufficient, especially for missions where high energetic particles are of major concern. However, for a number of missions, e.g., to the terrestrial planets Venus, Mars and Mercury as well as for Earth missions which do not orbit through the radiation belts, the MFA can be used with a quite simple chip external latch-up protection circuit.

As far as miniaturization and power consumption are concerned, it was possible to reduce the power required for the readout electronics of a fluxgate sensor at least by a factor of 8 and the required PCB area by a factor of 4–5 (see table 3) compared to, e.g., magnetometers aboard Messenger (Anderson *et al* 2007), Themis (Auster *et al* 2008) and Rosetta Orbiter (Carr *et al* 2007).

Two other miniaturized fluxgate magnetometer designs have recently been published by O'Brien *et al* (2007) and Forslund *et al* (2008). Both rely on laboratory set-ups with commercial components which makes comparison difficult.

5. Outlook

The magnetometer front-end ASIC in combination with a fluxgate sensor developed by the Institute of Geophysics and Planetary Physics, UCLA is selected to measure aboard the four-satellite mission Magnetospheric Multiscale (MMS) by NASA. For this reason, a final re-design and the space qualification of the MFA is going to be funded in the frame of the Austrian Space Application Programme (ASAP). MFA-3 will be very much based on the MFA-2 design. Further improvements in functionality and performance should be reached with (a) a separate pair of feedback buffers (with 3.3 V supply instead of 3.5 V) for each fluxgate channel to avoid cross tone effects, (b) a further reduction of parasitic resistances in the feedback circuit to decrease gain drift effects, (c) synchronization of the data acquisition to an external 1 Hz pulse which is provided synchronously to the master clock and (d) programmable data filtering and differentiation in the primary decimation filter in order to get a flexible corner frequency (30 and 60 Hz).

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