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A Timing Synchronizer System for Beam Test Setups requiring Galvanic Isolation

L. Meder, D. Emschermann, J. Frühauf, W. F. J. Müller, and J. Becker

***Abstract*—In beam test setups detector elements together with a readout composed of frontend electronics (FEE) and usually a layer of Field Programmable Gate Arrays (FPGAs) are being analysed. The FEE is in this scenario often directly connected to both the detector and the FPGA layer what in many cases requires sharing the ground potentials of these layers. This setup can become problematic if parts of the detector need to be operated at different high-voltage potentials, since all of the FPGA boards need to receive a common clock and timing reference for getting the readout synchronized. Thus, for the context of the Compressed Baryonic Matter (CBM) experiment a versatile Timing Synchronizer (TS) system was designed providing galvanically isolated timing distribution links over twisted-pair cables. As an electrical interface the so called timing DPB (tDPB) FPGA Mezzanine Card (FMC) was created for being mounted onto FPGA-based Advanced Mezzanine Cards (AMCs) for mTCA.4 crates. The FPGA logic of the TS system connects to this card and can be monitored and controlled through IPBus Slow-Control links. Evaluations show that the system is capable of stably synchronizing the FPGA boards of a beam test setup being integrated into a hierarchical TS network.**

***Index Terms*—Digital circuits, Timing electronics, FPGA, Digital signal processing.**

I. Introduction

DETECTOR elements operated with preproduction setups of readout chains are analysed during beam tests.

Usually, the readout chain operated during a beam time is composed of different kinds of processing boards, equipped with FPGAs, general purpose Integrated Circuits (ICs) and custom readout Application-Specific ICs (ASICs) for the different detectors. Besides the high speed fiber links transferring the data recorded by the FEE from the FPGA layer to a post-processing system, it is also important to provide means in order to control the readout system. For the overall system control a slow-control system can be used like the IPBus system [2] developed at CERN.

However, in many readout systems it is important that at least the FEE that samples the signals from the detector is operated with a clock of common frequency. Also it is usually required to have a global time reference or trigger for the FPGA layer which will need to package the data stream and add some kind of timestamp so that the post-processing will be able to analyse it as a coherent data set later on.

For that reason, a timing control system is required which distributes a clock and a synchronization signal from a central master to the slave nodes that connect to the FEE. In case of a pre-series beam test setup of the CBM Silicon Tracking System (STS) which uses the CBM nXyter chip [3], the detector elements together with the readout ASICs are dircetly interfaced to the FPGA layer with DC-coupled connections. Firstly this relaxes the jitter requirements of the distributed clock to about 150 ps peak-to-peak (pk-pk) since no synchronous high speed fiber links are used in the prototypical detector readout that require this clock as a reference source as it will be the case for the final CBM readout system. However, the detector elements need to be operated at bias potentials of usually +/- 150 V [4] for the p- and n-side respectively which causes large voltages between the ground potentials of the two groups of FPGA-based p-/n-side readout chains (see Figure 1). Thus, all of the control and data links to these processing nodes require a galvanic isolation in order to prevent damage from the connected electronics.

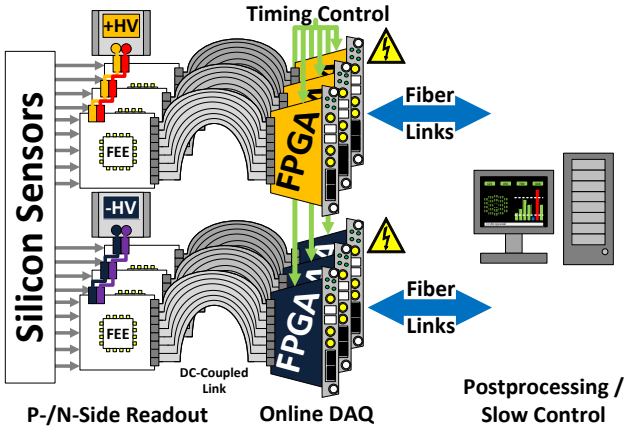

Fig. 1. Readout with DC-Coupled FEE for the example of Silicion Detectors

Taking into account all of these requirements, a versatile FPGA-based point-to-multipoint TS system was developed which allows to provide a common clock and synchronization information to the slave nodes.

The remainder of this article is organized as follows. In Chapter II the work presented in this article is set into the context of work from the literature. The design of the TS system is detailed in chapter III and it is evaluated in chapter IV. The article closes in chapter V with the conclusion.
The work of this article has been presented at the 20th IEEE Real Time Conference, 2016 in Padova, Italy. An extended abstracted is available as part of the conference record [1].

II. Related work

For the final version of the readout system of CBM it is planned to have a fully integrated Timing and Fast-Control

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(TFC) system. Here, timing information will be provided to the Slaves in order to allow them to autonomously adjust their system frequency and get into a known phase alignment relative to the Master. Since this system is currently under development and larger pre-series readout systems will be operated during beam times, the concept for a preliminary timing system was created which will allow a short development time and is easy to integrate into FPGA-based detector readout systems. During the concept phase of the TS system different available timing systems were taken into account.

The current state-of-the-art solution regarding its precision of timing synchronization is the White Rabbit system [5]. It is based on custom synchronous Ethernet switches using 1 Gigabit fiber links as transmission medium. The reason for its high performance is that it uses voltage controlled crystal oscillators (VCXO) at the nodes together with a Phase Locked Loop (PLL) being partially implemented in the software of a microprocessor and logic resources of the FPGA. Synchronization messages are exchanged over bidirectional fiber links which results in very balanced Upstream/Downstream latency ratios. By using a very linear and precise phase offset determination approach (digital dual-mixer time difference [7], [8]) it is possible to accurately control the PLL but also generate time-stamps with very fine resolution in the range of picoseconds. This approach offers a very good solution for synchronizing test beam setups since it also incorporates the required galvanic isolation due to the fiber links. However, it requires a relatively high integration effort because of the microprocessor-based soft-PLL required for tuning the VCXOs. Nevertheless, its core components are a good basis for the development of the future TFC system.

In the Belle II experiment a completely different approach is followed. Here, category (CAT)-7 twisted-pair cables are used to transmit clock and trigger information to the Slave nodes [6]. Compared to the White Rabbit system, a buffer-based approach is applied where custom FPGA boards are used for transmitting timing information over several RJ45 links. At the receiving end, a clock jitter cleaner (Texas Instruments CDCE62002 [9]) is used in order to improve the signal quality of the received uplink clock which is both used locally and forwarded to the next layer of buffer-boards and finally the frontends. In this system, compared to White Rabbit, no feedback loop is present because slow drifts of the clock are being calibrated by an offline analysis.

For the development of the TS system the Belle II timing distribution offers many very useful conceptual inputs. Using twisted-pair cables with cheap commercial-off-the-shelf (COTS) Ethernet connector components allows a simple integration into an interfacing Printed Circuit Board (PCB) of the TS system and the detector-specific ones. Also this approach will only require FPGA logic cores of modest complexity, since general purpose input output-based (GPIO) electrical interfaces may be instantiated which are operated at a rather low input/output (I/O) frequency compared to the High-Speed Transceivers required for the White Rabbit system. In contrast to the way it was done in Belle II, for the TS it is advantageous to rather design small daughter boards than a completely new platform because special pre-series readout FPGA AMCs are available. As there are currently no globally frequency locked high speed fiber links required towards the frontend, the clock jitter cleaner ICs are going to be omitted in favour of a less complex and more general PCB design.

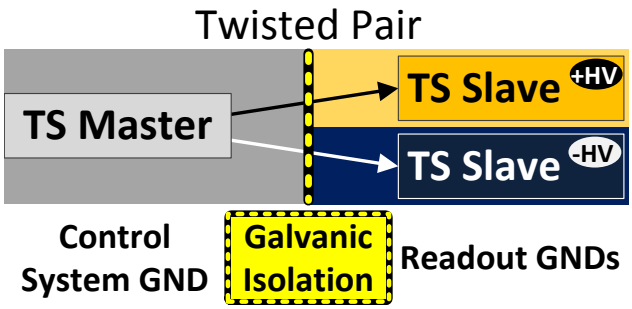

Fig. 2. Principle of galvanically isolated TS nodes

III. Design of the Timing Synchronizer System

As previously mentioned, the central need which lead to the development of the TS system of this article was to be able to synchronize the prototypical detector readout of a beam test setup at the FPGA layer where the FPGA nodes may be on different ground potential (see Figure 2). In case of the beam test readout of the CBM experiment, different ground potentials are required when using the legacy silicon detector frontend ASIC which needs to be connected through a DC-coupled data and control link. When being interfaced to the p- and n-side of the silicon sensors their +/-HV operating potential needs to be propagated through the FE boards up to the FPGA layer which causes a large potential difference between the grounds of these two groups of readout FPGAs. In order to avoid shorting the offset grounds and damaging the electronics, special care needs to be taken when designing the TS Link in order to guarantee an isolation of the control system ground domain from the readout nodes.

For the readout, AMC FMC Carrier Kintex (AFCK) FPGA boards are being used which provide two FMC connectors for daughter cards. In order to be able to connect this kind of FPGA boards through galvanically isolated links, a custom interfacing card was developed. Since the TS system's endpoints at the Slave side will be part of the FPGA-logic of the readout, it was decided to also integrate the logic of the Master side of the system into FPGAs and preferably also use the same boards as they are being used for the readout.

In the following subsections the developed TS system is detailed. First, the timing Data Processing Board (tDPB) FMC card is introduced in section III-A, afterwards the Hardware Description Language (HDL) design of the TS FPGA logic cores (section III-B) and the IPBus control software for the nodes of a laboratory setup is described (section III-C).

A. Design of the tDPB FMC Card

In CBM, custom FMC cards are created which provide the connections between the electronics to be evaluated during beam times. For the readout AMCs, detector-dependent cards need to be designed which house connectors for the different

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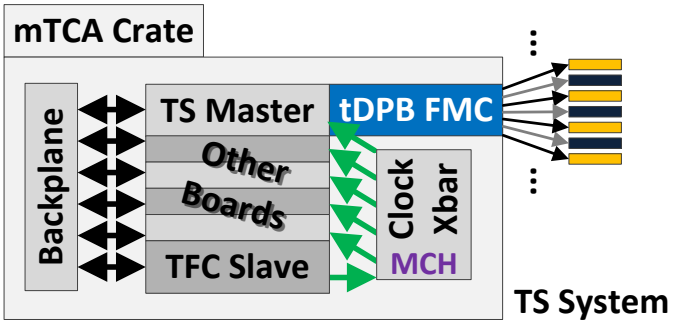

Fig. 3. Future setup where the TS system is interfaced to a mTCA crate based readout structure being synchronized by the TFC system

interfaces towards the frontend boards and also an interface for the Slave side of the TS system. In this chapter, the card is described which was developed as the TS Master interface, the so-called tDPB FMC (see Figure 4).

When considering both the design of custom PCBs and the simplicity of the FPGA-logic, as mentioned in section II, it was decided to not use a fiber-based TS link. Since the integration of fiber links in general requires an higher effort at the PCB side because of the needed optical transceiver components, the fiber medium would have to offer a significant advantage compared to using copper links to provide a reason to use this alternative transmission medium for the TS system.

In order to both transmit a clock and time base information to the Slaves over an optical link, several fibers or a procedure to derive a high quality clock signal from the data link are required. The usual way to extract clock signal from a serial stream when using commercial FPGAs is to use high speed transceiver primitives which are available at these ICs. However, these transceivers are used in CBM for the detector readout in order to transmit measurement data to the servers for post-processing. Moreover the synchronization system does not require the high data rates being offered by these transceivers but a simple way of sharing a common clock and time reference among the communication nodes. Also providing electrically isolated links does not make it necessary to use a fiber medium since the isolation may also be implemented by using a set of transformers in combination with twisted-pair copper cables. Because of these reasons a copper-based link was chosen in favor of a reduced system complexity.

In contrast to the readout FMCs, at the Master side the number of TS link interfaces is maximized in order to be able to connect a large number of readout nodes. On the other hand it was regarded as important during the concept phase of the TS system, to be able to use these cards in larger readout systems in the future where the TS Master can interface an mTCA.4 crate based system to the readout boards operated on different HV-potentials (see Figure 3).

To support this option, the maximum acceptable size of the card needs to be taken into account which still allows mounting it onto AMCs to be installed into slots of mTCA crates. Also, for not blocking a neighbouring slot of the crate, the components of the card should be located between the FMC PCB and the AMC motherboard, which offers a stacking height of up to 9.5 mm as stated in the ANSI/Vita 57.1 standard for FMC modules [10]. For multi-port Gigabit Ethernet connectors on the market, only those with four ports and a single-row alignment offer a size which comes close to the height limit underneath the FMC module. More specifically, a special low-profile connector had to be selected which makes use of a PCB cut-out under the connector's jack area [11], in order to stay below the maximum component height. Unfortunately, choosing this kind of connector had the disadvantage of having to increase the length of the PCB beyond the size of a usual FMC card by 13 mm in order to avoid a collision of the RJ45 connector's housing with the mounting holes of the FMC card which provide the necessary cable relief. The down side of this modification is that the default slot cover plate of the used AFCK cards cannot be installed when these cards are mounted.

Since these components only provide the electrical connections to the TP cables but offer no galvanical isolation, additional transformers are required on the PCB. Here, the differential pairs of the four RJ45 ports are interfaced with the FMC connector through two 8-channel transformers. In order to support the transformers in rejecting the LVDS common mode voltage from the FPGA's output signals, which is referenced to the local ground potential, addtional ac-coupling capacitors are available on the signal traces.

Another means to electrically isolate two connected boards on different ground potentials is to couple the chassis ground of the RJ45 connector only capacitively to the ground of the FMC connector. For doing that and in order to withstand a potentially electrostatically charged cable shield, a 2kV-rated set of ceramic type X7R [12] capacitors with isolation voltages of ~1,000 $M\Omega/\mu F$ is connected between the mentioned grounds. Like this, for steady or slowly ramping ground potentials only very small currents can flow between two FPGA boards which are connected through the shield of a S/FTP cable.

At the FPGA side LVDS signals are used for transmitting clock and synchronization signals over the TP links. For being able to properly receive the ac-coupled TS link signals, DC biasing resistors are available at the FMC connector's side

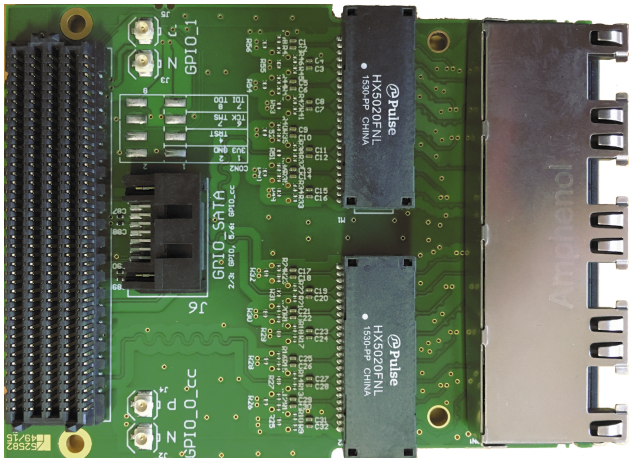

Fig. 4. tDPB FMC with galvanically isolated Twisted-Pair links

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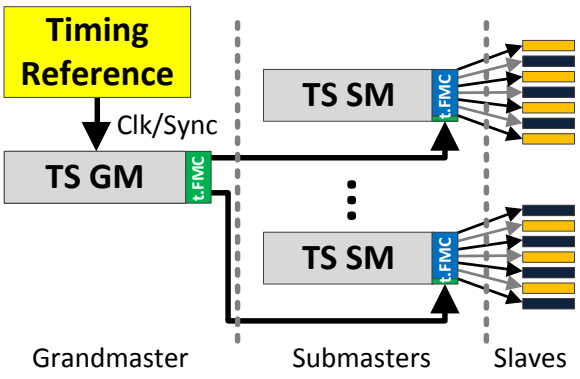

Fig. 5. Topology of an hierarchical TS Systems

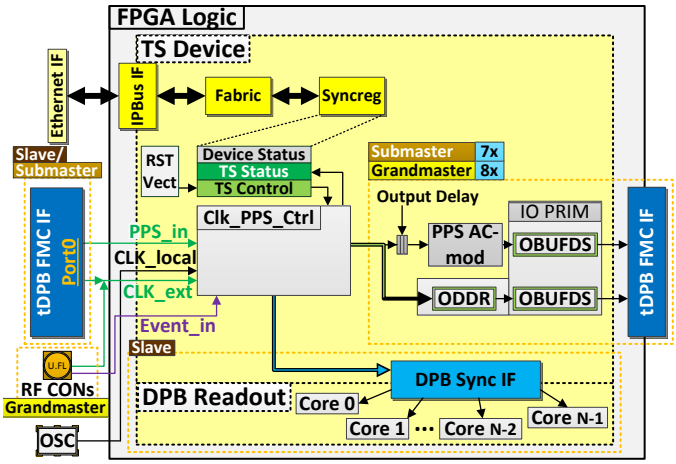

Fig. 6. Block diagram of the TS cores instantiating the clk_pps_ctrl

of the LVDS lines which are dimensioned by default for an adjustable voltage (V_{adj}) of 2.5V. At the PCB it is also possible to install a 100 Ω parallel resistor for terminating the line. However, for minimum reflections the internal termination resistors should be enabled at the receiving IO pairs at the FPGA side. For the used Xilinx FPGAs [15], this option is available in order to reduce the length of the transmission line between the differential receiver and the termination resistor, i.e. the unterminated stub of the transmission line.

Since on the AFCK AMCs there are only a few user I/Os, the tDPB FMC is equipped with two additional clock capable and two usual I/O pairs. One pair of each type is connected to very small Hirose U.FL jacks [13] and one Serial ATA connector. The connectors are mounted on the bottom side of the card so that the I/O cables may also be connected when the card is installed in an mTCA crate. In case of the TS system, the U.FL pairs are used to input a clock reference and a synchronization signal or to output signals from the FPGA for the purpose of system evaluation.

In summary, the tDPB FMC provides a versatile, galvanically isolated interface between FPGA boards. Due to fact it uses LVDS signals for transmitting information over the TP links, the application detailed in section III-B is not the only possible scenario. More specifically, the four differential pairs are not constrained to a specific protocol, i.e. the designer is free to decide which kind of information to transmit in what direction as long as the selected signalling rates are within the the capabilities of the TP link (see section IV).

B. Design of the Timing Synchronizer logic cores

An important requirement when designing the TS system was the simple integration of the TS core logic into existing processing nodes and to ease the usability of the final system. For the former, the TS cores are built around a parametrizable central core (see Figure 7) which processes a clock and a synchronizing pulse-per-second (PPS) from the TS link at the Slaves. The same core can be used at the TS Master by changing the parameters and adding a few output primitives in order to interface up to eight TS links. In Figure 6 a block diagram of the TS Slave/Master designs is shown which instantiate the parametrizable clk_pps_ctrl core.

For the beam test setup with more than eight slaves, it is possible to parametrize the central core in the TS Submaster configuration so that it receives the information from one TS link and forwards it to up to seven TS Links. When a topology is extended by a TS Submaster layer an hierarchical TS system is formed which allows to connect up to 56 TS Slaves with only one additional layer of hierarchy (see Figure 5).

In order to allow controlling the TS nodes, they are designed as IPBus Slaves. By connecting a TS node to an available IPBus Fabric interface, it can be easily integrated into existing IPBus designs. Through a set of IPBus slave registers, all of the important status and control signals of the central clock and PPS logic can be accessed which gives a high level of control to the user during runtime.

The main functionality of the central logic part is the generation of a PPS and a clock signal which will be transmitted over a TS link. For the former, a PPS generator is available which provides a PPS signal for the TS link and a cycle/second counter signal for using it by the local DPB readout logic. Here, the cycle-level counter is locked to the PPS signal, i.e. the occurrence of the PPS marks the beginning of a new second where the cycle counter is zero.

In the basic operation mode of the PPS core, it is controlled by the Start and Halt signals which autonomously generates a PPS signal based on the aforementioned counters.

Besides that, the PPS logic may be locked to an external

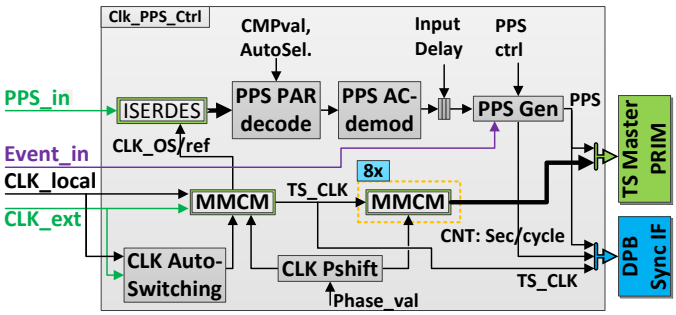

Fig. 7. Block diagram of the parameterizable central Clk_PPS_Ctrl core

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PPS signal, i.e. an user defined signal from the GPIO ports or the TS link PPS. As an alternative, it is also possible to use the local PPS generation but start its operation when a certain event condition becomes true, e.g. a high level at an input signal. The difference between both mentioned external PPS triggering features is that the former requires a strictly periodically occurring pulse-shaped signal at the PPS generator's input whereas the latter starts the PPS generation only once after the event mode has been activated through IPBus. The event listening functionality becomes especially important when a TS Grandmaster (the root of the TS system) needs to be synchronized to an external high quality reference which doesn't provide a PPS-like timing signal. For the example of CBM, this may be the CLOSY clock generator system [16] from CBM's TOF detector. Here, an adequate means is to use a GPIO pair to input some kind of a periodically occurring event and an internal counter which registers the time since the last activity of the event. Through IPBus the software may monitor this counter and enable the event triggering at a desired point in time, e.g. in order to start it when there is enough slack until the next event so there is sufficient time to adjust certain settings at the TS Slaves like the second counters. After the event triggering is enabled, the TS Master starts the PPS generation on the next occurence of the event.

The clocking functionality of the TS system is handled by using Xilinx MMCMs [14]. At the TS Master, a clock signal from a local oscillator or an external reference source is processed to provide the TS link clocks. Compared to that, the TS Slaves or Submasters may use a clock from the TS input link or from a local oscillator. For the TS Master and Slave nodes it is of utmost importance to stay available independent from the currently selected clock source. Thus, for the clock control of the TS system an auto clock-switching feature was implemented. The fundamental assumption for this implementation is, that the local oscillator is always present, but the external clock is to be preferred because it is of higher quality or locked in frequency to a global timing reference. For the auto-detection, the clock from the local oscillator samples a divided version of the external clock signal. Afterwards, counters in the domain of the local clock (cnt_good/∗_bad) are used in order to determine if the external signal is active or if it is stalled. In case one of the counters wraps, the clock source is switched at the MMCM to the external (∗_good) or back to the local clock source (∗_bad) in order to guarantee the reachability of the node through IPBus and e.g. to analyse a potential problem remotely.

Due to the ac-coupling of the LVDS links at the tDPB FMC caused by the capacitors in series and the isolation transformers, transmitting a usual PPS signal may lead to problems because it is for most of the time at a constant DC-level. For that reason, the transmitted PPS is encoded into an rectangle sequence using a logical exclusive or conjunction (XOR). For simplicity, the high/low duration of this alternating signal is of the period of a PPS pulse (one clock cycle). On the output the XOR conjunction causes three periods of the same value (low or high) in case of a PPS activity.

At the TS slave side the decoding of the PPS signal is handled by applying the same conjunction on the current value and the one from the previous cycle. If this condition was applied in its basic form to the data from the incoming TS link, this could cause erroneous PPS detection on a startup/reset of the TS Master where the TS link PPS may be at a constant value for a certain amount of time. Because of that, the history of the PPS signal needs to be taken into account at the decoding stage, i.e. it is enforced that the input PPS has shown a certain number of alternations before an input PPS signal may be interpreted as valid.

To ease aligning the PPS input signal, the TS link PPS is oversampled by a factor of eigth through Xilinx ISERDES primitives [15]. An PPS oversampling decoder core is attached to the input serializers which allows an automatic determination of the current alignment of the received PPS signal relative to the system clock. With this method no user intervention is required for a proper PPS detection as it might be the case for approaches using Xilinx's IDELAY components [15].

When it comes to the point where a TS network of a Grandmaster, potentially a Submaster and several Slaves is composed, means are required which allow to set the alignment of the Slave nodes relative to each other. Due to the fact there is no feedback path to the hierarchical parent node in the current system, a calibration of the setup is required.

For tuning the coarse alignment of nodes, the TS cores are equipped with cycle delay lines for the PPS signal which may be adjusted via IPBus. At the Slaves, the input PPS signal may be shifted before it enters the PPS generator which derives a local PPS and second/cycle counter signal. For the Master nodes it is also possible to delay any TS Link PPS output independently from the others. Like that the system designer may decide whether to adjust the Slave or the Master side for tuning the cycle-level delay of the PPS.

In case an alignment is required which is more accurate than a PPS cycle period, there is also the option to tune it at the clock level. In order to provide this option to the user, the fine phase shifting feature of the MMCMs [14] is made available through the IPBus registers at the TS nodes. At the Slaves it is possible to shift the received TS link clock by any desired angle, currently at the resolution of about 25 ps. For completeness it should be noted that the accuracy of this feature is limited by the jitter of the received clock which is in the range of about 110 to 130 ps peak-to-peak jitter (see section IV).

Using the phase shifting at the Slaves/Submasters however has the disadvantage that the alignment of the received PPS signal relative to the clock changes which may lead to instabilities. The better approach is to shift the phase of the transmitted clocks at the Masters. For that reason, every TS link output at the Masters may be equipped with a dedicated MMCM which allows to shift the phase of the output, again, independently from the others.

In order to fully make use of the advantage of adding a phase shift at the Master side, the adjusted transmit clocks are used to operate the PPS ac-modulation cores which are connected to the output primitives towards the TS link. Like this, the phase relation of the TS link PPS relative to the TS link clock stays the same since both output signals are effectively shifted by the same amount of phase.

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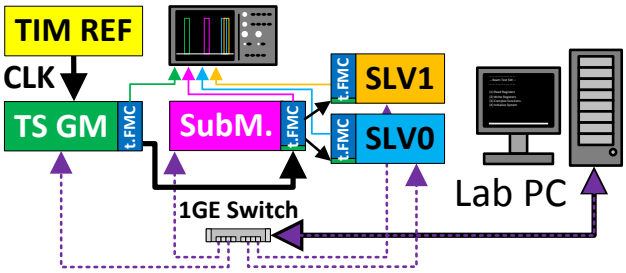

Fig. 8. Block diagram of the evaluated Hierarchical TS System

Last but not least, early laboratory tests showed that configuring the TS Slaves and Submasters through software from the scratch can be a lengthy process. Thus, it was chosen to set the Submaster and Slave IPBus register reset values to the most common default configuration. Like that, the startup of these nodes is eased since no software activity is required in order to bring up a system where Submasters and Slaves automatically lock to a connected TS link and/or provide the required signals.

C. The Timing Synchronizer IPBus Software

For controlling the TS nodes in a laboratory setup, a software based on the IPBus Framework [2] was designed.

The software to be executed on the laboratory PC supports all of the HDL logic core's features described in chapter III but requires only a relatively low level of complexity. It uses address files as defined in the IPBus framework for determining the register addresses in the FPGA design when executing the software.

The software is structured in a way that there are functions of different complexity which may be used by the developer. On the one hand, there are basic functions which directly access status and control registers by only performing one read or write operation. On the other hand, complex functions perform several consecutive accesses to different registers like the fine-phase shifting or even the initialization of the whole laboratory setup.

When starting up the software, the current laboratory system's configuration can be determined on-the-fly. For doing so, the software iterates through the IPBus connection file which states all potentially available boards' IP addresses and accesses each of the FPGAs. For all present boards, the type of TS core is determined (status register) and it is added to the list of hardware devices for the current laboratory setup. Afterwards, the developer can control and monitor any node on the list through an easy to use user menu in software.

IV. Evaluation

A laboratory setup was integrated which allows to accurately evaluate the TS subsystem of future beam tests. Here, the AFCK mTCA AMCs are the target device of the readout chain and also the TS nodes.

The system in focus was built from four AFCK boards, where one served as a Grandmaster, another one as Submaster

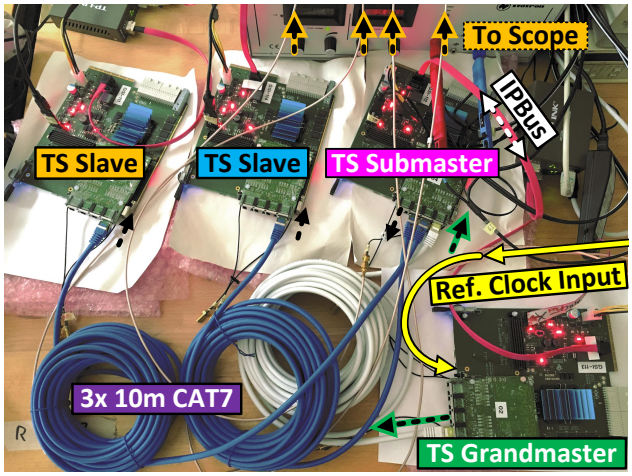

Fig. 9. Picture of the evaluated TS system

and the remaining two as Slaves which are connected to the Submaster board (see Figure 8 and 9).

For this laboratory setup, on every of the AFCK boards one tDPB FMC was mounted. Ethernet Category-7 Twisted-Pair cables of 10 m length were selected, since this will be the maximum required distance for connecting any board in the beam test to the respective hierarchical parent node. An external 40 MHz reference clock (SMA cables at the tDPB FMC) is provided to the TS Grandmaster which is processed and forwarded to the TS network. As can be seen in Figure 6 of chapter III, port 0 of the tDPB FMC serves as the TS link receive port at the Submasters and Slaves whereas at the Grandmaster, all of the TS link ports are used as outputs.

In the laboratory setup, an IPBus network is composed in order to interact with the nodes. Later on this interface will be used as the slow-control of the beam tests.

Using the U.FL connectors on the tDPB FMCs the local PPS signals of each TS node is output and fed to an oscilloscope. Comparing these outputs allows do determine whether the nodes were able to receive data from the TS link, lock to the provided link clock and how much delay is added by the TP cable and the TS FPGA logic itself. Due to the delay skew being intentionally added by the manufacturers to the pairs of these cables [17] the Slaves are usually not perfectly phase aligned. This may be compensated later on through fine phase shifting of the TS clock or offline calibration which depends on the recorded detector data or test patterns from the FE ASICs. The latter may be the potentially better way for obtaining accurately synchroned data from a beam test setup in case e.g. the produced detector elements show variations in their characteristics regarding latency, like amplitude dependent signal slopes or process variations during fabrication which may anyway require a calibration in the offline domain. On the other hand, coarse adjustments on the level of several clock cycles (25 ns at 40 MHz) are usually not required at 10 m distance since the propagation delay is at this frequency in the range of only one up to two cycles. Nevertheless, in case of irregular TS networks where e.g. some Slaves are directly connected to the TS Grandmaster and others through

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a Submaster, cycle-based adjustments will become necessary.

Final measurements show that the system is capable of operating beam test setups with twisted-pair cables at the target distance of 10 meters with TS Link data referenced to a 40 MHz clock. In Figure 10 (a) the PPS signals of the four mentioned nodes are shown. Since in this measurement the Slaves had an offset below 1 ns, Subfigure (b) shows another recording of the same measurement with a smaller timescale. In Subfigure (c) the phase offset between the two Slaves is compensated by the fine phase shifting functionality. With the tested cables there is usually a maximum phase misalignment of up to about 2 ns for Slaves at the same hierarchy which is mainly caused by the delay skew of the TP cables.
Through further measurements it was possible to show that a TS link referenced to a 40 MHz clock is not the limit of the TS system (see Figure 11). In a test setup of two Slaves and a Master node it was measured that even at 120 MHz which is three times the TS system's target frequency it is possible to operate stable TS links with 10 m CAT7 cables. Since on the PCB components for 1 Gigabit Ethernet are used (reference frequency of 125 MHz), these evaluations prove that the designed tDPB FMC does not limit the performance of the TS system.

In order to analyze the jitter performance of a 40 MHz clock from a TS link being driven by a TS Master, the setup depicted in figure 13 was constructed. Here, an Agilent 86100C Digital Communication Analyzer (DCA) [18] receives a reference signal (TRIG) from an Hewlett Packard 8648D signal generator [19] which is also forwarded (3 dB splitter) to a TS Grandmaster node in order to use it as a reference clock. For converting single-ended to differential signals and vice versa, Marki BAL-0006 [20] balanced-unbalanced (balun) components were used which offer a built-in 100 Ω differential/50 Ω single-ended line termination. One of the TS link Twisted-pair cable outputs of the Master is connected to a Texas Instruments RJ45 to SMA adapter board [21] in order to extract the TS link clock which is connected to the signal input of the DCA. Like this, both the DCA and the TS Master are referenced to the same clock source allowing to analyse the jitter being caused by the TS node. For the measurements, the standard settings for the slew rate (SLOW) for the LVDS signal outputs were selected at the Xilinx FPGA of the TS Grandmaster. The curves recorded by the DCA are depicted in Figure 12. For better recognisability of the deviation of the signal's rising edge from a perfect line, an implied ideal rising edge is drawn into the graphs.

With 10 m of CAT7 Screened Foiled Twisted Pair (S/FTP) Ethernet cables about 15 ps RMS jitter was measured (Figure 12a) which translates to 112 ps pk-k jitter for a sample size of 10.000 [22]. As a comparison, the CAT7 cable was replaced in one measurement by 10 m of flat CAT6 Unshielded Twisted Pair (UTP) cable (Figure 12b) which leads to a not that worse jitter of about 17.5/130 ps RMS/pk-pk respectively.

As can be seen in the recorded graphs of Figure 12, using the UTP CAT6 cable leads to a worse signal quality for the TS link regarding the attenuation of the general signal amplitude (about -1.56dB) but also the higher frequency range causing significantly less steap signal edges. The 10%/90% rise times were determined as 5.3/6.8 ns for 10 m of CAT7/CAT6 cable respectively. The rise time of an ideal rising edge implied in Figure 12 by a line, evaluates to about 3.1/3.75 ns respectively. With a 3 m CAT7 cable a rise time of about 2.6 ns was measured. Nevertheless, system tests showed that both types of cables are sufficient to operate the TS system at 10 m cable length without instabilities.

Besides the evaluation of the quality of the electrical properties of the system, the laboratory setup was also tested in terms of its controllability and the repeatability of results. Regarding ease of use, the hierarchical TS network is able to automatically become synchronized as soon as the TS Grandmaster is started due to the selected default configuration on a system reset mentioned in chapter III. Like this, for

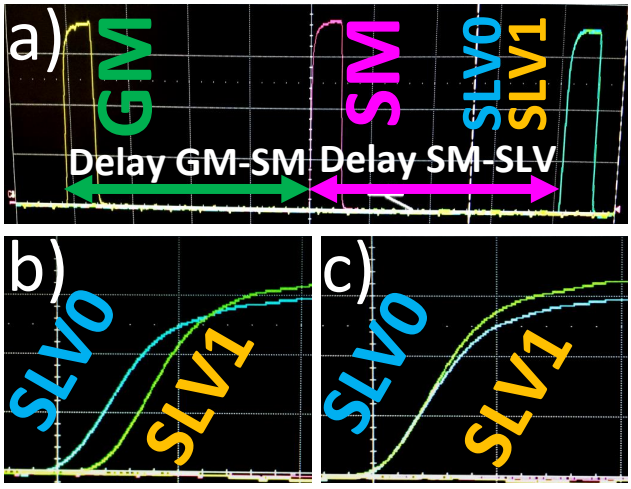

Fig. 10. (a) PPS signal of a locked TS System with active Grandmaster, Submaster and two Slaves (TS Link referenced to 40 MHz clock, 50 ns/div timescale); (b) detailed view of the PPS signals of the two Slaves (SLV0 = blue, SLV1 = green, 2 ns/div); (c) PPS of Slaves after fine-phase shifting

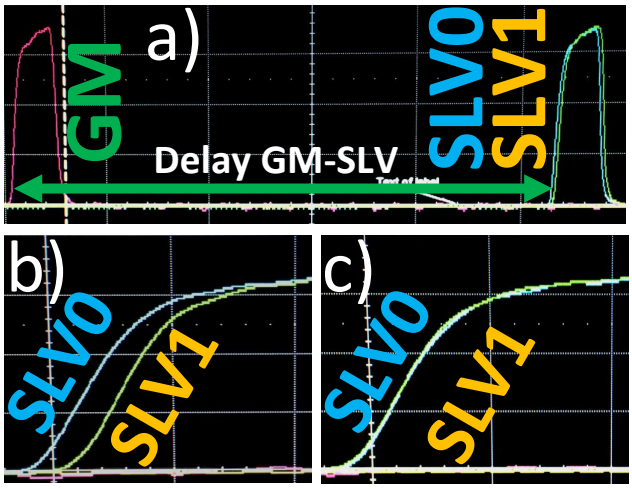

Fig. 11. (a) PPS signal of locked TS System with active Grandmaster and two Slaves and TS Link referenced to 120 MHz clock (20 ns/div timescale); (b) detailed view of the PPS signals of the two Slaves (SLV0 = blue, SLV1 = green, 2 ns/div); (c) PPS of the two Slaves after fine-phase shifting

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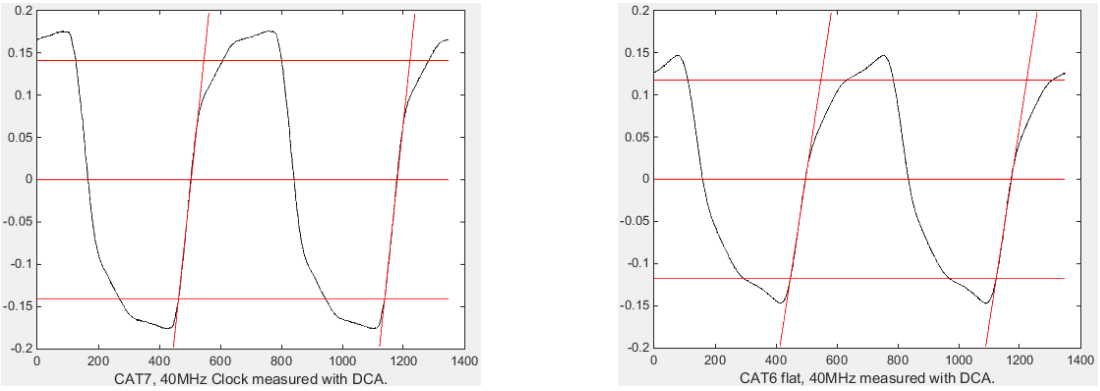

(a) Measurement of TS Link on CAT7 S/FTP cable

(b) Measurement of TS Link on flat CAT6 UTP cable

Fig. 12. TS Link Clock signals recorded by the DCA for a 10 m CAT7 and CAT6 cable with lines for the implied perfect rising edges and 10%/90% levels

the default case of the system configuration, no additional user intervention is required to initialize the Submaster or Slave nodes of the system. In addition to that, measurements show that a quite constant sub clock-cycle latency on the FPGA input/outpus can be achieved for repetitive system startups, FPGA reconfigurations and implementation runs for the same device through a modest amount of floorplanning (e.g. selection of MMCM primitives) and by using the IOB Flipflops [15] for the PPS outputs.

V. Conclusion and Outlook

In summary, the presented system offers the performance required to synchronize pre-series beam test setups. Regarding jitter the system is cable of meeting the requirement of 150 ps pk-pk for both CAT7 S/FTP and CAT6 UTP cables (110/130 ps pk-pk). Through the tDPB FMC an galvanically isolated interface to Twisted-Pair cables is provided offering links for constant latency transmissions at the level of clock cycles. The card allows the interconnection of units on significantly different steady/slowly ramping ground potentials using shielded cables. For some scenarios, using the evaluated unshielded cables can be an additional safety measure in case of fast-changing potential differences. The versatile TS cores can be integrated into existing readout designs with a small amount of effort. Through the IPBus-based slow-control interface the configuration of the distributed TS network is eased since a high degree of control is given to the user during operation of the system. Measurements prove the capability of the system to provide a TS link with a clock at rates of up to three times the required frequency of 40 MHz and a matching PPS signal at 10 m distance in order to synchronize an hierarchical TS network integrated into the readout of a beam test.

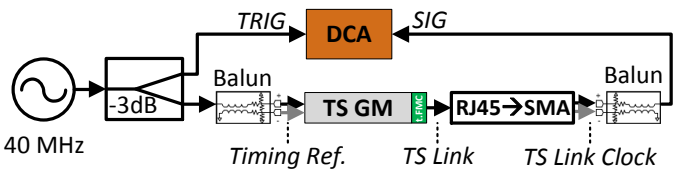

Fig. 13. Setup for measuring the quality of the clock on the TS Links

Since the clock jitter of the current system is not sufficient to operate synchronous fiber links towards the FEE and no feedback channel is available, the so-called Timing and Fast-Control system will add a timing synchronization with low jitter and automatic phase compensation in combination with a control system for bidirectional low-latency transfers of critical messages to enable the final free-streaming readout of CBM.

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