NbSi Barrier Junctions Tuned for Metrological Applications up to 70 GHz: 20 V Arrays for Programmable Josephson Voltage Standards

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***Abstract*—PTB started using the robust Nb_xSi_{1-x} barrier junction technology for the fabrication of large arrays for the Programmable Josephson Voltage Standard (PJVS) and for the Josephson Arbitrary Waveform Synthesizer 3 years ago. We demonstrate how Nb-doping of the amorphous Si barrier causes the transition from an underdamped to a desired overdamped junction behavior. Special dc SQUIDs have been used to evaluate junction capacitance and noise properties. The critical current of small junctions as a function of applied magnetic field has been investigated. On the basis of an existing 70 GHz design previously used for 10 V PJVS chips, we fabricated for the first time 20 V circuits with nearly 140 000 double-stacked Josephson junctions. A direct on-chip comparison between the two 10 V halves of the binary-divided array confirmed the metrological suitability of the 20 V circuits for dc and ac applications.**

***Index Terms*—Amorphous NbSi barrier, Josephson junctions, programmable Josephson voltage standard, SINIS junction, SIS junction, SNS junction, SQUID.**

I. Introduction

FOR a few years now, Nb junctions with Nb_xSi_{1-x} barriers have been used to fabricate large arrays for PJVSs and JAWSs [1], [5]. As the electrical properties of this junction type can be easily tuned by changing the niobium content and the thickness of the barrier, operating frequencies ranging from 15 GHz to 70 GHz and above are possible [2]. The implementation of this robust technology as a substitute for the formerly used SINIS technology was a breakthrough in the realization of functioning and defect-free 10 V circuits for the PJVS [3]. Since 2010, PTB fabricates completely in-house 10 V circuits comprising 69 632 Josephson junctions (JJs) with Nb_xSi_{1-x} barriers operating at 70 GHz [4]. Also in 2010, NIST reported their first 10 V PJVS realized with triple-stacked Nb_xSi_{1-x} JJs for operation from 16 GHz to 20 GHz [5]. In 2012, the use of Nb_xSi_{1-x} JJs for voltage standard applications will culminate undoubtedly with the fabrication of the first binary-divided 20 V circuits with 139 264 JJs (realized by double stacks) operating at 70 GHz for the PJVS at PTB. Section III of this paper describes this recent achievement and the metrological characterization of these circuits. But first in Section II, we report the current status of the fabrication technology at PTB and summarize the electrical properties of Nb-Nb_xSi_{1-x}−Nb JJs as function of the Nb content in the barrier.

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II. Fabrication Process and Basic Properties of Arrays Built With Nb-Nb_xSi_{1-x}−Nb Junctions

A. Fabrication Process

In 2006, PTB produced the first-ever 10 V binary-divided arrays in SINIS (S = superconductor, I = insulator, N = normal metal) technology usable for applications in ac metrology [6]. But the low fabrication yield due to damage of the very thin AlO_x-barriers, was a strong motivation to seek another barrier material with sufficient damping and evaluating its suitability for an existing and proven 70 GHz microwave design [3]. Driven by the idea that SNS junctions are very robust also in a complex fabrication process, the barrier material finally found was the "rediscovered" amorphous Nb_xSi_{1-x}. The resistivity of this material, already known since 1987 as a candidate for Josephson junctions [7], can be controlled by its Nb content from insulating to conducting (metallic). It therefore represents an almost universal barrier material for Josephson junctions, allowing control of characteristic frequency and damping. For instance, NIST started using Nb_xSi_{1-x} barriers for SNS arrays driven at 20 GHz already in 2007 [8]. PTB (design, circuit fabrication) and NIST (trilayer deposition) together successfully demonstrated that this junction type can also be customized for 70 GHz. Within the framework of this cooperation, 10 V arrays for the PJVS with Nb_xSi_{1-x} barrier junctions were first realized in 2008 [3]. These 70 GHz circuits immediately showed a better performance (current margins larger than 1 mA) and for the first time no "missing junctions", as compared to 10 V SINIS arrays.

In 2010, PTB itself started to fabricate such 10 V arrays for the PJVS completely in-house using an automated sputtering cluster. The patterning process of the SNS circuits starts from Nb-Nb_xSi_{1-x}−Nb trilayers deposited by the dc sputtering technique onto 3 inch Si wafers. The growth of the Nb_xSi_{1-x} layer is the key step within the trilayer deposition, because both the thickness and the composition determine very sensitively the critical current density j_c and the characteristic voltage I_cR_n of the JJs (I_c being the critical current and R_n the normal state resistance). To ensure a well-controlled deposition, the Nb_xSi_{1-x} barrier is co-sputtered in a separate chamber from two 2 inch targets (Nb and p-doped Si) in confocal position onto the rotating wafer. This extends the life time of the Nb

target and the sputtering rate is kept relatively constant over a long period. The target values for I_c and R_n of a given design [3] hence become easier to achieve and to reproduce. Control of the Nb content is realized by adjusting the power supplied to the Nb sputter gun and assuming a fixed power on the Si target. We fabricate our trilayers for 70 GHz with 14 W, which results in a Nb content of $x \approx 10$ at.% evaluated by EDX analysis using Ge substrates. For 16 GHz, we apply about 28 W ($x \approx 20$ at.%). Si is always sputtered at 130 W. Another key parameter of the barrier deposition is the co-sputtering time of Si and Nb which determines the thickness of the Nb_xSi_{1-x} layer. We found that the co-deposition rate is always smaller than the sum of the Nb and Si rate and at 14 W nearly identical with the Si deposition rate. These facts suggest a relatively loose structure of the amorphous Si which facilitates the inclusion of Nb atoms up to a certain degree.

A 4 inch Nb target in a different chamber and positioned face to face is used for all other Nb layers: Base electrode of the trilayer (200 nm thick), counter electrode (100 nm) and the 560 nm thick wiring layer. The deposited trilayers are patterned by means of a self-aligning process that is very similar to the fundamental SNEP technique first developed by Gurvich *et al.* [9]. The only difference is that Al_2O_3 is substituted by Nb_xSi_{1-x}. All metallic (Nb, NbSi) and insulating (SiO_2) layers are patterned with e-beam lithography and ICP (Inductive Coupled Plasma) dry etching with SF_6 and CHF_3 except for the Nb ground plane and the AuPd load resistor for termination of the microstripline. More details can be found in [3]. As the etching rates of Nb and NbSi are quite similar and result in nearly vertical edges, the patterning of double-stacked junctions from deposited pentalayers easily allows to increase the number of JJs [2].

B. Basic Junction and Array Properties

Josephson junctions with amorphous Si (a-Si) as barrier material were already investigated in the early eighties. It was demonstrated that under certain conditions large values of I_cR_n up to 1 mV are achievable [10]. Electrical transport processes in amorphous Si are dominated by hopping conduction: resonant tunneling between localized states of similar energy formed by non-bound electrons (dangling bonds of Si). It is assumed that inelastic resonant tunneling through localized states causes the internal shunting of Nb-Si-Nb junctions [11]. There are a number of experimental and theoretical papers dealing with the hopping conduction and its noise properties. A detailed review article about the $1/f$ noise in variable range hopping conduction was written by Shklovskii [12]. Another group observed enhanced shot noise (with respect to the Poisson value) and explaines it by correlated resonant tunneling involving interacting localized states [13]. The influence of Schottky barriers (between Nb and Si) on the electrical transport processes through the barrier is still an open question [14]. In order to characterize the initial situation (quality of Si target, deposition parameters) without Nb-doping, we prepared Nb JJs with a 5 nm thick a-Si barrier.

Fig. 1 shows the current-voltage characteristic (IVC) of a 100 junction array. The shape of this IVC is typical for underdamped SIS junctions of high quality [15], i.e. low subgap current and steep current rise at the Nb sumgap voltage $2\Delta/e = 2.88$ mV/JJ. The characteristic voltage I_cR_n is about 1 mV, calculated with an averaged $I_c = 280$ μA (inset of Fig. 1). This high-quality SIS characteristic can be explained by assuming distances between localized states larger than the thickness of the a-Si layer. The a-Si constitutes in this case a nearly ideal semiconducting tunnel barrier with a low barrier height which ensures a sufficiently large tunneling probability even for a relatively large barrier thickness (5 nm).

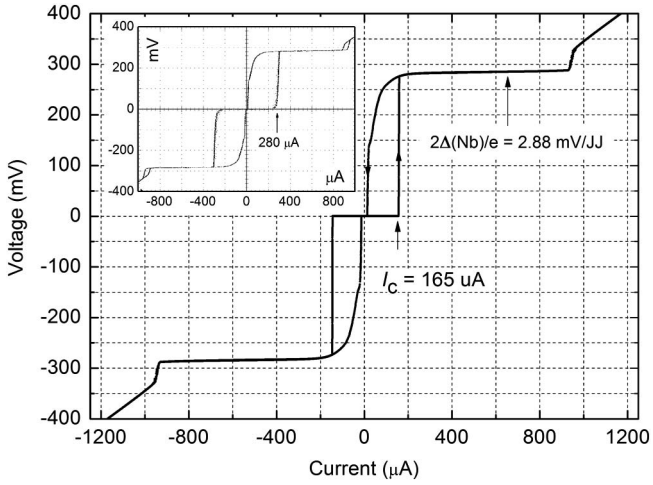

Fig. 1. IVC of an array with 100 Nb-Si-Nb Josephson junctions. Averaged junction parameters: $I_c = 280$ μA (inset), $I_cR_n = 1$ mV with $R_n = 3.4$ Ω given by the linear IVC above $2\Delta(\mathrm{Nb})/e$, $d_{Si} = 5$ nm and junction area $= 120$ μm^2. The inset shows a larger I_c for the case where the current source is battery-powered and the voltage measured with an oscilloscope instead of a digital voltmeter.

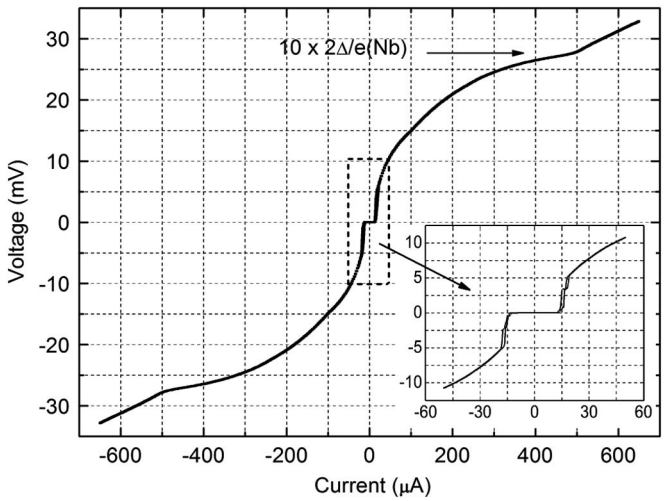

Fig. 2. IVC of a 10-junction array with Nb_xSi_{1-x} barriers ($x \approx 9$ at.%, $d = 10$ nm). The inset shows the enlarged IVC at low currents. Junction parameters: $I_c = 15$ μA, $I_cR_n = 375$ μV (R_n at 2 I_c) and junction area $= 20$ μm^2.

Adding Nb by co-sputtering to the a-Si increases the density of electron states inside the barrier and therefore the subgap current too. It is well known that a significant effect on the electronic properties of a-Si can only be observed for a Nb content in the percent range [16]. This effect of Nb-doping is illustrated by Fig. 2, presenting the IVC of an array consisting of 10 JJs. The Nb_xSi_{1-x} barrier is 10 nm thick and contains

about 9 at.% of Nb. The strongly increased subgap current generates the desired internal shunting of the JJs, i.e. the JJs have become more or less overdamped [15] and show negligible hysteresis (inset of Fig. 2). When the Nb content is increased further, Nb_xSi_{1-x} undergoes at 11.5 at.% a metal-insulator-transition (M-I-T) [17]. Arrays used for JAWS are characterized by $x > 11.5$ at.% (typically 20 at.%). The barrier becomes metallic and the resulting IVC in the subgap region resembles the classical SNS type that can be described by the RSCJ model [15]. Microwave-induced Shapiro steps of first order with a large current width, needed both for the PJVS and for the JAWS, are always generated just above I_c. For that reason and in order to avoid a possible hysteresis close to I_c, we define the characteristic voltage $V_c = I_c \cdot R_n$ for a resistance R_n measured at 2 I_c of the bent IVC. The characteristic voltage has to be optimized for a given frequency f according to $V_c \approx (h/2e) \cdot f$ (h being the Planck constant and e the elementary charge).

In the RSCJ model, the McCumber parameter $\beta_c = (2e/h) I_c R_n^2 C$ describes the damping of the JJs [15]. Most applications, PJVS, SQUIDs, JAWS and single flux quantum based electronics (SFQ), require $\beta_c \leq 1$, i.e. no hysteresis of the IVC. In contrast to SNS junctions with classical N metals, the capacitance C of Nb_xSi_{1-x}–Nb junctions can take non-negligible values. JJs with $x \approx 10$ at.% and a thickness of ≈10.5 nm, hereafter referred to as "70 GHz-composition", were of special interest for us. This barrier composition enables characteristic voltages V_c from 130 μV to 150 μV and a current density j_c ranging from 2 kA/cm^2 to 4 kA/cm^2. We followed the method proposed by Maegerlein [18] and determined by means of LC resonances in specially designed dc SQUIDs a specific capacitance of about 380 fF/μm^2. This value is in approximate agreement with comparable measurements made by NIST on similar JJs, regarding barrier thickness and current density [19]. The large specific capacitance is caused by a huge permittivity ($\varepsilon_r = 385$) of this material, which is not yet fully understood for the Nb-Si system. However there are experimental results demonstrating the divergence of the dielectric constant near the metal-insulator transition in doped semiconductors [20].

Measurements on dc SQUIDs also revealed that the $1/f$-noise at low frequencies, $10^{-4} \cdot \Phi_0/\mathrm{Hz}^{1/2}$ at 1 Hz, is about two orders of magnitude larger than in comparable SQUIDs with shunted Nb-AlO_x–Nb junctions [21]. Investigations at different operating points suggest that the increased $1/f$-noise is due to I_c fluctuations. In other words: I_c fluctuations of the Nb_xSi_{1-x} barrier junctions are possibly due to the noise properties of the hopping conduction via localized states mentioned in the introduction to this chapter. However, the I_c fluctuations are not relevant for Josephson voltage standards, as they are too small to influence significantly the current width of the Shapiro steps.

We also measured I_c as a function of applied magnetic field in order to investigate the uniformity of the current density [22]. Fig. 3 shows the "magnetic diffraction pattern" of a small ($4\ \mu\mathrm{m} \times 5\ \mu\mathrm{m}$) junction with a "70 GHz–composition" of the barrier, whose Josephson penetration depth $\lambda_J = 12.6\ \mu$m is large compared to both junction dimensions. However, there

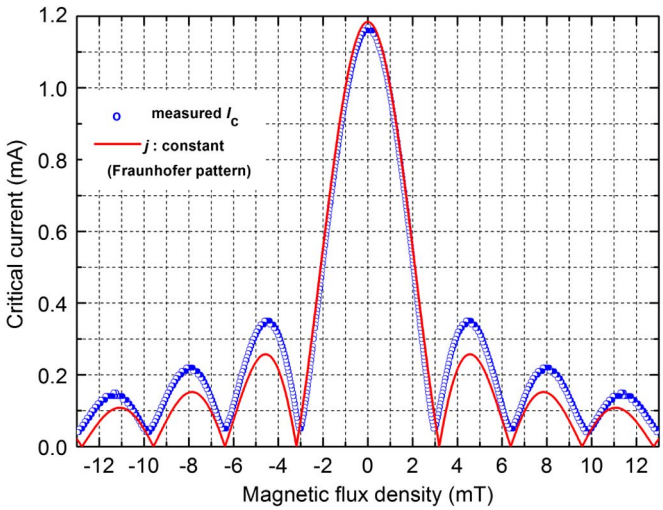

Fig. 3. Magnetic field dependence of I_c for a rectangular ($4\ \mu\mathrm{m} \times 5\ \mu\mathrm{m}$) JJ with a Nb_xSi_{1-x} barrier ($x \approx 10$ at.%, $d = 10$ nm). The magnetic field is parallel to the chip plane and perpendicular to $L = 4\ \mu$m.

is a significant deviation from the Fraunhofer pattern valid for a homogenous current distribution: The secondary maxima of the critical current are elevated and the supercurrent cannot be completely suppressed for any value of the applied field. Whether these facts mean a real deviation from a uniform current distribution, or a non-sinusoidal current-phase relation for this junction type, cannot be concluded from the performed experiments. There is experimental evidence that the current-phase relation for Nb-Si-Nb junctions deviates from the sinusoidal form if resonant tunneling through local states dominates the superconducting current transport [11].

III. 20 V Arrays for the PJVS Operated at 70 GHz

Programmable Josephson Voltage Standards (PJVS) represent, besides the JAWS, the state of the art in the field of dc and ac (limited to low frequencies) voltage metrology. They deliver precise quantized voltages according to the Josephson equation: $U = nMf/K_{J-90}$, where n, M, f and K_{J-90} denote the order of the Shapiro steps (0, ±1), the number of JJs, the precisely controlled microwave frequency and the Josephson constant, respectively. The voltage amplitude can be nearly arbitrarily controlled by programming M and to a lesser extent f.

10 V arrays with Nb_xSi_{1-x} junctions have been routinely produced at PTB since 2010. The 70 GHz design of these binary-divided (programmable) arrays, the experimental investigation and their large field of application in metrology are described in detail by a PTB review paper [1]. The targeted junction parameters: $I_cR_n = 145\ \mu$V, $j_c = 3$ kA/cm^2 and an almost non-hysteretic IVC could be realized with ≈11 nm thick barriers containing ≈10 at.% Nb, i.e. the Nb_xSi_{1-x} is "located" close to the M-I-T point on the insulating side.

It was challenging for us to use the same design for the fabrication of 20 V arrays by means of double-stacked JJs. After a first incomplete attempt, made in 2009 with pentalayers grown at NIST [23], we were worried about the number of JJs increased by a factor of 2 in each of the microstriplines that are connected in parallel (for the microwaves). However,

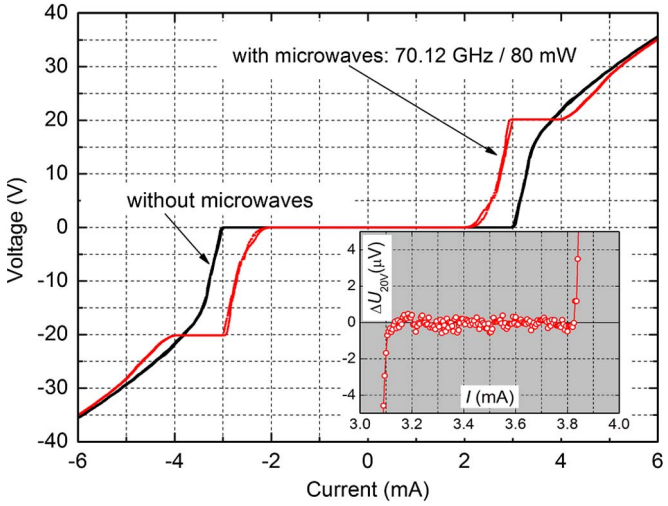

Fig. 4. IVC of a 20-V PJVS with 139 259 double-stacked Nb-Nb_xSi_{1-x}—Nb Josephson junctions. Averaged junction parameters: $I_c = 3$ mA, $I_cR_n = 130$ μV (at 2 I_c), junction area $= 120$ μm^2. The inset shows the width of the 20 V step with high voltage resolution (referenced to 2 series-connected Zener diodes).

experiments revealed that the microwave attenuation in an "active" stripline ($I_{dc} > I_c$) with double-stacked JJs increases only by approximately 25% compared to a stripline with single JJs. The only slight increase of the microwave attenuation, despite a doubling of the junction number, is caused in our opinion by a nearly complete synchronization of the two vertically stacked JJs only separated by a 50 nm thick Nb layer. Self-coupling effects between neighboring stacks occur in active striplines and facilitate the propagation of microwaves. On the other hand, striplines with unbiased array segments (only in one of the outermost striplines of the 10 V design) can present a serious problem as their microwave attenuation becomes relatively large (≈0.04 dB/JJ) [3]. Consequently, active segments lying behind them, could receive too little microwave power in the worst case. Nevertheless, we were able by using the "old" but proven 10 V design, to fabricate the first-ever 20 V binary arrays. Their operating margins are only slightly smaller than for 10 V circuits.

Fig. 4 shows the IVC of the 20 V array with nominal 139 264 JJs arranged in double stacks without and with microwave irradiation. "Missing" JJs (5 for this array) are generally caused by insulation defects between wiring and base electrode leading to superconducting shorts (even number of missing JJs) or by large pinholes in one or both of the double-stacked barriers. A superconducting short between wiring and middle electrode of the stack is very unlikely but cannot be excluded. The inset shows the Shapiro step $n = +1$ at 20 V with a current width of at least 0.7 mA, which is an acceptable value for most applications.

This binary-divided 20 V circuit allowed us to perform for the first time a direct on-chip comparison between two 10 V arrays by using the two halves of the circuit. We demonstrated that the quantization of the two 10 V Shapiro steps agrees within 5 ± 7 parts in 10^{11} (at room temperature). The suitability of the array for metrological applications has therefore been confirmed.

IV. Conclusion

The PTB fabrication technology for JJs with NbSi-barriers enables the production of microwave circuits with overdamped ($\beta_c \leq 1$) junctions for metrological applications (JAWS and PJVS) in the frequency range from 15 GHz to 70 GHz. This is possible by controlling the thickness and the Nb content of the Nb_xSi_{1-x} barrier. Even strongly underdamped SIS JJs ($\beta_c \gg 1$), formerly used for classical Josephson voltage standards, can be realized at the limit of pure ($x = 0$) a-Si barriers. The demonstrated high performance of binary-divided 20 V arrays for the PJVS opens up new metrological applications, e.g. linearity measurements of digital voltmeters up to 20 V or synthesizing of 10 V_{rms} ac signals.

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