Cryocooled 10 V Programmable Josephson Voltage Standard

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***Abstract*— The two main challenges to operating a programmable Josephson voltage standard (PJVS) on a cryocooler are the available cooling power and the temperature oscillations of the cold head. We overcame these challenges and successfully operated a PJVS circuit on a cryocooler by employing one supercritical helium buffer that damps the temperature oscillations, developing a new cryogenic package that increases the thermal conductivity between the chip and the cold head, and increasing overall device performance with fabrication improvements. A 1.32 mA step width of the quantized voltage produced with all of the subarrays of the PJVS circuit biased was achieved at an operating temperature of 4.3 K. The quantum accuracy of the PJVS is maintained at temperatures up to 4.8 K. This result was obtained with a cryocooler that employs a 3 kW water-cooled compressor to produce at the chip about 270 mW of net cooling power at 4.3 K.**[1]

***Index Terms*— Josephson arrays, quantization, standards, superconducting integrated circuits, voltage measurement.**

I. Introduction

SCARCITY of liquid helium (LHe) in many areas of the world provide strong motivation for cryogen-free operation of superconducting devices, such as National Institute of Standards and Technology (NIST) 10 V programmable Josephson voltage standard (PJVS) systems. The PJVS systems [1]–[8] are more immune to current noise than are the conventional Josephson voltage standards (CJVSs), both of which are implemented as primary voltage references at national metrology institutes. Cryocooler operation is essential for enabling complete automation of the of PJVS systems because systems operated in LHe require occasionally human intervention to thermally cycle the device between room temperature and the 4 K device operating temperature. Such automated systems will allow primary voltage references to be used more broadly because they would not require an expert operator who is trained to use liquid cryogen or superconducting devices.

The biggest challenge with implementing a PJVS circuit on a cryocooler is extracting the heat dissipated on the device. The present design of the NIST 10 V PJVS circuit dissipates around 350 mW of power and is typically operated at the LHe boiling point (4 K to 4.2 K depending on altitude). The microwave power used to bias the Josephson junctions (JJs) is the main contributor and is almost entirely dissipated in the coaxial cable and in the circuit termination resistances. The maximum current range of constant-voltage Shapiro steps is obtained by applying 250 mW of microwave power at the room-temperature cryostat head. The power dissipated by the dc bias current scales with the circuit critical current (I_c) and varies with the programmable output voltage of the circuit. If all the subarrays are biased at the center of the Shapiro step, generating an output voltage of 10 V, then heat produced by the dc bias is around 100 mW ($I_c = 6.5$ mA). There are two options to implement such device on a cryocooler. The first option is to select a cryocooler with a cooling power larger than the total heat dissipated by the device. The second option is to select a more economical cryocooler that requires a reduction in the PJVS circuit performances. A limited cryocooler cooling power can be compensated by operating the chip at higher temperatures or by reducing the microwave power biasing the circuit.

Yamamori *et al.* [7], [8] developed a niobium–nitride PJVS circuit with NbN/TiN_x/NbN JJs that can operate at 10 K. The cryocoolers used at this higher temperature have a capacity in excess of one watt with only an air-cooled compressor running on a single-phase power outlet. The CJVS circuits have also been successfully implemented on cryocoolers [9], [10]. Since no continuous dc current is required to generate quantized voltages with the hysteretic JJs of CJVS circuits, only the microwave bias contributes to the power dissipation on the chip, typically less than 15 mW.

An alternative option to the cryocooler is to operate a PJVS circuit in a closed-cycle helium reliquefier. The performance of our NIST 10 V PJVS circuit operating in the reliquefier were identical to that obtained when operated with a standard LHe dewar. The reliquefier we tested had a regeneration rate of 18 L/day with an 8.4 kW compressor. These results will be the topic of another publication. In this paper, we present the results and challenges associated with implementing the NIST PJVS circuit on two different cryocoolers.

II. 10 V PJVS Array

The present design of the NIST 10 V PJVS circuit employs a 32-way microwave splitter that divides the Josephson arrays into individual segments, which are grouped into 23 subarrays (Table I) that are independently current biased either on the positive (p), negative (n), or zero (0) voltage step [2], [11]. At 18.3 GHz, the minimum voltage of 227 μV is obtained by current biasing the subarray with 6 JJs. Each of the subarrays

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TABLE I
10 V PJVS ARRAY CONFIGURATION

Sub-array	Number of junctions	Sub-array	Number of junctions
1	4372	13	16800
2	1458	14	16800
3	486	15	16800
4	162	16	16800
5	54	17	16800
6	18	18	16800
7	6	19	16800
8	8400	20	14958
9	16800	21	16800
10	16800	22	16800
11	16800	23	16800
12	16800		

with 16 800 JJs generates a voltage of 635.7 mV at this frequency. The JJs are triple-stacked junctions made with niobium superconducting leads and amorphous niobium–silicon barriers. The previous flip-chip-on-flex cryogenic package was optimized for immersion in LHe [12]. New device packaging was recently developed for PJVS circuits that optimizes the thermal connection between the JJs and a cryocooler while still allowing operation in LHe [13]. The first patterning step of the circuit fabrication process is removal of the thermal oxide at the surface of the wafer to minimize the thermal impedance between the junctions and the silicon substrate [14]. The backside of the wafer is also metalized with 120 nm of sputtered PdAu to enable the device to be soldered with indium to a copper pedestal on the cryopackage base. Wire bonds connect the array to a high-frequency printed circuit board that is also mounted on the base of the pedestal. The copper base is screwed tightly to the cryocooler cold head, using an indium interface [13]. A semirigid coax and phosphor–bronze wires provide the microwave and dc bias connections to the board.

Improvements in the yield and the uniformity of the JJs [15] have produced devices capable of generating Shapiro steps having bias current width greater than 2 mA. The dc current range over which the quantum state of all the subarrays of junctions remains locked to the ac drive signals is defined as the operating margin of the circuit. The operating margins of an individual subarray or set of subarrays is measured with a dither current relative to the center of the constant voltage step that is generated. When evaluating the operating margin of the device at a specific microwave power and frequency for a PJVS circuit, its subarrays are biased so as to generate a combined voltage close to 0 V (dither-current flat-spot) [11]. For the PJVS circuit described in this paper, operating margin at 18.38 GHz and power around +24 dBm (at room temperature) when immersed in LHe was greater than 1.8 mA. This large operating margin makes the device an ideal candidate for implementation on a cryocooler.

III. CRYOCOOLER

The PJVS circuit was mounted successively on two models of cryocoolers for evaluation. The first cryocooler, based on a Sumitomo RDK-101DP cold head, has 200 mW nominal cooling power at 4 K if operated with a 3 kW water-cooled compressor.[2] The second system (Sumitomo SRDK-205DP) has 500 mW nominal cooling power at 4 K with a 4 kW water-cooled compressor. Unlike the RDK-101DP, which is a standard product, the SRDK-205DP is a special research prototype developed to explore the limits of our technology.

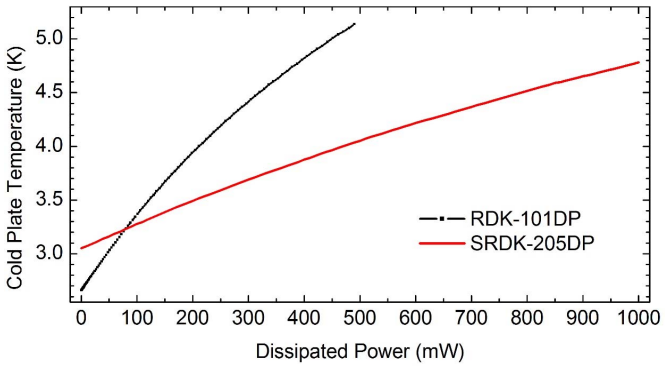

Fig. 1. Load curves measured for the two cryocoolers. Includes all parasitic heat loads.

Both cold heads consist of two-stage Gifford–McMahon cryocoolers. The PJVS array is thermally anchored to the cold plate. The thermometer is mounted on the cold plate next to the PJVS cryopackage. A supercritical helium buffer between the cold head and the cold plate is used to damp the 1.2 Hz temperature oscillations of the cold head. The amplitudes of the temperature oscillation measured at 4 K were 38 mK and 35 mK, respectively, for the RDK-101DP and the SRDK-205DP cryocoolers [13]. This result is a factor of four improvement compared with the temperature oscillation measured without the helium buffer [16]. The bias leads (phosphor-bronze wires), the output voltage leads (twisted-pair copper), and the microwave coaxial cable (CuNi outer conductor and Ag-plated CuNi center conductor) are all thermally anchored at both stages of the cryocooler to reduce the heat conduction to the PJVS circuit. The thermal electromotive force (EMF) signals measured on the precision output voltage leads are similar to those obtained with the LHe cryoprobe. A μ-metal shield is placed around the vacuum enclosure to attenuate the environmental magnetic field at the PJVS circuit. The cooling power of both cryocooler units was characterized with all wiring in place. The load curves, i.e., variation of the temperature when power is dissipated at the cold plate are shown in Fig. 1. Although the base temperature of the RDK-101DP is slightly lower than that of the SRDK-205DP, the cooling power of the SRDK-205DP is significantly larger for dissipated power greater than 100 mW. For comparison, an earlier cryocooler tested in [16] and [17] had a cooling power of 170 mW at 4 K.

IV. BIAS PARAMETERS AND POWER LIMITATIONS

The heat load of a PJVS circuit on a cryocooler consists of the following.

[2]Certain commercial equipment, instruments, or materials are identified in this paper to facilitate understanding. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the materials or equipment that are identified are necessarily the best available for the purpose.

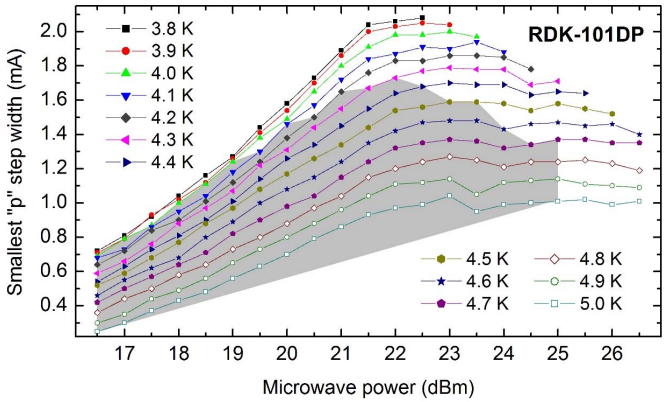

Fig. 2. Smallest step width ($n = +1$ Shapiro step) of the 23 subarrays measured for various temperature set points versus the microwave power at the input of the RDK-101DP cryocooler. The step corners are defined with a ± 3 μV threshold relative to the calculated step voltage. All the data from the RDK-101DP were acquired at a microwave frequency of 18.38 GHz.

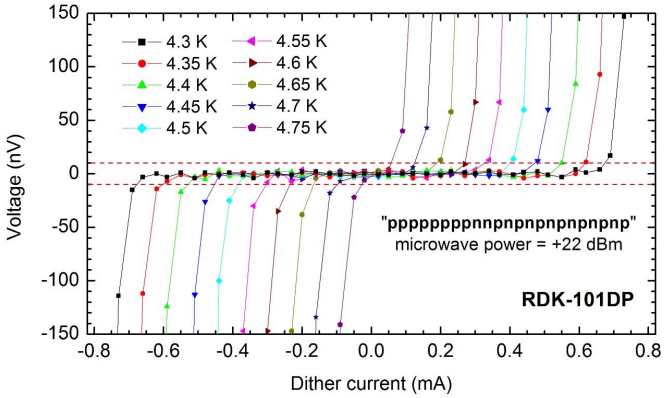

Fig. 3. Dither current flat-spot measurement of all the subarrays at various temperatures with the RDK-101DP cryocooler. The bias parameters of each subarray were set to the values optimized for operation at 4.3 K. The two horizontal dash lines (± 10 nV) serve as guide to the eyes to emphasize the step flatness.

1) The parasitic heat load due to the cryostat, the radiation, the wiring, and the thermometers. These heat loads determine the cryocooler's base temperature.
2) The heat load generated by the microwave power dissipated in the coaxial cable and in the PJVS circuit (in the JJs and the termination resistors).
3) The heat load generated by the dc current used to bias the JJs.

Both cryocoolers that we tested were mounted in cryostats constructed for research purposes and were equipped with spare bias cables. In addition, the RDK-101DP cryostat was wired with four coaxial cables. We expect that the cooling power performance will improve for a cryostat that is optimized for a single PJVS circuit.

The first step of the PJVS operation consists of optimizing the operating margins with respect to the microwave power. Once adjusted, the microwave power remains fixed to ensure a constant heat load on the cold plate. In comparison, during operation in LHe, the microwave power is set to the minimum level when the output of the array is set to 0 V, to reduce the LHe consumption. The heat load generated by the dc bias varies between 0 W and approximately 100 mW, depending on the output voltage and the combination of subarray biases. To keep the temperature of the cold plate constant, the total heat dissipated must remain unchanged. A temperature controller is thus used to regulate the temperature of the cold plate by providing power to a resistor located on the cold head. The results of the temperature stability and response time of the regulation circuit are discussed in Section VI.

The bias parameters of the PJVS are strongly dependent on both the temperature set point and the microwave power that is selected, as shown in Fig. 2. The dependence on power and temperature is correlated; the operating margins improve if the PJVS circuit receives more microwave power, and decrease with increasing temperature. While measuring the bias parameters, each subarray is biased independently and sequentially, resulting in approximately 1/16 of the dc bias heat load generated at 10 V. The gray zone in Fig. 2 shows the parameter space within which the cooling capacity is large enough to compensate for the heat load generated when all the subarrays are dc biased and is also capable of withstanding an extra heat load of at least 20 mW that is required for temperature regulation. For the RDK-101DP cryocooler, the optimum bias point was measured to occur at 4.3 K and 22 dBm (158 mW), with a current margin of 1.74 mA. This value is 15% less than the operating margins measured at 3.9 K and 22.5 dBm. This emphasizes the need to produce PJVS circuits with operating margins in LHe that are greater than 1.5 mA to ensure successful implementation on a cryocooler with nominal cooling power of 200 mW at 4 K. To be safely automated for metrology applications, the PJVS ideally needs subarrays with a current margin of at least 1 mA [11]. The leakage resistance measured with the PJVS circuit mounted on the RDK-101DP cryocooler was identical to that measured in LHe [18], and is dominated by the leakage resistance of the bias electronics.

V. Operating Margins

The operating margins of the PJVS circuit are determined with all the subarrays biased simultaneously using the bias parameters measured initially for each subarray individually (Fig. 2). When the PJVS circuit is operated on the cryocooler, the operating margins must also be verified as a function of temperature. Fig. 3 shows the worst case scenario flat-spot when all the adjacent subarrays with the largest number of JJs are biased in opposite voltage polarity (pppppppppnnpnpnpnpnpnpnp, where p and n represent, respectively, the positive and negative step voltage and the order corresponds to the subarray order in Table I) with a resulting voltage of 0 V across the array. In this alternating p-n case, the current in each bias lead is twice the value required to bias a single subarray. To remove the contribution of the thermal EMF, the flat-spot measurement was performed with bias polarity reversal for each dither current value with a +-+- sequence identical to the procedure implemented for Zener voltage standard calibrations [19]. When the circuit is biased on step, the scatter in the measured voltage is only a few nanovolts. No additional voltage noise, such as 60 Hz coupling that might have been induced by the compressor or from the temperature regulation circuit, was observed in the

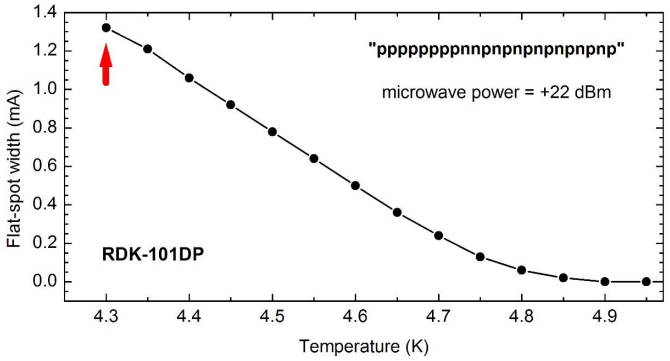

Fig. 4. Evolution of the operating margins with temperature on the RDK-101DP cryocooler, extracted from the flat-spot data measured in Fig. 3. Arrow: temperature at which the bias parameters were optimized.

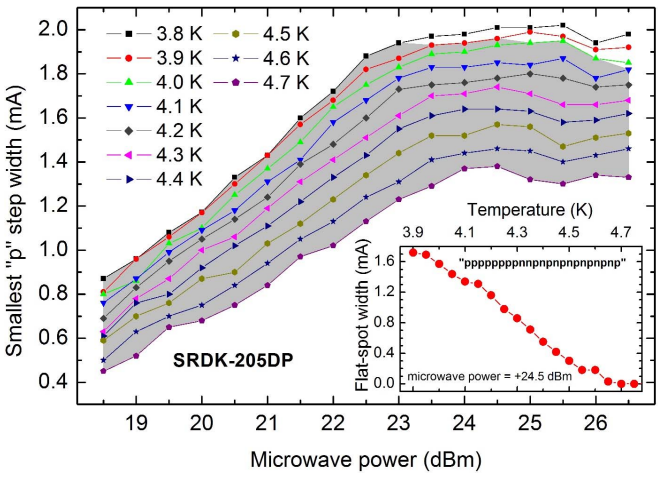

Fig. 5. Smallest step width ($n = +1$ Shapiro step) of the 23 subarrays measured for various temperature set points versus microwave power at the input of the SRDK-205DP cryocooler (500 mW of cooling power). Inset: operating margins versus temperature for the bias parameter table optimized at 3.9 K and 24.5 dBm. All data taken with the SRDK-205DP were acquired with a microwave frequency set to 19.23 GHz.

output voltage. The measurement was performed on the 1 mV range of the nanovoltmeter.

At 4.3 K, the operating margin (1.32 mA) is 24% less than the smallest $n = +1$ step width measured for the same microwave power. This relative difference is typical when comparing the results for the bias parameters (single subarray biased) and the flat-spot measurements (all the subarrays biased) [11]. The bias parameters are defined with a ± 3 μV threshold around the quantized voltage. With the polarity reversal method, the corners of the flat-spot are more tightly defined by use of a voltage resolution of ± 10 nV. The operating margins are affected by the temperature in two ways. First, the step width decreases when the temperature increases, as shown in Fig. 2. Second, the optimum bias current varies with temperature, i.e., the averaged bias current for the 23 subarrays varies from ~8.5 mA at 3.8 K to ~7.5 mA at 5 K. Thus, the bias parameters that are optimal for one operating temperature are not optimal for other temperatures due to this temperature dependence of the bias current (and critical currents). As shown in Fig. 3, the flat spot measured at each temperature remains centered at zero dither current, even though the bias parameters remained fixed at the set points that were optimized for operation at 4.3 K. The observed flat-spot symmetry is due to the fact that the two voltage polarities (p and n Shapiro steps) are tested simultaneously and the PJVS circuit shows homogeneous bias parameter properties.

Fig. 4 shows the temperature dependence of the operating margins that were extracted from the data in Fig. 3. The flat-spot widths reported in Fig. 4 include the effect due to the temperature dependence of the bias current. The quantum accuracy of the PJVS voltage is preserved up to a temperature of 4.8 K, i.e., 500 mK above the temperature where the bias parameters were optimized.

The same PJVS circuit was mounted on a cryocooler with a nominal cooling power of 500 mW at 4 K (SRDK-205DP). With this cryocooler, the best operating margins for all the subarrays were produced at a frequency of 19.23 GHz. The results obtained for the bias parameters (Fig. 5) show that the PJVS circuit can be biased at higher microwave power and at lower temperature than were possible with the RDK-101DP cryocooler (Fig. 2). The gray zone, which is compatible with the cooling power requirement to bias all the subarrays, covers almost all of the data shown in Fig. 5. The ideal operating point was measured at 3.9 K and 24.5 dBm, with the smallest current step width measured at 1.96 mA. The dither current operating margin was 1.72 mA, when measured with the polarity reversal flat-spot method and biased with the worst case (maximum bias current) scenario (pppppppppnnpnpnpnpnpnpnp). The inset of Fig. 5 shows that the PJVS voltage remains quantum accurate up to 4.6 K, i.e., 700 mK above the set point temperature of 3.9 K. The flat-spot measurements are centered at zero dither current (not shown) even as the average bias current set points for the 23 subarrays decrease from ~8.6 mA at 3.9 K to ~8 mA at 4.7 K. Even with a temperature increase of 250 mK, the operating margin remains greater than 1 mA. These results confirm the ability of the half-watt cryocooler to operate a PJVS circuit with performance comparable with that obtained when the PJVS cryopackage is immersed in LHe.

VI. Temperature Stability

Temperature stability is a key component for operating a PJVS circuit on a cryocooler. The temperature stability of the cold plate is affected by variations of the dc bias, due to the time-constant response of the temperature regulation. In addition, the cooling performances of the cold head and compressor must remain stable. Fig. 6 shows two different scenarios in which the dc biases are changing. The temperatures reported in Fig. 6 were averaged over a period of 6.4 s to remove the 1.2 Hz and ~35 mK temperature oscillations of the cryocooler. Fig. 6(a) shows the temperature recorded for two stepwise approximated sine waves (4 Hz and 0.1 Hz) with peak amplitudes of 9.899 V. The overshoot (30 mK) is identical for the two waveform frequencies and results in a temporary reduction of the current operating margins of 0.07 mA (RDK-101DP cryocooler, Fig. 4). After about 7 min, the temperature controller compensates for the rms power dissipated by the dc bias and the cold plate temperature fluctuations become less than 4 mK, even for the lowest frequency of 0.1 Hz. This underdamped response to such a step

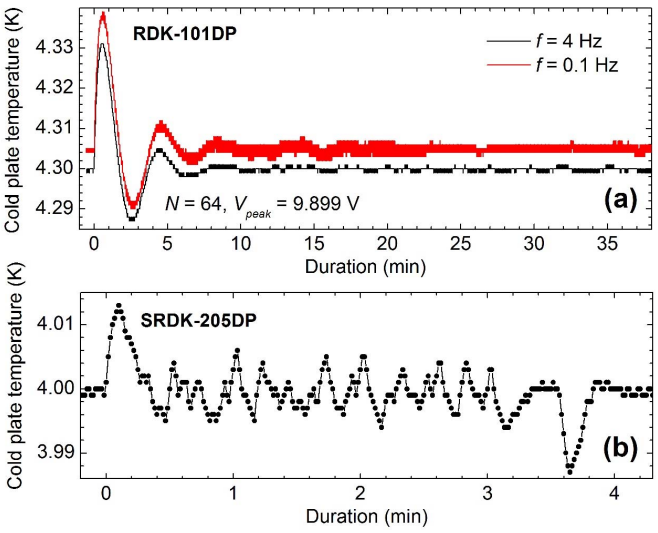

Fig. 6. Temperature stability measurement of (a) stepwise approximated sine waves with $N = 64$ voltage levels per period and two waveform repetition frequencies ($f = 4$ and $f = 0.1$ Hz), on the RDK-101DP cryocooler and (b) DVM gain calibration of the 10 V range on the SRDK-205DP cryocooler. For clarity, the $f = 0.1$ Hz curve in (a) is intentionally shifted with an offset of 5 mK.

function change in the dissipated rms power can be improved in the future through optimization of the proportional-integral-derivative (PID) parameters.

Another example that shows the effect of a varying dc current bias on the cryocooled PJVS is the act of calibrating the gain and linearity of a digital voltmeter (DVM). The measurement method alternates between positive, negative, and zero voltages to remove thermal EMF offsets of the PJVS output voltage leads. Fig. 6(b) shows that the temperature of the cold plate varies slightly during the random selection of voltages of the DVM gain calibration. Note that the two largest temperature deviations with a relative temperature variation of ± 14 mK around the set point temperature occur at the beginning and at the end of the measurement sequence. These temperature variations reduce the operating margins by 0.02 mA (SRDK-205DP cryocooler, Fig. 5).

In the future, we intend to improve the temperature stability and maximize the performance of the PVJS circuit by compensating for the changing dc bias. We can calculate the power dissipated by the dc bias in real time. When the power dissipated by the dc bias is reduced from maximum, we will employ a second heater located on the cold plate to apply an additional heat load, which would keep the total heat load constant. This approach would also simplify the search for the best bias parameters (temperature and microwave power) that would be compatible with the heat load generated when all the subarrays are biased.

VII. Conclusion

The constraint of limited cooling power when running a PJVS circuit on a cryocooler causes a small reduction of the operating current margins as compared with the same device operated in LHe. This emphasizes the importance of having PJVS circuits with large bias current margins, to guarantee successful operation on a cryocooler. We demonstrated that the quantum accuracy is preserved even if the temperature of the PJVS rises half a degree above the set-point temperature. The temperature stability achieved with the cryocoolers was better than ± 50 mK because of the supercritical helium buffer and the improved cryogenic packaging. This stability was maintained even in the presence of large variations in the heat load caused by necessary changes in the dc bias. Results obtained on a cryocooler with 500 mW of cooling power at 4 K show similar performance to that of the PJVS circuit operating in LHe. The next step will be to compare a PJVS system running on a cryocooler to a second PJVS system operating in LHe. After a modification of the PJVS control software to further improve the temperature regulation, we hope to realize a fully automated PJVS system.

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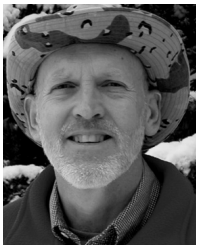
He joined the Quantum Voltage Project, National Institute of Standards and Technology, Boulder, in 2011. He has focused on the integration of Josephson voltage standards into low-capacity cryocoolers.

Anna E. Fox received her Ph.D. in Electrical Engineering from Drexel University in 2009. From 2009 to 2010 Dr. Fox was a National Research Council Postdoctoral researcher in the Optoelectronics Division at the National Institute of Standards and Technology in Boulder, CO where she worked fabricating superconducting transition-edge sensors for use at optical wavelengths. She continued her work in transition-edge sensor fabrication in the NIST Quantum Sensors Project where she fabricated arrays of TES bolometers for cosmic microwave background detection.

Dr. Fox has been with the NIST Quantum Voltage Project since 2013 pursuing the design and fabrication of voltage standard devices such as the Programmable Josephson Voltage Standard and the AC Josephson Voltage Standard.



Robert E. Schwall (M'91–SM'98) received the B.S. degree in physics from the St. Mary's University of Texas, San Antonio, TX, USA, in 1968, and the M.S. and Ph.D. degrees in applied physics from Stanford University, Stanford, CA, USA, in 1969 and 1972, respectively.

He was with IBM, Armonk, NY, USA, from 1984 to 1993, where he developed and patented a quench protection system for superconducting MRI magnets which was utilized worldwide for over 20 years. He served as the Manager of the Optical Systems Group at the IBM Thomas J. Watson Research Laboratory, Yorktown Heights, NY, USA, and also led a project addressing the packaging and cooling of CMOS circuits operating at cryogenic temperatures. From 1993 to 2003, he held various positions at American Superconductor, Boston, MA, USA.

Paul D. Dresselhaus was born in Arlington, MA, USA, in 1963. He received the B.S. degree in physics and electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1985, and the Ph.D. degree in applied physics from Yale University, New Haven, CT, USA, in 1991.

He joined the Quantum Voltage Project, National Institute of Standards and Technology, Boulder, CO, USA, in 1999, where he has been developed novel superconducting circuits and broadband bias electronics for precision voltage waveform synthesis and programmable voltage standard systems. He was with Northrop Grumman, Falls Church, VA, USA, for three years, where he designed and tested numerous gigahertz-speed superconductive circuits, including code generators and analog-to-digital converters. He also upgraded the simulation and layout capabilities at Northrop Grumman to be among the world's best. He has been a Post-Doctoral Assistant with the State University of New York at Stony Brook, Stony Brook, NY, USA, where he is involved in the nanolithographic fabrication and study of Nb-AlOx-Nb junctions for single-electron and SFQ applications, single-electron transistors and arrays in Al-AlOx tunnel junctions, and the properties of ultrasmall Josephson junctions.

Dr. Dresselhaus received two U.S. Department of Commerce Gold Medals for Distinguished Achievement and the IEEE Council on Superconductivity Van Duzer Prize in 2006.

Charles J. Burroughs, Jr. was born in 1966. He received the B.S. degree in electrical engineering from the University of Colorado Boulder, Boulder, CO, USA, in 1988.

He was with the National Institute of Standards and Technology (NIST), Boulder, where he was involved in superconductive electronics, including the design, fabrication, testing of Josephson voltage standards, and digital-to-analog and analog-to-digital converters. He has been with NIST as a permanent staff member since 1988. He has authored 45 publications and holds three patents in the field of superconducting electronics.

Mr. Burroughs received three U.S. Department of Commerce Gold Medals for Distinguished Achievement.

Samuel P. Benz (M'01–SM'01–F'10) was born in Dubuque, IA, USA, in 1962. He received the B.A. (*summa cum laude*) degree in physics and mathematics from Luther College, Decorah, in 1985, and the M.A. and Ph.D. degrees in physics from Harvard University, Cambridge, MA, USA, in 1987 and 1990, respectively.

He joined the National Institute of Standards and Technology (NIST), Boulder, CO, USA, in 1990, as a NIST/NRC Post-Doctoral Fellow, and became a permanent staff member in 1992. He has been the Project Leader of the Quantum Voltage Project at NIST since 1999. He was involved in broad range of topics within the field of superconducting electronics, including Josephson junction array oscillators, single flux quantum logic, ac and dc Josephson voltage standards, Josephson waveform synthesis, and noise thermometry. He has authored over 220 publications and holds three patents in the field of superconducting electronics.

Dr. Benz is a fellow of NIST and the American Physical Society, and a member of the Phi Beta Kappa and Sigma Pi Sigma. He was a recipient of an R. J. McElroy Fellowship to work toward the Ph.D. degree from 1985 to 1988. He has received three U.S. Department of Commerce Gold Medals for Distinguished Achievement and the IEEE Council on Superconductivity Van Duzer Prize in 2006.