A 100MHz Eight-Phase Buck Converter Delivering 12A in 25mm^2 Using Air-Core Inductors

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***Abstract*- We present a 100MHz eight-phase synchronous buck converter using air-core inductors. The voltage regulator (VR) chip was manufactured in a 90nm CMOS process and mounted on a flip-chip test package together with surface-mount inductors and decoupling capacitors. The measured peak efficiency is 84.0% for V_{in}/V_{out}=2.4V/1.5V and 79.3% for 2.4V/1.2V. The VR delivers a load current of 12A in an area of only 25mm^2 and 2.5mm height. This is the first demonstration of a high-frequency VR with air-core inductors, that reaches a record power density of 3.78kW/in^3.**

I. Introduction

Rising cost and motherboard real-estate, and the low impedances required for power delivery in modern computer platforms have spurred research of integrated high-frequency point-of-load DC-DC converters and voltage regulators [1, 2]. High switching frequencies of up to several 100MHz can be achieved in integrated voltage regulators (IVR's) implemented in high-speed digital CMOS processes, which enable multi-phase designs with very small inductances and minimum decoupling capacitance [2].

In this paper we present an integrated 100MHz eight-phase VR using discrete air-core inductors. The VR was implemented in a state-of-the-art 90nm CMOS technology originally developed for high-speed digital applications such as microprocessors [6]. The circuit design supports an input voltage of twice the maximum CMOS process voltage, V_{in}=2.4V=2x1.2V, using a cascode bridge. A fast transient-load chip mounted on the same package allows high-speed transient testing.

II. VR Specification, Architecture, and Assembly

Table 1 summarizes the specifications and measured performance of the VR (details of the measurements are given in Section 3). The chip dimensions are 4.5mm x 5.5mm. The actual VR circuit occupies only 10mm^2, whereas the remaining area is used by a transient-load circuit, so that the same chip can be used as a VR as well as a load. Figure 1 shows the assembled test package with the VR chip and the transient load chip on the top and the 0402-size inductors and 0603-size decoupling capacitors on the bottom of the package. The inductors are placed underneath the VR chip in order to minimize the package routing resistances. The maximum output current of 12A is limited by the inductors' 1.5A current rating. An RF launch on the top is connected to the output voltage at the load chip for high-speed transient droop measurement at a typical load step of 5A/100ps.

TABLE I
VR Specification & Performance

Technology	90nm CMOS
VR chip dimensions	4.5mm x 5.5mm
VR silicon area	10mm^2
Total VR height	2.5mm
Rated load current	12A
Input voltage	2.0–2.5V
Output voltage (VID)	0.8–1.6V
Efficiency at V_{in}/V_{out}=2.4V/1.5V	84.0%
Efficiency at V_{in}/V_{out}=2.4V/1.2V	79.3%
Switching frequency range	40–320MHz
Number of phases	8
Inductance per phase	0.9nH, 1.8nH
Decoupling capacitance	8.8µF
Output voltage ripple	<20mV
1st droop at ΔI/Δt=5A/100ps	+/- 100mV
2nd droop at ΔI/Δt=5A/100ps	+/- 30mV
Response time	50ns

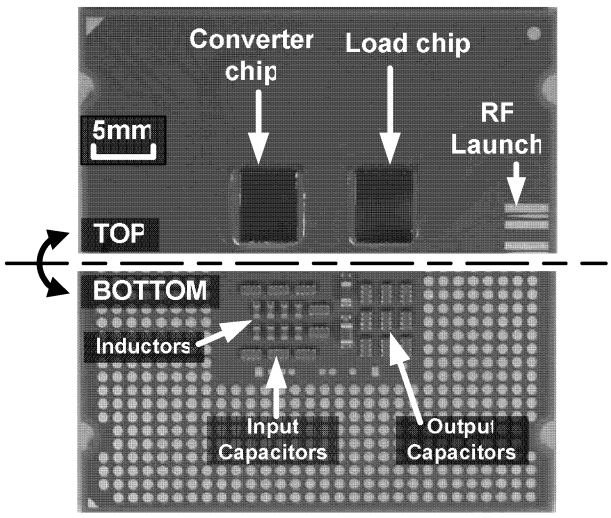

Figure 1. Assembled IVR test package with the converter and transient-load chips on the top, and decoupling capacitors and inductors on the bottom

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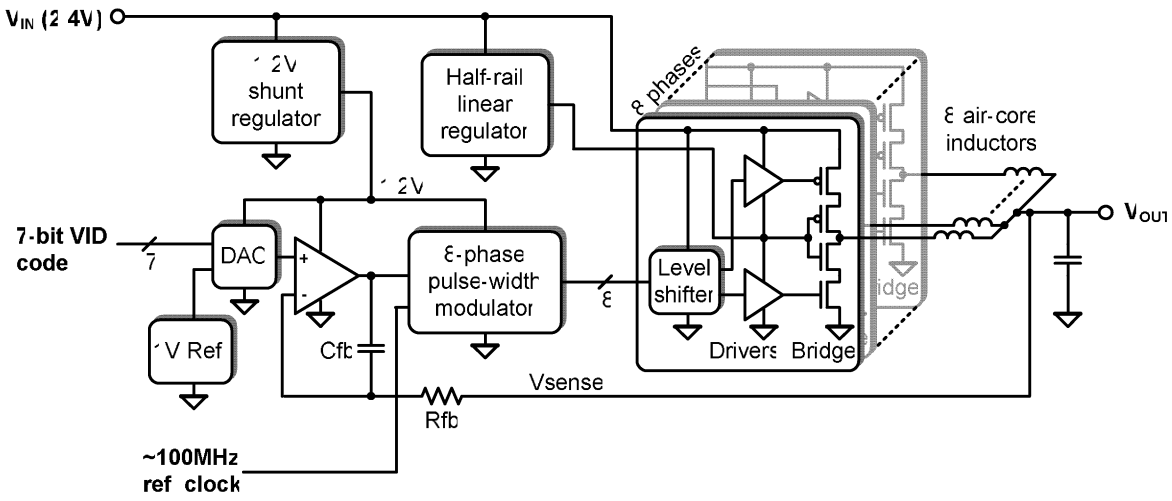

Figure 2. Eight-phase VR architecture

The VR architecture shown in Fig. 2 uses a 1.2V shunt regulator to safely supply the analog and control circuits at start-up and during normal operation. A half-rail linear regulator [5] supplies the bridge drivers and holds the center rail of the cascode bridge at $V_{in}/2$. The PMOS bridge drivers are controlled through level-shifters, so that none of the transistors' $|V_{GS}|$ or $|V_{GD}|$ exceed the CMOS process V_{max}, but the VR input voltage can be as high as $V_{in}=2V_{max}$. The supply currents of the PMOS drivers and of the NMOS drivers are comparable, so that the half-rail regulator has to supply only a small current.

While near-perfect ripple cancellation occurs at the output (V_{out}) for voltages close to a multiple of $V_{in}/8$, great care was taken in the floor-planning of the eight phases to reduce the input current ripple as much as possible without incurring large routing resistances on the chip: bridge transistors of opposite phases (i.e., with nearly 180° phase difference) were placed together to reduce input current ripple.

To generate the internal reference voltage a 1V precision bandgap reference is used together with a D/A-converter controlled by a 7-bit parallel VID code. The feedback loop is based on a simple integrator, and the effective ESR (series resistance) from V_{out} to ground is sufficient for stability. The gain-bandwidth product of the feedback loop and other test/debug functions of the VR can be digitally controlled through scan-chain flip-flops. The 8-phase PWM generator can be phase locked to an external reference clock in order to allow for averaging in voltage ripple measurements and to ensure consistent results in transient measurements. The PWM supports a frequency range of 40-320MHz, so that a wide range of inductances can be tested. The transient-load circuit can be programmed to toggle between two different load current values with a rise time of <100ps to mimic the worst-case load step of a modern microprocessor.

III. Test Setup and Experimental Results

Figure 3 shows the test setup with the heat spreader, heat sink, and fan attached to the VR on the test board. The chip was packaged in a 37.5 x 37.5 mm organic package, similar to those used for microprocessors. During measurements, the chip was placed in a zero insertion force LGA775 socket, also known as socket-T. The input voltage was provided by an external power supply via minifit-Sr connectors on the four-layer test board. A high-precision electronic load is used for efficiency measurements, whereas the load chip is used for high-speed transient measurements. The bridge outputs and other test signals are accessible through SMA connectors on the board. A computer connected to the board is used to

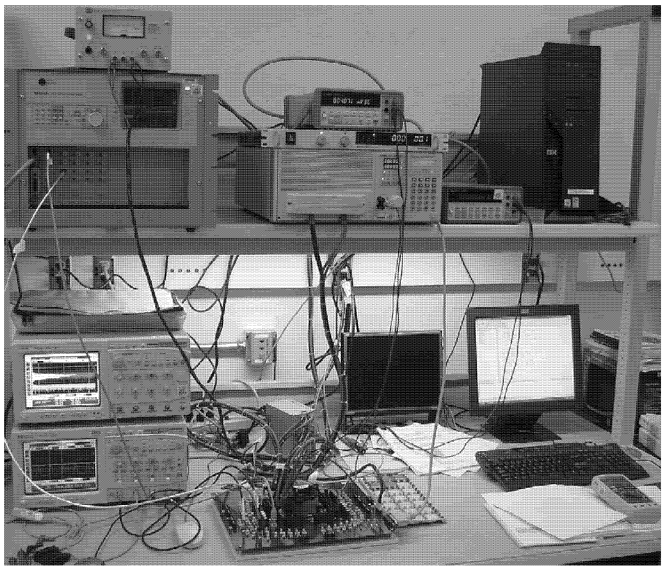

Figure 3. Test setup with test board, IVR with cooling attached, precision electronic load, power supplies, and DSO

program the functionality of the VR chip and of the transient-load chip through the chips' scan chains (a number of scan flip-flops connected as a shift register). A separate scan supply allows 'cold' programming before the VR chip is powered up.

Figure 4 shows a measurement of the eight bridge output voltages at 60MHz with V_{in}/V_{out} = 2.4V/1.2V, and 12A load current. Since the routing of V_{in} and ground is not identical for all phases, each of the waveforms shows a slightly different deviation from the ideal square wave due to input current ripple. The bandwidth limitation of the package does not allow to accurately measure the rise and fall times, which are typically a few 100ps.

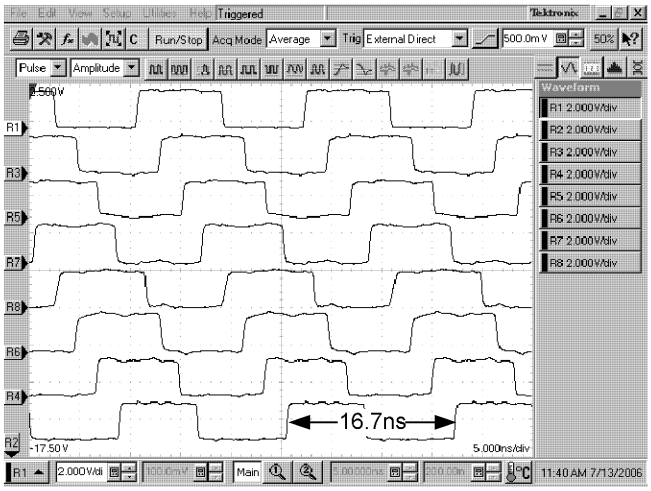

Figure 4. Bridge output voltages at 60MHz, V_{in}/V_{out} = 2.4V/1.2V, and 12A load current

Figure 5 shows the measured efficiency vs. load current for various inductors and output voltages. The peak efficiency for V_{in}/V_{out}=2.4V/1.2V is 79.3% at 12A load current and 84.0% for 2.4V/1.5V respectively. The optimal frequency for each case lies in a range of 60MHz to 100MHz, depending on the inductance: For 1.8nH, the optimum frequency is 60MHz, whereas for 0.9nH it is 80-100MHz, so that the ripple current does not change much. With L=1.8nH efficiency peaks at 10-12A and drops by only a few percent as the load current is increased to 20A. For reliability reasons the VR can only sustain an output current of 12A but for brief periods of time, it can deliver as much as 20A. This property is very important because the high-frequency components of load current of high-end CPUs often exceed the average, or thermally-limited, load current. With L=0.9nH efficiency peaks at a higher current, as expected, but even at higher currents the efficiency is lower than for 1.8nH, which suggests higher losses in routing parasitic resistance.

Figure 6 shows a transient droop measurement, where the load current is switched between 5A and 10A with <100ps rise time. The gain-bandwidth product of the feedback loop was set to 5MHz. The VR response time of 50ns allows to limit the second droop to +/-30mV, whereas the first droop of +/-100mV is largely determined by the decoupling capacitors' ESL and the load on-die capacitance. The limitation of the active droop control to the 'slow' second droop comes from the VR output inductance, which is 0.225nH for eight phases and 1.8nH/phase, and from the limited inductor voltage $\min(V_{in}-V_{out}, V_{out})$<1.2V, which ultimately limits the di/dt that can be sustained by the VR without decoupling to 5.3A/ns. Even so, this value is much higher than for conventional VRs, so that the output decoupling capacitance can be reduced by orders of magnitude.

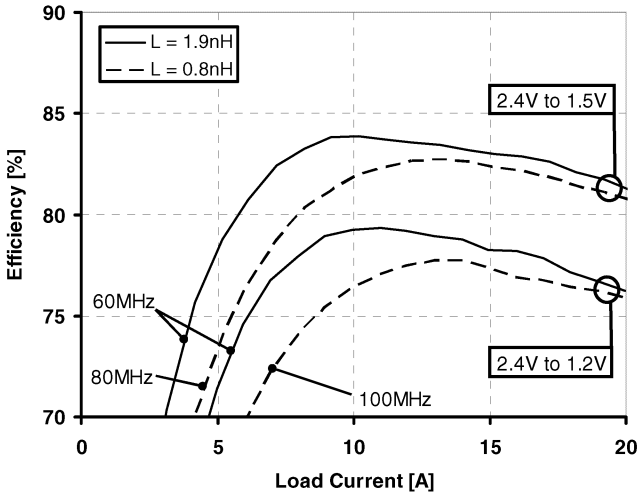

Figure 5. Efficiency vs. load current for various inductors and output voltages

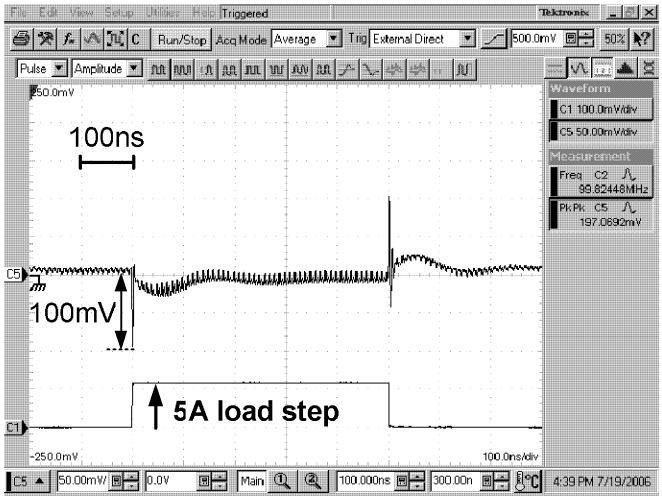

Figure 6. Transient output voltage droop for 5A load step at >50A/ns

TABLE II
COMPARISON TO PRIOR WORK.

	[1]	[2]	[3]	[4]	This work
Year	2004	2004	2006	2006	2006
V_{in}	2.8-5.5V	1.6V	2.375-5.5V	3.3V	2-2.5V
V_{out}	1-1.8V	0.8V	0.8-4.9V	1.5-2V	0-1.8V/2.5V
I_{out}	0.4A	0.5A	6A	0.2A	12A
Efficiency	92%	76%	91%	64%	84%
@ V_{in}/V_{out}	4V/1.5V	1.6V/0.8V	3.3V/2.5	2.8V/1.8V	2.4V/1.5V
Switching frequency	0.5-1.5MHz	220MHz	5MHz	45MHz	40-320MHz
# phases	1	4	1	2	8
Inductance / phase	10μH	15nH	?	11nH	0.8-1.6nH
Decoupling capacitance	47μF	2.5nF	50μF	6nF	8.8μF
Output voltage ripple	2mV	5mV	15mV	200mV	20mV

The comparison in Table 2 shows that our VR has the highest current rating reported for IVRs with air-core inductors so far [2, 4]. This is also the only integrated VR with eight phases. The cascode bridge was previously used in [1] at <1A current rating. Our work demonstrates that the cascode bridge can provide both a small chip area and acceptable efficiency at high output currents, despite using two FETs in series.

IV. SUMMARY

We demonstrated the first eight-phase integrated 100MHz synchronous buck converter using air-core inductors with a 12A current rating in 25mm^2 area and 2.5mm height, corresponding to a record-breaking power density of 3.78kW/in^3. The converter has a fast transient response and 79.3%-84.0% efficiency for output voltages of 1.2-1.5V.

ACKNOWLEDGMENT

The authors would like to thank M. Haycock, S. Borkar, K. Ikeda, D. J. Finan, C. M. Parsons, G. Gellman, K. Truong, B. Allesh, R.K Lava., M. S. Krishnamurthy, R. Mohan, H. T. Do, V. Pandey, M. W. Newman, M. A. Strunk, S. E. Davies, C. Hendricks, R. Chase, C. J. Sweeney, E. M. Katircioglu, and J. S. Ng for their invaluable contributions to this work.

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