Application Report
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Multiphase Buck Design From Start to Finish (Part 1)

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ABSTRACT

This application note covers the basics of multiphase buck regulators. A comparison versus single-phase regulators is presented before diving into a detailed design example aimed at powering the core rail of a generic networking ASIC setting up a second application note discussing printed-circuit board (PCB) layout techniques and performance testing.

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1 Introduction

In today's computing environment CPUs, FPGAs, ASICs, and even peripherals are growing increasingly complex and in turn so do their power delivery requirements. To handle the higher demands, multiphase regulators are becoming increasingly common on motherboards in many areas of computing from laptops and tablets to servers and Ethernet switches. Designing with these regulators is more challenging than using conventional switchers and linear regulators but the benefits of multiphase outweigh the complexity for high-performance power applications. This tutorial is designed to provide the necessary equations and guidance to get a new multiphase design up and running and ready for validation. After an overview of multiphase benefits, an in-depth design example of a multiphase buck regulator for an ASIC core rail is presented. Part 1 of this series focuses on the design specifications and component selection. Part 2 covers the PCB layout and basic performance testing.

2 Multiphase Buck Regulator Overview

A multiphase buck regulator is a parallel set of buck power stages as shown in Figure 1 and Figure 2, each with its own inductor and set of power MOSFETs. Collectively, these components are called a phase. These phases are connected in parallel and share both input and output capacitors. During steady-state operation individual phases are active at spaced intervals equal to 360° / n throughout the switching period where n is the total number of phases. Figure 2 shows a TPS53679 multiphase controller demonstration board and TI power stages for a six-phase design.

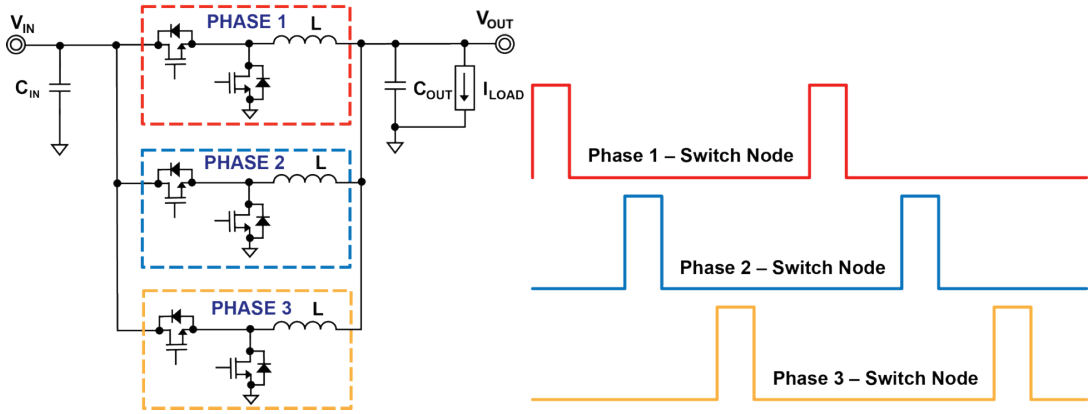

Figure 1. Multiphase Regulator Example

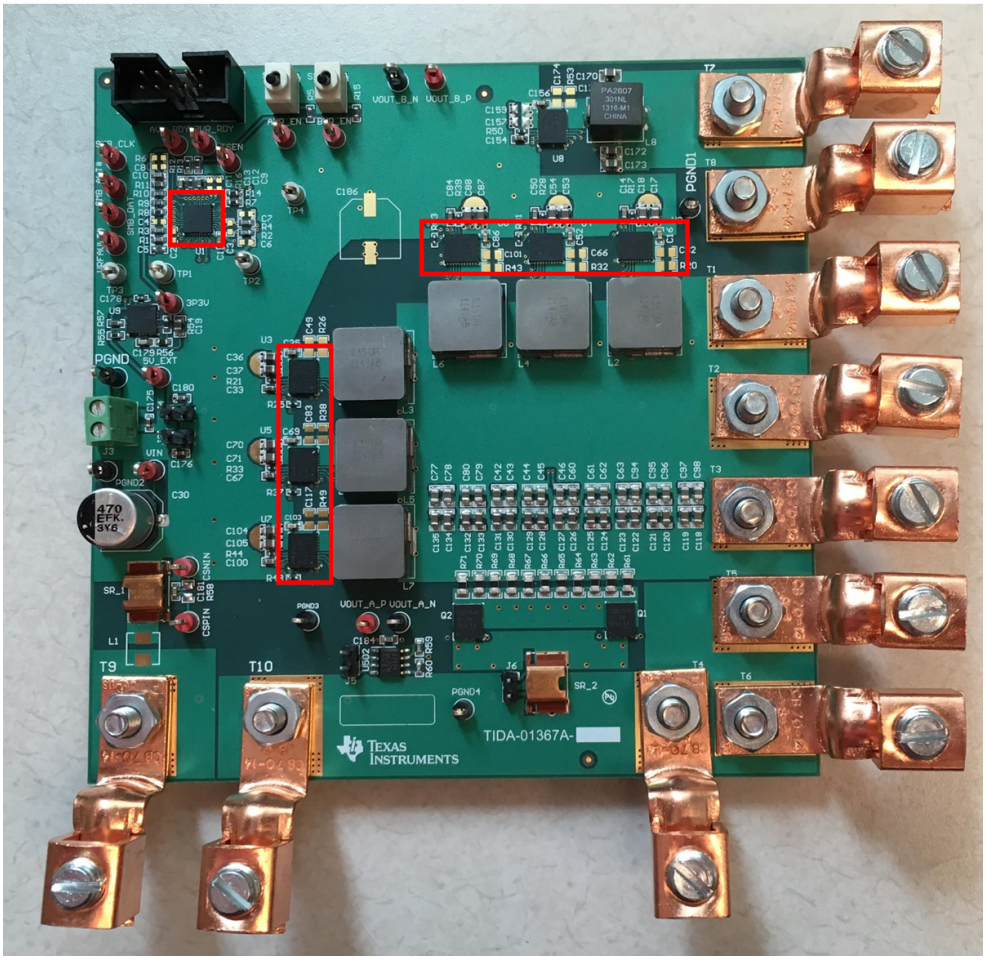

Figure 2. TPS53679 Demo Board With Controller and Power Stage ICs Highlighted

Today's controllers most commonly support applications needing two to eight phases. Techniques exist to extend the phase count to 12 or more but these are outside the scope of this document. As a general guideline, the maximum phase current should be kept between 30 to 40 A. Depending on budget, efficiency targets, and available cooling methods, the maximum phase current can be increased but it is highly recommended to do a thorough study of the ramifications before committing to the design.

3 Advantages of Multiphase Regulators

Compared to single-phase buck regulators, multiphase converters offer several key performance advantages that make them the default choice for high-power, high-performance applications:

a) Reduced input capacitance

b) Reduced output capacitance

c) Improved thermal performance and efficiency at high load currents

d) Improved transient over- and undershoot during load transients

3.1 Input Capacitance Reduction

Adding additional phases to a design decreases the RMS input current flowing through the decoupling capacitors thereby reducing the ripple on the input voltage, V_{IN}. Fewer capacitors are then needed to keep V_{IN} ripple within specifications. Self-heating effects within the capacitors themselves due to equivalent series resistance, ESR, are also reduced.

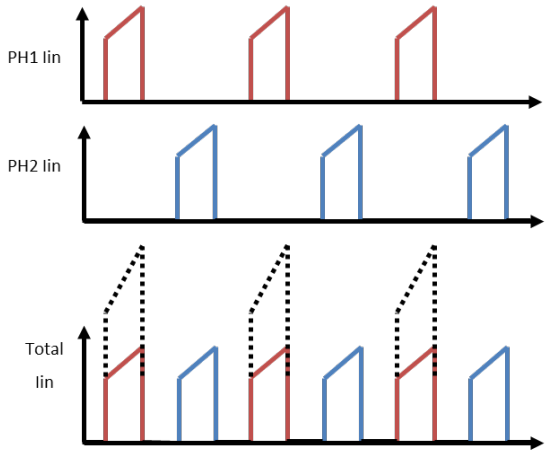

Figure 3. Input Current Waveforms

Figure 3 shows the input current waveforms for a two-phase buck compared to a single-phase design (dashed line). Lower RMS and peak currents from the addition of a second phase not only reduces the input capacitance, C_{IN}, but also provides less stress on the upper MOFET of each phase.

$$I_{CIN_{norm}}(RMS) = \sqrt{\left(D - \frac{m}{n}\right) \times \left(\frac{1+m}{n} - D\right)}$$

where

- $D = V_{OUT} / V_{IN}$
- n = # of phases
- m = floor (n × D) (1)

Calculating the normalized RMS input current of a regulator can be done using the formula in Equation 1. Plotting this equation as a function of duty cycle and phase number gives the curves in Figure 4. These graphs show a higher phase count can reduce the amount of current the input capacitors have to handle by 50% or more, depending on the duty cycle.

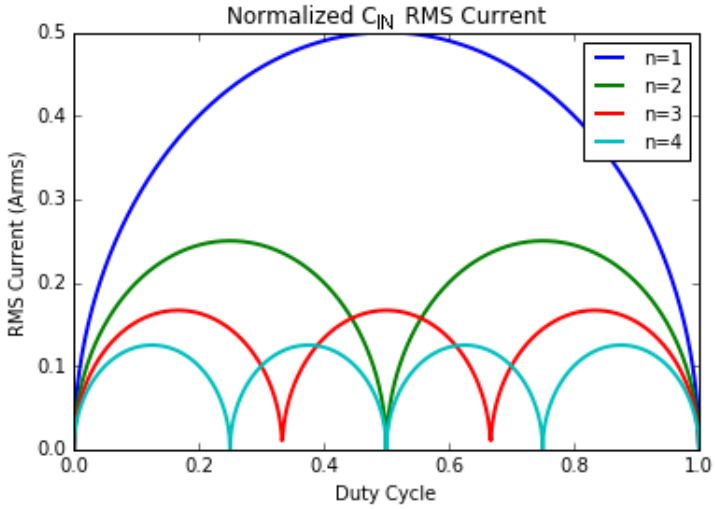

Figure 4. Normalized Input Capacitance RMS Current

At several points on the graphs in Figure 4, the input RMS current drops to zero as the individual ripple currents for each phase cancel one another out. While mathematically it may be possible set the phase number and duty cycle of a design to operate at a zero current point and eschew input caps altogether, in reality this is unachievable. Noise, line transients, load transients, and natural variations in the duty cycle make no input current ripple unrealizable in practice. Spacing between phases can reach several inches for 4+ phase designs causing PCB inductance to reduce the effects of ripple cancellation. Capacitors must always be used.

3.2 Output Capacitance Reduction

Because all phases of a multiphase design are tied together at the output node, the inductor currents of each phase are concurrently charging and discharging the output capacitors depending on whether or not a given phase is active. This charging and discharging produce one overall current, I_{SUM}, the AC portion of which gets absorbed by the output capacitance, C_{OUT}. Compared to the current of an individual phase I_{SUM} has a lower peak-to-peak value in steady state as shown in Figure 5. Smaller ripple current in the output capacitors lowers the overall output voltage ripple which in turn lowers the amount of capacitance needed to keep V_{OUT} within tolerance.

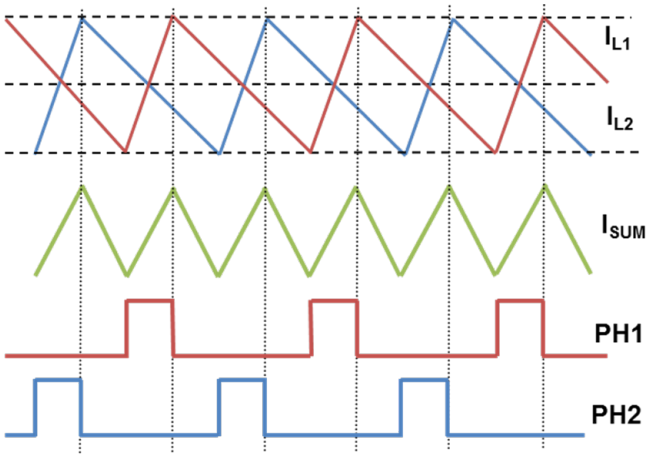

Figure 5. Inductor Ripple Current Waveforms

The normalized ripple current for the output capacitors is calculated using Equation 2 and plotted in Figure 6 for two-, three-, and four-phase buck converters. Setting n = 1 gives $I_{COUTnorm}$ = 1 for all duty cycles making Equation 2 invalid for single-phase calculations. Much like with the input capacitor current, at various duty cycles the currents of the inductors mathematically cancel out suggesting no output current ripple. Even when designed to operate at one of these points, a converter will always require some amount of output capacitance due to noise, transients, and duty cycle variation. However, for fixed output applications, operating near one of these zero points will lead to an optimal design with the fewest number of output capacitors.

$$I_{COUT_{norm}} = \frac{n}{D \times (1 - D)} \times \left(D - \frac{m}{n} \right) \times \left(\frac{1 + m}{n} - D \right) \quad (2)$$

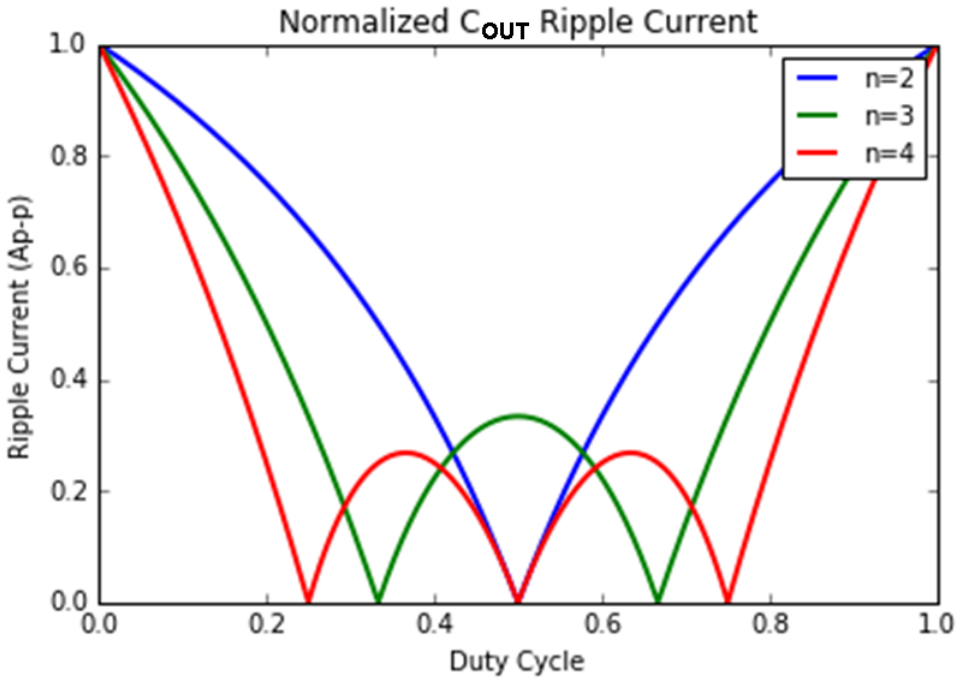

Figure 6. Normalized Output Capacitance Ripple

Unlike with input ripple cancellation, output ripple cancellation is less affected by the PCB layout. Usually, a significant number of output capacitors are tightly packed close to the CPU or point of load reducing the effects of parasitic inductance between components. Also, the inductor value of each phase dominates parasitics for all but the highest frequency designs.

3.3 Thermal Performance and Efficiency Improvements

Single-phase converters by definition have all the out power flowing through a single inductor and pair of FETs. Any power loss is contained solely within those components. For an application with greater than 100 A of output current, sourcing FETs and inductors rated to such large currents becomes difficult and expensive. Concentrating the entirety of the losses of a design into one small area of a PCB and set of components comes at an undesirable loss of efficiency.

Multiphase regulators spread power loss evenly across all phases. Since each phase is dealing with only a portion of the total output current selecting FETs and inductors becomes easier as less thermal strain is placed on these components. Regulator efficiency is also able to remain much higher over the entire load range when compared to an equivalent single-phase design. Performance is further improved by the reductions in C_{IN} and C_{OUT} discussed previously as lower ripple current in the capacitors produces less self-heating and lower power loss.

Modern DC/DC controllers allow for phases to be added and dropped, as needed, depending on the load current as shown in Figure 7. These add and drop points can be tuned to account for various FET and inductor combinations for optimal efficiency across many applications.

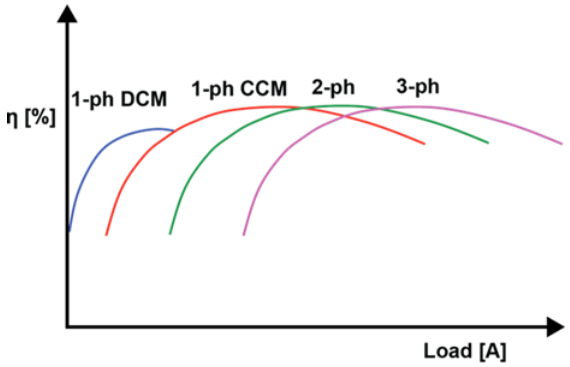

Figure 7. Efficiency vs Phase Number

At low currents fewer phases are used, down to a single phase operating in *Discontinuous Conduction Mode*, to minimize the FET switching losses and the current draw associated with the power stage and gate drivers of each phase. As the load current increases, conduction losses begin to dominate over switching loss and more phases are activated to keep the efficiency as high as possible. The optimum set point to turn on a phase occurs at the intersection of two efficiency curves. For example, phase two should be turned on where the falling single-phase efficiency curve crosses the rising two-phase efficiency curve.

Figure 8 depicts an efficiency curve taken of a five-phase design using the TPS53661 controller and CSD95372B power stage. The design called for V_{IN} = 12 V, V_{OUT} = 1.8 V, used a switching frequency of 600-kHz and 150-nH inductors. An efficiency > 90% is maintained from 5 A to 200 A, a feat which for all intents and purposes is impossible to do with only a single-phase buck.

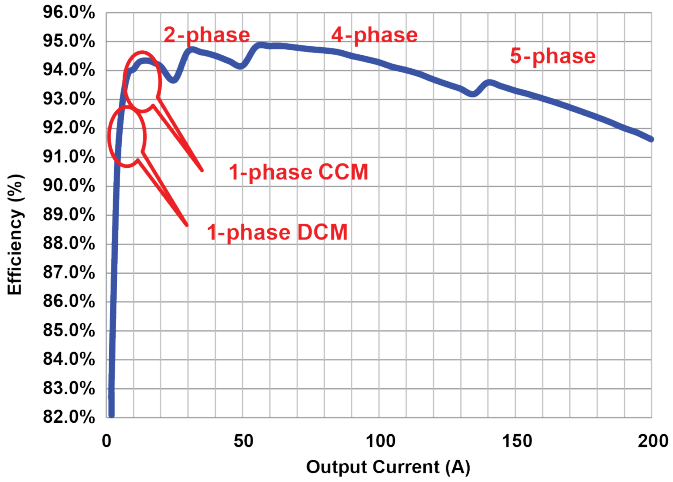

Figure 8. TPS53661 5-PH Efficiency Curve

3.4 Transient Response Improvements

In many high-performance applications, the capacitance requirements demanded by load transients far exceed what is called for to successfully hit DC ripple targets. During load transients, multiphase converters offer the advantage of needing fewer output capacitors to keep V_{OUT} within the specifications of a given design.

During a transient, a multiphase controller will overlap phases during a load step or turn all phases off during a load release, effectively putting the inductors in parallel with one another. This reduces equivalent inductance, LEQ, seen at the output node by a factor of n, where n is the total number of phases. With a smaller LEQ charge can quickly be supplied from the supply to the output caps reducing undershoot. Similarly, overshoot is reduced as less excess charge stored in the inductors is transferred to the output capacitors when the phases are all shut off.

4 Multiphase Challenges

While multiphase bucks offer many benefits over single-phase converters, they do present some challenges that must be overcome in order to successfully implement a design. Adding additional phases to a converter increases bill of materials (BOM) cost and PCB area. The price of more inductors and FETs must be weighed against the increased cost of sourcing more robust components and needing higher capacitor counts to implement a single-phase regulator instead. To minimize the greater board area needed for multiphase solutions, a balance between current capabilities and thermal performance versus overall phase number must be found.

Perhaps the biggest challenge of multiphase converters is phase management. In order to achieve the highest possible performance, current must be evenly balanced between active phases to avoid thermally stressing any one phase and provide optimal ripple cancellation. Additionally, phases must be quickly added or removed during transients to minimize excursions on the output voltage. Keeping the phases balanced requires a more sophisticated controller versus a single-phase buck. The sophistication comes from more sense lines, signal routing, current sense components, and so forth, that must be fed back to the controller in order to accurately balance phase currents.

Determining the phase current is traditionally done through a current sense resistor in series with each inductor or by utilizing the parasitic DC resistance (DCR) of the inductor. These methods are sensitive to component placement and signal routing making implementation difficult. The sense circuitry for each phase requires additional passive components to provide filtering and in the case of resistor sensing, adds an additional point of power loss. However, *Smart Power Stages*, such as the CSD95372B and CSD95490, have recently hit the market integrating current sense capabilities directly in the Driver-MOSFET package. When paired with a compatible controller, these ICs offer increased sense accuracy, eliminate a number of passive components, and require fewer differential signals, if any, to be routed across the PCB as seen in Figure 9.

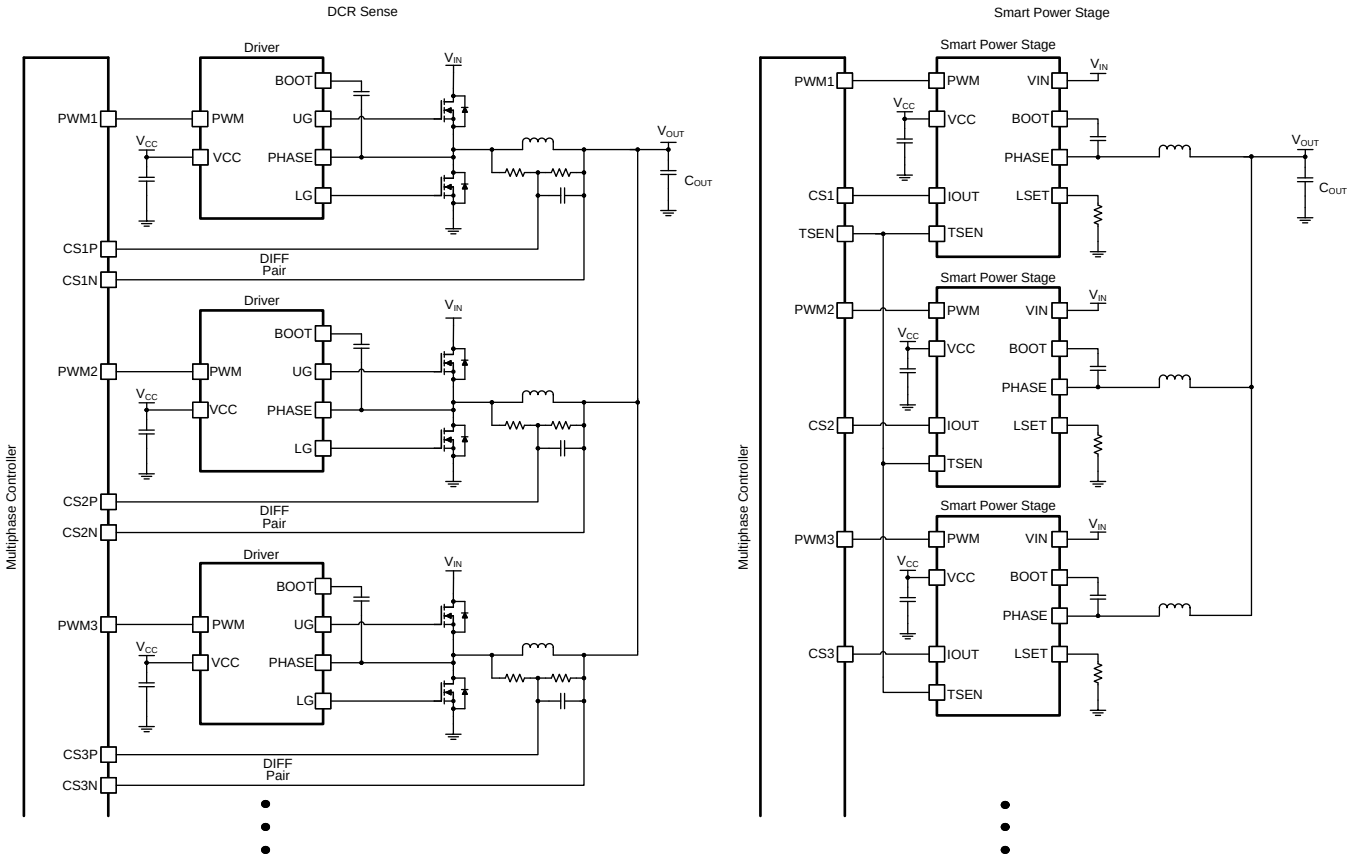

Figure 9. Simplified Comparison Between Current Sense Methods

5 Multiphase Design Example - Component Selection

To illustrate the benefits of multiphase buck regulators, a design using the specifications in Table 1 will be worked through from initial component selection, to PCB layout, and finally performance testing. Only the initial design will be discussed currently; layout and testing will be the subjects of a future application note. While working through the design process component count, efficiency, and layout complexity will be studied to strike a balance between performance and ease of implementation.

Table 1. Multiphase Design Targets

V_{IN}	12 V	Input Voltage
V_{OUT}	0.9 V	Nominal Output Voltage
I_{TDC}	200 A	Thermal Design Current
I_{MAX}	240 A	Max Current
I_{STEP}	150 A	Max Load Step
DCLL	0.5 mΩ	DC Load Line
$\Delta V_{OUT(DC)}$	±1%	V_{OUT} DC Ripple
$\Delta V_{OUT(AC)}$	±5%	V_{OUT} Transient Specifications
$\Delta V_{IN(DC)}$	240 mVpp	V_{IN} DC Ripple
$\Delta V_{IN(AC)}$	±360 mV	V_{IN} Overshoot and Undershoot
PMBus with Telemetry	Yes	Requires PMBus interface with V_{IN}, I_{IN}, V_{OUT}, I_{OUT}, and Temp readings

The requirements in Table 1 are typical specifications for the core voltage rail of a generic networking ASIC that may be found on an enterprise motherboard. Most of the specifications are fairly straightforward to anyone who has done a DC/DC switcher design before with the possible exception of the DC load line and PMBUS requirements.

With a DC load line, a buck regulator will essentially present itself as a fixed resistance to the output load. From the example numbers with a 200-A load being pulled by the ASIC, the nominal output voltage of 0.9 V will drop by 200 A × 0.5 mΩ, or 100 mV, to 0.8 V. This drops the power consumption of the processor by 20 W, easing strain on whatever heatsink or thermal solution is in place. This 20 W difference is not dissipated by the regulator; it simply is not drawn from the input supply. When the load current drops below 200 A the output voltage will rise accordingly. Load lines also make meeting the transient specifications much easier by reducing the amount of output caps needed, as discussed in Section 5.5.

Power Management Bus or, PMBus, is an open, industry standard interface based on I2C that can be found on many modern regulators, both single and multiphase. When implemented, the bus allows for easy adjustment of the output voltage, reporting of load conditions and FET temperature, as well as fault recording. If a digital or hybrid modulator is used in the controller, the PMBus can also be used to change the compensation of a converter during the testing and validation of the design.

5.1 Phase Count

With a 200-A TDC and 240-A maximum current, the design requires six phases to keep the individual phase currents below 40 A. Four- and five-phase designs result in TDC current levels that make power loss through the inductors and FETs difficult to manage. Conversely, a six-phase solution will only have 33 A flowing per phase at ITDC and 40 A while at I_{MAX}, providing a more manageable power loss scenario. The additional phases also provide a significant reduction in the amount of capacitors required to maintain regulation during load transients which can be seen in Table 6 of the *Design Summary* section.

5.2 Inductor

To choose an inductor, the switching frequency must first be decided. Frequencies around 300 kHz can provide low switching loss and high efficiency at the price of slow transient response as larger inductors are needed and the control loop bandwidth must be set lower than it otherwise would be at higher frequencies. Similarly, higher switching frequencies around 1 MHz suffer from greater switching loss but offer faster transient response.

For this design a switching frequency of 600 kHz will be used to provide a balanced tradeoff between transient response and efficiency. Using the standard buck design equation for calculating inductance and a ripple current target of 25%, an inductance of 0.138 µH per phase is calculated using Equation 3. Rounding towards the closest standard value gives an inductance of 0.15 µH per phase.

$$L = \frac{V_{OUT} \times (1 - D)}{f_{SW} \times I_{PP}} = \frac{0.9\ V \times \left(1 - \frac{0.9\ V}{1.2\ V}\right)}{600\ kHz \times \left(0.25 \times \frac{240\ A}{6}\right)} = 0.138\ \mu H \quad (3)$$

The inductor for this design was chosen from the popular IHLP line of inductors from Vishay Dale, specifically the IHLP-5050FD series. The 150-nH choke from this series has a typical DCR of 0.53 mΩ for low conduction losses as well as minimal AC loss that can be estimated using the Vishay online calculator. It is also thermally rated out to 55 A, providing margin since only 40 A per phase is expected.

The soft saturation curve of the powdered core on this inductor means the inductance remains relatively flat out to its saturation current rating before slowly rolling off, giving predictable performance over the range of expected operating conditions. Should a severe overcurrent event occur above the saturation current rating, a powdered core makes damage to the FETs and PCB much less likely than with a ferrite core. With a ferrite core the inductance will drop off quickly at the saturation point and the inductor essentially becomes a short which can pull a damaging amount of current.

5.3 Driver and Power MOSFETs

When working through a multiphase design there are three options available to a designer when it comes to deciding how to implement the controller, drivers, and power MOSFETs. The general pros and cons of each option are summarized in Table 2.

1) Discrete ICs for the controller, MOSFET drivers, and FETs

2) A controller with integrated drivers and discrete FETs

3) A driverless controller with the FETs and IC combined into one IC package

Option 1 offers the most design flexibility provided common footprints are used as the FETs and drivers can be swapped out easily if requirements change. The controller sends a PWM signal out to each driver IC which then converts the signal into the upper and lower gate drive signals for the MOSFETs. This option may also prove to be the cheapest since the individual ICs themselves are not highly integrated and sophisticated. However, going with an all discrete solution places the optimization of the driver-FET combination on the designer which increases the design complexity and may not be an option in a time-constrained scenario. Performance is much more affected by the PCB layout as opposed to more integrated solutions as there are a greater number of high-power nodes, drive signals, and sense lines to route around, along with additional parasitic elements.

Option 2 restricts the design freedom an engineer has since the drivers are paired with the controller and may not be suitable for driving all possible FETs. It also requires that the controller be located relatively close to the phases because the gate signals cannot be run for long distances without compromising performance. Layout area and complexity compared to an all discrete solution will depend on the phase count. As the phase count increases, the controller size balloons out as at least four additional pins per phase (*Upper Gate Drive*, *Lower Gate Drive*, *Phase Sense*, and *Boot*) are needed. For designs greater than two or three phases maintaining a proper layout with this option becomes difficult, at best. Finding a controller that supports a high phase count with integrated drivers may not be possible at all. Stacking multiple controllers together only further complicates the design.

Option 3 provides the easiest design and layout at the expense of BOM cost because of the high integration in the ICs. Only PWM signals are sent between the controller and driver-FET IC. No gate drive signal routing is required. This option also provides the optimal driver FET combination, with the lowest parasitics, translating into higher efficiency and a lower chance of shoot-through. If telemetry data for parameters such as input current, output current, and temperature are required, these features can be easily added into a driver-FET power stage instead of requiring additional discrete circuitry.

Table 2. Summary of Driver and FET Implementations

Design Parameter	Option 1 – Discrete Solution	Option 2 – Controller+Driver with FETs	Option 3 – Controller with Driver+FET
Flexibility	High	Average	Average
BOM Cost	Low	Phase # Dependent	High
Complexity	High	High	Low
Density	Low	Phase # Dependent	High
Performance	Average	Average	High

For the current design, Option 2 can be eliminated right away. A controller and driver package that can handle six phases does not exist and stacking multiple controllers adds unneeded complexity when controllers exist with six PWM outputs. Option 1 looks attractive because of the potential for a cheaper BOM cost but the PCB area needed to layout a driver, FETs, and associated passives, multiplied by six phases increases the board area and raises the cost of its production and assembly.

Choosing Option 3 reduces the overall component count and provides for the simplest board layout. It also eliminates the challenge of selecting an optimal pair of FETs and drivers to use for each phase, a topic that merits its own application note (Reference 7). Choosing a *Smart Power Stage* provides support for PMBus telemetry by integrating the needed circuitry on the chip.

Two possible options for power stages to consider for this design are the CSD95372AQ5M and the CSD95490Q5MC. Each stage is rated for a continuous current of 60 A and 75 A respectively, and supports the input/output voltages required, can switch at 600 kHz, and has a built in temperature monitor pin. Both parts come in low inductance packages to reduce parasitics that can affect steady-state switching and transient response. Finally, both are compatible with 3.3- and 5-V PWM signals allowing for more flexibility when choosing a controller IC.

Upon closer inspection, the CSD95490Q5MC proves to be a better fit for powering the networking ASIC. No DCR matching or resistor sense filter circuit is needed, thanks to the integrated bi-directional current-sense capability, removing six differential current sense signals routed back to the controller. An amplified, single-ended, current sense signal per phase is reported back instead. Because this current sense signal is amplified at the power stage it is much less susceptible to corruption from noise and other switching signals simplifying the circuit layout. A single resistor value on the LSET pin is all that is needed to properly configure this part. Additionally, a small amount of power loss is eliminated because a minimum sense resistor or DCR value is no longer needed to keep the sense signal SNR high enough to accurately balance the phase currents.

Most importantly, the CSD95490Q5MC has much lower power loss than the CSD95372AQ5M under identical conditions. Power loss is calculated at 33 A (TDC) and 40 A (maximum) and shown in Table 3 using the loss curves in both data sheets for the following conditions: V_{IN} = 12 V, V_{OUT} = 0.9 V, f_{SW} = 600 kHz, L = 150 nH, T_J = 100°C. With losses 1.4 W less per phase at TDC and 3 W less at maximum current, the CSD95490Q5MC is the clear choice.

Table 3. Power Stage Loss Calculations per Phase

Phase Current	CSD95490Q5MC	CSD95372AQ5M
33 A (TDC)	3.36 W	4.71 W
40 A (MAX)	4.56 W	7.54 W

5.4 Input Capacitors

Typically input capacitor requirements are met via a combination of multi-layer ceramic capacitors (MLCCs) and either aluminum or polymer electrolytic bulk capacitors. The MLCCs are sized to handle the RMS current and DC ripple in steady-state conditions while the bulk capacitance is used to provide charge and keep V_{IN} within tolerance during load transients.

To calculate the number of MLCCs simply multiply the RMS current value calculated from Equation 1 by the maximum current and divide by RMS current rating for an individual MLCC, rounding up to the nearest whole number. MLCC current rating can be obtained from the manufacturer's website. The RMS input current for this application is 19.9 Arms. A 22-µF, X5R, 1210, 16-V capacitor is rated at approximately 5 A of RMS ripple current at 600 kHz with a 20°C rise. Under these conditions, four total capacitors would be needed to carry the current.

Equation 4 calculates the amount of ceramic capacitance per phase needed to keep the input voltage ripple within its limits. In order to get a better estimate of the capacitance required, the duty cycle can be divided by the target efficiency, η, at the maximum phase current in order to get an adjusted duty cycle term, D_{ADJ}.

$$C_{INphase} = \frac{I_{PHASEmax} \times D_{ADJ} \times (1 - D_{ADJ})}{f_{SW} \times \Delta V_{IN(DC)}} = \frac{40\ A \times 0.882 \times (1 - 0.882)}{600\ kHz \times 240\ mVpp} = 22.3\ \mu F$$

where

- $D_{ADJ} = V_{OUT} / V_{IN} \times \eta$ (4)

Assuming a conservative efficiency of 85%, η = 0.85, at 40 A, a minimum of 22 µF is needed to keep V_{IN} within tolerance. You may initially think only one ceramic capacitor is needed per phase to hit both the ripple and RMS current requirements but the derating of each capacitor as a function of the DC bias voltage proves otherwise. From Figure 10 a single 1210, 22-µF capacitor will derate to approximately 15 µF with a 12-V bias. Taking this into account, two 22-µF capacitors per phase are needed to meet the input ripple requirements. Using identical capacitors from the same vendor but in a smaller 1206 package, a 22-µF capacitor will derate to about 5 µF at 12 V requiring four capacitors per phase instead of two.

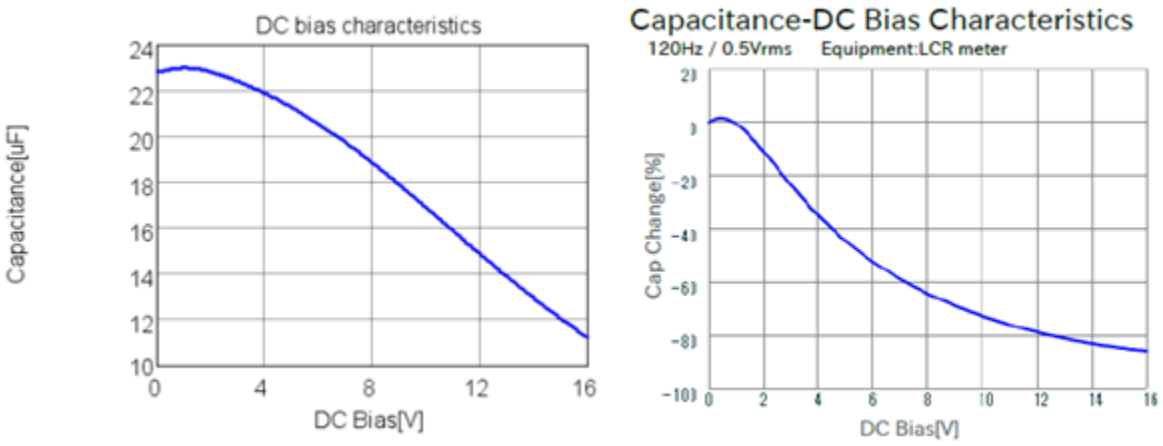

Figure 10. Capacitor Derating Curves Courtesy of Murata
Left:1210 Case, GRM32ER61C226ME20L, Right: 1206 Case, GRM31CR61C226ME15

Choosing a bulk capacitor to decouple the input voltage is more of an art than a science. Equations can give an engineer a starting point for a design but ultimately the performance must be verified on the board during validation. A tradeoff must be made between minimizing the ESR spike caused by the bulk capacitor while at the same time maintaining a high enough resistance to dampen any oscillations caused by ceramic capacitor ringing during a transient.

For this design, the process outlined in Reference 10 is used to get a starting bulk capacitance value assuming a 10-kHz bandwidth for the 12-V bus regulator. After completing the process, 550 µF should be the minimum capacitance with an ESR of less than 27 mΩ. Two 330-µF, 16-V, 20-mΩ Aluminum polymer capacitors will be used as bulk decoupling on V_{IN}.

Additionally, a single 1-µF, 0603 ceramic capacitor will be placed on each phase to help suppress ringing on the phase node and reduce the requirements of a snubbing circuit should testing reveal one to be needed.

5.5 Output Capacitors

Calculating the output capacitance requires taking into account both the DC ripple and AC transient specifications of an application. As previously discussed, the AC transient requirements are typically more demanding than the DC ripple specifications and will dictate how much total output capacitance is needed. Just as when choosing input capacitors, a mix of MLCCs and bulk caps are used.

Ceramic capacitors keep the output impedance of the converter low before the control loop can respond during fast transients, minimizing overshoot and undershoot. Bulk capacitors provide enough of a charge reservoir for the output voltage to stay within tolerance as the controller ramps the inductor current the new load current level.

Assuming minimal ESR and ESL in the capacitor network, the amount of output capacitance needed to handle the DC ripple can be calculated using Equation 5. In this equation, I_{PP} is the ripple current for a single phase of the converter as there is no inductor current cancellation in single-phase operation making it the worst-case scenario.

$$C_{Ripple} = \frac{I_{PP}}{8 \times f_{SW} \times \Delta V_{OUT(DC)}} = \frac{0.25 \times \frac{240\ A}{6}}{8 \times 600\ kHz \times (0.01 \times 0.9\ V)} = 214\ \mu F \quad (5)$$

Figure 11 and Equation 6 to Equation 9 explain the process behind calculating starting capacitance values needed to handle load transients. During a load step the inductance, L or L_{EQ} – depending on the total phase number, takes some amount of time, $t_{Undershoot}$, to slew to the high current level. In that time, an amount of charge equal to $Q_{Undershoot}$ is pulled from the output capacitors while V_{OUT} dips below its set point. Upon load release, excess charge in the inductor, $Q_{Overshoot}$, is dumped into the output capacitors during time $t_{Overshoot}$, causing V_{OUT} to swing above its regulation point.

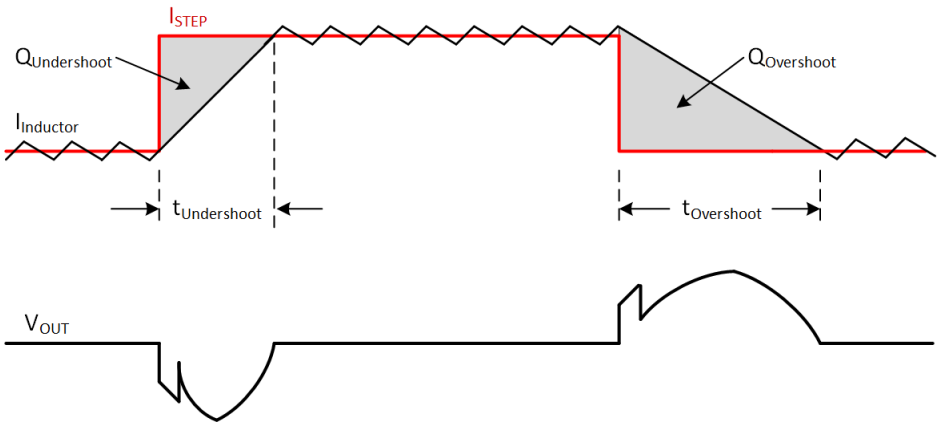

Figure 11. Load Transient Waveforms

$$t_{Undershoot} = \frac{L_{EQ} \times I_{STEP}}{V_{IN} - V_{OUT}} = \frac{\frac{150\ nH}{6} \times 150\ A}{12\ V - 0.9\ V} = 438\ ns \quad (6)$$

$$Q_{Undershoot} = \frac{1}{2} \times t_{Undershoot} \times I_{STEP} = \frac{1}{2} \times 438\ ns \times 150\ A = 32.85\ \mu C \quad (7)$$

$$t_{Overshoot} = \frac{L_{EQ} \times I_{STEP}}{V_{OUT}} = \frac{\frac{150\ nH}{6} \times 150\ A}{0.9\ V} = 4.3\ \mu s \quad (8)$$

$$Q_{Overshoot} = \frac{1}{2} \times t_{Overshoot} \times I_{STEP} = \frac{1}{2} \times 4.3\ \mu s \times 150\ A = 322.5\ \mu C \quad (9)$$

After calculating $Q_{Overshoot}$ and $Q_{Undershoot}$, finding the output capacitance is simply a matter of dividing the charge by the allowable swing on V_{OUT}. The current design specifies a DC load line which must be taken into account as shown in Figure 12. The total capacitance needed to handle the maximum transient of the application is calculated in Equation 10 for the load step and Equation 11 for the load release. For applications without a DC load line, simply set DCLL = 0.

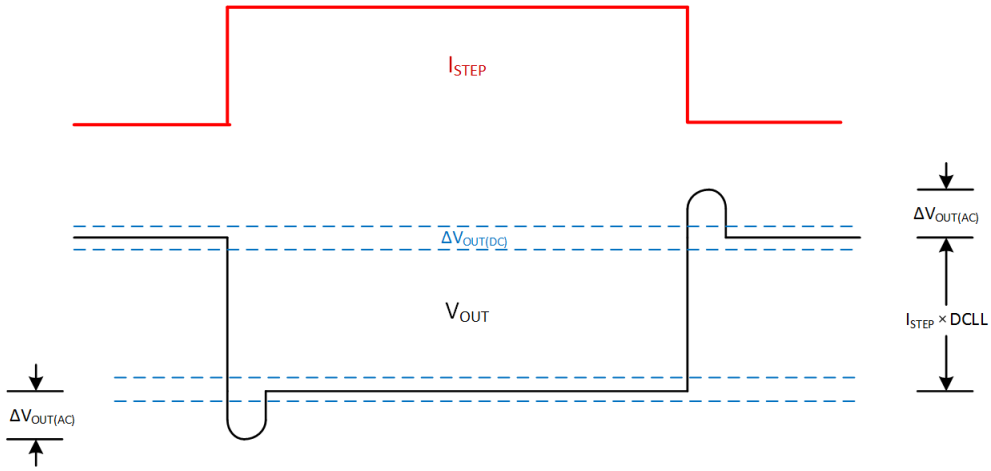

Figure 12. Load Transient with DC Load Line

$$C_{Undershoot} = \frac{Q_{Undershoot}}{\Delta V_{OUT(AC)} + I_{STEP} \times DCLL} = \frac{32.85\ \mu C}{0.05 \times 0.9\ V + 150\ A \times 0.5\ m\Omega} = 273.6\ \mu F \quad (10)$$

$$C_{Overshoot} = \frac{Q_{Overshoot}}{\Delta V_{OUT(AC)} + I_{STEP} \times DCLL} = \frac{322.5\,\mu C}{0.05 \times 0.9\,V + 150\,A \times 0.5\ m\Omega} = 2688\ \mu F \quad (11)$$

Comparing the values calculated for C_{Ripple}, $C_{Undershoot}$, and $C_{Overshoot}$ the load release dictates the amount of capacitance needed to keep V_{OUT} within regulation. $C_{Overshoot}$ comes out to be much greater than $C_{Undershoot}$ because during load release, less energy is required by the processor and so any excess stored in the inductor gets transferred to the output capacitors causing V_{OUT} to overshoot. During a load step the processor is pulling energy from the capacitors and the energy stored in the inductor refills them helping mitigate undershoot.

Table 4 and Table 5 are used to come up with a mix of output capacitors that can satisfy the transient requirements while balancing component count and BOM cost. Table 4 compares the prices and specifications of several popular capacitor options while Table 5 looks at combinations of capacitors that meet the necessary requirements and can be used as a starting point for the design. Depending on bench results, the amount and type of capacitors may be adjusted. The total capacitance of each option is set higher than $C_{Overshoot}$ to provide margin and account for derating on the MLCCs. Since the DC bias on each capacitor is lower than on the input side of the regulator, less derating occurs and the capacitors still retain most of their nominal capacitance.

Table 4. Output Capacitor Options

Capacitor Type	Capacitance	Specifications	Price/1000 Units
Ceramic	22 µF	0805, 6.3 V, X5R	$0.054
Ceramic	47 µF	0805, 6.3 V, X5R	$0.131
Organic Polymer	470 µF	V-Case, 2.5 V, 6 mΩ	$1.357
Organic Polymer	680 µF	D-Case, 2.5 V, 6 mΩ	$2.537

Table 5. Output Capacitor Solution Comparison

Capacitor Mix	Total Capacitance	Component Count	Price
3 × 470 µF + 20 × 47 µF + 25 × 22 µF	2900 µF	48	$8.04
1 × 680 µF + 32 × 47 µF + 35 × 22 µF	2950 µF	68	$8.62
2 × 680 µF + 20 × 47 µF + 20 × 22 µF	2850 µF	47	$9.04
47 × 47 µF + 35 × 22 µF	2980 µF	82	$8.05

From Table 5 a combination of 470-µF bulk capacitors and MLCCs provides the best balance between component count and price. For applications that may require an all ceramic solution the component count increases substantially though not necessarily at the expense of BOM cost.

5.6 Controller

Studying the TPS53679 Dual-Channel Multiphase Controller data sheet (SLUSC47) proves it to be a good fit for this ASIC core rail. The D-CAP+ modulator is optimized for multiphase control and keeping the current balanced between phases. Six PWM channels offer a great deal of design flexibility to work with a variety of power stages, including the chosen CSD95490, while minimizing the size of the controller package. Support for PMBus communication checks the box to meet the telemetry specification of the design. The PMBus also enables tuning functionality of the phase add and drop points so that optimal efficiency can be achieved over the whole load range. For a deeper look into the D-CAP+ modulator see Reference 2 and Reference 12.

As an added bonus, the controller also supports full digital compensation through the PMBus making tuning the design on the board much easier than reworking components on an analog compensation pin. Finally, the second single-phase buck regulator can be used to power any auxiliary rails that the ASIC may require saving money and PCB area.

5.7 Design Summary

Table 6 gives a comparison of the current six-phase design compared to alternatives using one, two, or four phases with the same power stage and inductor. Fewer phases are not a feasible option for this design when looking at the results. Power loss can be mitigated to some degree by selecting components rated to the higher currents but between component cost, power loss concentration, plus modifications to fans or heatsinks, any benefits from these changes will likely be equivalent when compared to a six-phase solution.

The output capacitance to hit the overshoot requirement drops by thousands of micro-Farads as the phase count increases. Input ceramic capacitor count is also more manageable with a higher phase count.

As an academic exercise, the benefit of a DC load line is shown for each case by recalculating the value of $C_{Overshoot}$ after setting DCLL = 0 from Equation 11. Without a load line, V_{OUT} cannot swing more than 45 mV, 5%, in either direction during a 150-A transient. The ability of the ASIC to handle a shallow 0.5-mΩ load line on its core voltage rail allows V_{OUT} to swing an additional 75 mV for the same transient for a total of 120 mV, drastically reducing the output capacitance.

Table 6. Multiphase Design Comparison

Phases	1	2	4	6	
I_{IN} (Arms)	63.2	42.8	27.5	19.9	RMS Input Current
$I_{MAX,PH}$ (A)	240.0	120.0	60.0	40.0	Max Current per Phase
$I_{TDC,PH}$ (A)	200	100	50	40	Thermal Design Current per Phase
$P_{FET,TDC}$ (W)	-	-	6.81	3.36	FET Loss @ TDC
$P_{IND,TDC}$ (W)	-	7.04	2.07	1.15	Inductor Loss @ TDC
$C_{IN,MLCC}$ (µF)	134.1	57.0	33.5	22.3	Ceramic Input Capacitance per Phase
$C_{Overshoot}$ (µF)	15,688	7,875	3,969	2,668	Output Capacitance to Meet Overshoot
$C_{Overshoot}$ (µF)	41,833	21,000	10,583	7,111	Output Capacitance to Meet Overshoot, no load line

Table 7 displays a brief summary of the major design decisions and components selected for this case study. These components will be used in Part 2 of this multiphase series when the PCB is laid out and tested in the lab.

Table 7. Case Study Design Summary

V_{IN}	12 V
V_{OUT}	0.9 V
I_{MAX}	240 A
TDC	200 A
Phase Count	6
Inductor	150nH, 0.53 mΩ, 55 A I_{TEMP}
FETs	CSD95490
TDC Power Loss	FETs - 20.1 W
	Inductors - 6.87 W
TDC Eff. Estimate	86.9%
C_{IN}	2 × 330 µF, 10 mΩ, 16 V, Al Poly
	12 × 22 µF, 1210, X5R, 16 V
C_{OUT}	3 × 470 µF, 6 mΩ, 6.3 V
	20 × 47 µF, 0805, X5R, 2.5 V
	25 × 22 µF, 0805, X5R, 6.3 V
Controller	TPS53679

6 Conclusion

After an introduction to the pros and cons of multiphase regulators, a paper design of a high-performance, six-phase buck has been completed. During the design tradeoffs between component count, power loss, ease of design, and BOM cost were made resulting in an optimal solution. Looking forward to the next portion of the tutorial, a PCB based on this design will be completed and tested on the bench against the target specifications. For more information on TI's multiphase controllers, both with and without PMBus, visit the web portal referred to in Reference 11.

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