Année 2015 *N° ordre*

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THESE

Design and Implementation of High Frequency 3D DC-DC Converter

sous la direction du Professeur Bruno **Allard**

Présentée devant

L'Institut National des Sciences Appliquées

pour obtenir

Le grade de docteur

Spécialité : "Génie Électrique"

préparée au laboratoire AMPERE dans le cadre de
l'École Doctorale "Électrotechnique Électronique Automatique"

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Soutenue le 11 Décembre 2015

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AW Active Well.

BJT Bipolar Junction Transistor.

CAD Computer Aided Design.

CCM Continuous Conduction Mode.

CMOS Complementary Metal-Oxide-Semiconductor.

DCM Discontinuous Conduction Mode.

DRC Design Rule Check.

DVS Dynamic Voltage Scaling.

ECU Engine Control Unit.

EEF Efficiency Enhancement Factor.

EMI ElectroMagnetic Interference.

ESD Electro-Static Discharge.

ESL Equivalent Series Inductance.

ESR Equivalent Series Resistance.

FIVR Fully Integrated Voltage Regulator.

FoM Figure of Merit.

I/O Inputs/Outputs.

IC Integrated Circuit.

JFET Junction Field-Effect Transistor.

LDMOSFET Laterally-Diffused MOSFET.

LDO Low Drop-Out.

LRF Losses Reduction Factor.

MIM Metal-Insulator-Metal.

MLCC Multi-Layer Ceramic Capacitor.

MOM Metal-Oxide-Metal.

MOS Metal-Oxide-Semiconductor.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

PCB Printed Circuit Board.

PFM Pulse Frequency Modulation.

PICS Passive Integrated Connecting Substrate.

PLS Post Layout Simulation.

PMIC Power Module IC.

PMU Power Management Unit.

PowerSiP Power Supply in Package.

PowerSoC Power System on Chip.

PWM Pulse Width Modulation.

RMS Root Mean Square.

SCR Space-Charge Region.

SiP System in Package.

SMD Surface Mounting Device.

SMPS Switched-Mode Power Supply.

SMU Source-Measurement Unit.

SoC System on Chip.

SPICE Simulation Program With Integrated Circuit Emphasis.

SRF Self-Resonant Frequency.

VNA Vector Network Analyzer.

ZCS Zero Current Switching.

ZVS Zero Voltage Switching.

Acknowledgements

This work was supported by the European Commission through the Seventh Framework Programme (FP7), under the project grant PowerSWIPE No. 318529.

Besides the funding, this work would not have been possible without the help and support of many people. This include many people from Ampere Laboratory, and also partners of the PowerSWIPE project

This list of people starts with my PhD advisor, Bruno Allard, who talked me into doing a PhD while he was one of my university teacher. Looking back, I'm glad I followed his advice. Bruno Allard was also of very good technical advice, with a strong enthusiasm, that sometimes needed to be mitigated with my finite working capabilities.

Next in line is Christian Martin, the co-supervisor of my PhD. He helped me on lot of things, that I won't go through here as I don't want to make this too tedious. He was also a very good supervisor outside the working environment, and he definitely taught me the true meaning of the word *cohesion*.

I have to acknowledge the work of Pascal Bevilacqua, who helped me a lot on the development of the test-bench (I even could say that he was the one doing it, I was the one trying to help), and did a very good work, even with my last-minute small change requests, that were not that small in the end.

I also want to thank the secretaries of the laboratory, whom I bothered with several requests, Michelle (for the most of the time), Sandrine, Maguy, Edwige and Anne-Cécile. They were my interface to the obscure maze that is

the administrative world, and thanks to them I managed to not get lost and to stay on the bright side of things.

I'd like to thank all the people from the laboratory (with an emphasis on people from Léonard de Vinci and Oméga buildings). There was a great atmosphere in the office, thanks to the people filling it through the years. It won't go through the exhaustive list of everyone here as I'm too afraid to forget someone; but if you want to be thanked in person, please let me know and we can do that around a drink! It was a pleasure to be part of this lab, and to meet all these students, post-docs and researchers. I'll remember the endless, purposeless and yet passionate debates during coffee breaks.

On the project side of things, I'd like to thank all the partners of the PowerSWIPE consortium, for giving me the opportunity to be a full contributor to the project. A special thanks goes to Cian Ó'Mathúna from Tyndall, who did a great job leading this project and made me feel like a valued contributor to the overall project. I also want to thank the people from Infineon, Anamaria Anca and Christoph Sandner, and also Herbert Gruber for its valued help and feedback on the layout. I also thank Frédéric Vorion from IPDiA, for his input and his good work on the interposer. I thank also the people from UPM, José Cobos, Pedro Alou and Jésus Oliver for their valuable knowledge on converter architecture. I also address thanks to people from Tyndall, Santosh Kulkarni for the designed inductors, and Nicolas Cordero, for the overall project management.

Last but not least, I want to thank Aleksandar Prodic and Bernhard Wicht, who kindly accepted to review this manuscript, as well as Marc Cousineau, José Cobos and Cian Ó'Mathúna for being part of my jury, and Yves Lembeye for being the chair of this jury.

Remerciements

Ce travail a été supporté par la Commission Européenne via le septième programme-cadre (7ePC), via le financement du projet PowerSWIPE No. 318529.

En dehors du financement, ce travail n'aurait pas été possible sans le support et l'aide précieuse de nombreuses personnes. Ceci inclut à la fois les personnes du laboratoire Ampère et les partenaires du projet PowerSWIPE.

En haut de la liste se trouve mon directeur de thèse, Bruno Allard, qui me convainquit de me lancer dans un doctorat lorsqu'il était encore un de mes enseignants. Avec le recul, je me dis que ce n'était pas un mauvais conseil. Bruno Allard a été de très bon conseil du côté scientifique, avec un fort enthousiasme, qui dut parfois être modéré en raison de ma capacité de travail non infinie.

Le suivant est Christian Martin, co-encadrant de mes travaux de thèse. Il m'a aidé sur de nombreux aspects, que je ne développerai pas ici dans un souci de concision. Il fut aussi un encadrant digne de ce nom en dehors du travail, et m'a notamment fait comprendre l'authentique sens du mot *cohésion*.

Je suis fortement reconnaissant du travail de Pascal Bevilacqua, qui m'aida énormément sur le développement du banc de mesure (pour être honnête je dirai même que c'était plutôt lui qui faisait le travail, et moi qui essayait de l'aider). Il a fait du très bon travail, tout en prenant en compte mes petites modifications de dernière minute (pas si petites d'ailleurs).

Je tiens à remercier les secrétaires du laboratoire, que j'ai ennuyée avec nombre de requêtes, Michelle (pour la plupart du temps), Sandrine, Maguy,

Edwige et Anne-Cécile. Elles étaient mon interface avec les méandres obscurs que sont l'administration, et grâce à elles j'ai pu rester du côté lumineux sans avoir à m'égarer dans la pénombre.

Je voudrais aussi remercier toutes les personnes du laboratoire (principalement celles des bâtiments Léonard de Vinci et Oméga). Il y avait une très bonne ambiance dans le bureau, et ça grâce à toutes les personnes présentes au cours du temps. Je ne vais pas me lancer dans une liste exhaustive car je ne me pardonnerais l'oubli d'une personne ; cependant si vous souhaitez un remerciement personnel, faites-le moi savoir et on pourra faire ça autour d'un verre ! C'était un plaisir de faire partie de ce laboratoire, et de rencontrer tous ces étudiants, post-docs et chercheurs. Je n'oublierai pas les fameux débats, tout aussi inutiles que passionnés, qui s'instauraient durant les pauses café.

Du côté du projet, je souhaite remercier tous les partenaires du consortium PowerSWIPE de m'avoir donné l'opportunité d'être un contributeur à part entière de ce projet. Une mention spéciale va à Cian Ó'Mathúna, de Tyndall, dont j'ai fortement apprécié la direction et l'animation du projet, et qui me donnait le sentiment de contribuer utilement au projet. Je tiens aussi à remercier les personnes d'Infineon, Anamaria Anca et Christoph Sandner, ainsi que Herbert Gruber pour son aide et ses commentaires précieux vis à vis du dessin des masques. Je remercie aussi Frédéric Voiron d'IPDiA, pour son apport et son travail au niveau de l'interposeur. Je remercie aussi les personnes de l'UPM, José Cobos, Pedro Alou et Jésus Oliver pour leurs connaissances appréciées sur les architectures de convertisseur. J'adresse aussi des remerciements aux personnes de Tyndall, Santosh Kulkarni pour la conception des inductances, et Nicolas Cordero pour la gestion globale du projet.

Et finalement, je tiens à remercier Aleksandar Prodic et Bernhard Wicht, qui ont aimablement accepter de rapporter ce manuscrit, ainsi que Marc Cousineau, José Cobos et Cian Ó'Mathúna pour avoir pris part à mon jury, et Yves Lembeye pour en avoir été le président.

Dissemination

The presented work has been disseminated through various conference and journal publications, as well as miscellaneous contributions to workshops, conferences, etc. All the dissemination work is listed in the following sections.

Conferences

- Florian Neveu, Christian Martin and Bruno Allard, "Review of High Frequency, Highly Integrated Inductive DC-DC Converters", in *8th International Conference on Integrated Power Electronics Systems (CIPS)*, **2014**.

- Cian Ó'Mathúna et al., "Power Supply With Integrated PassivEs - The EU FP7 PowerSWIPE Project", in *8th International Conference on Integrated Power Electronics Systems (CIPS)*, **2014**.

- Florian Neveu, "Composants passifs pour convertisseurs en 2.5D à très forte contrainte d'intégration", in *Journée des Jeunes Chercheurs en Génie Électrique (JCGE)*, **2015**.

- Florian Neveu, Christian Martin, Bruno Allard, Pascal Bevilacqua and Frederic Voiron, "Design of a highly integrated, high frequency, low power DC-DC converter with cascode power stage with a 2.5D approach", in *9th International Conference on Integrated Power Electronics Systems (CIPS)*, **2016**. [accepted]

Journals

- Florian Neveu, Bruno Allard, Christian Martin, Pascal Bevilacqua and Frederic Voiron, "A 100 MHz, 91.5 % peak efficiency Integrated Buck Converter with a Three-MOSFET Cascode Bridge", in *Power Electronics, IEEE Transactions on*, **2015**.

- Florian Neveu, Bruno Allard and Christian Martin, "A Review of State-of-the-art and Proposal for High Frequency Inductive Step-Down DC-DC Converter in Advanced CMOS", in *Analog Integrated Circuits and Signal Processing*, **2016**.

Miscellaneous

- Florian Neveu, "Design of a Highly Integrated, High Frequency, Low Power DC-DC Converter with Cascode Power Stage", in the *WYMPhD forum* of *21st IEEE International Conference on Electronics Circuits and Systems (ICECS)*, **2014**.

- Bruno Allard, Florian Neveu and Christian Martin, "State-of-the-art of high switching frequency inductive DC-DC converters in SoC context", in *International Power Supply on-Chip Workshop (PowerSoC)*, **2014**. [presentation only]

- Florian Neveu, Bruno Allard and Christian Martin, "Power stage design and optimization for low power, high frequency, integrated DC-DC converter", in *International Power Supply on-Chip Workshop (PowerSoC)*, **2014**. [poster only]

- Florian Neveu, "Review of high frequency, highly integrated inductive DC-DC converters: descriptive trade-offs in integrated DC-DC converters", in *ECPE PowerSoC Workshop µPE: Powering Low-power Systems*, **2015**. [presentation only]

- Cian Ó'Mathúna, Santosh Kulkarni, José A. Cobos and Bruno Allard, "Power Supply on Chip", Professional Education seminar in *29th and*

30th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), **2014, 2015**. [contributions]

Abstract

Ultimate integration of switch-mode power converter relies on two research paths. One path investigates the development of switched-capacitor converters. This approach fits silicon integration but is still limited in terms of power density when targeted peak power is quite important. Inductive DC-DC architectures of converters suffer by the values and size of passive components. This limitation is addressed with an increase in switching frequency. Increase in switching losses in power switches leads to consider advanced technological nodes. Consequently, the capability with respect to input voltage is then limited.

Handling 3.3 V input voltage to deliver an output voltage in the range of 0.6 V to 1.2 V appears a challenging specification for an inductive buck converter if the smallest footprint is targeted at +90 % efficiency.

Smallest footprint is approached through a 3D assembly of passive components to the active silicon die. High switching frequency is also considered to shrink the values of passive components as much as possible. From silicon integration point of view, it is well known that the proximity of decoupling capacitors to the power switches is mandatory for the sake of output voltage quality, efficiency, ElectroMagnetic Interference (EMI) and robustness.

In the context of on-chip power supply, the silicon technology is dictated by the payload, i.e. the digital functions. Complementary Metal-Oxide-Semiconductor (CMOS) bulk C40 is selected as a study case for 3.3 V input voltage. 3.3 V Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) features poor $Q_G \cdot R_{DS_{ON}}$ figure of merits and 1.2 V standard core, regular

devices are preferred. Moreover future integration as an on-chip power supply is more compatible. A three-MOSFET cascode arrangement is experimented and compared experimentally to a standard buck arrangement in the same technology. The coupled-phase architecture enables to reduce the switching frequency to half the operating frequency of the passive devices.

+100 MHz is selected for operation of passive devices. CMOS bulk C40 offers Metal-Oxide-Metal (MOM) and Metal-Oxide-Semiconductor (MOS) capacitors, in density too low to address the decoupling requirements. Capacitors have to be added externally to the silicon die but in a tight combination. Trench-cap technology is selected and capacitors are fabricated on a separate die that will act as an interposer to receive the silicon die as well as the inductors. The inductive devices must also be fabricated in an integrated manner to limit their footprint.

The work delivers an object containing a one-phase buck converter with the silicon die flip-chipped on a capacitor interposer where a tiny inductor die is reported. The one-phase demonstrator is suitable for coupled-phase demonstration. Standard and cascode configurations are experimentally compared at 100 MHz and 200 MHz switching frequency. The implementation of a three-MOSFET cascode power stage is the key innovation of this thesis.

The manuscript reviews the state-of-the-art of high switching frequency DC/DC converters, namely buck converter with a high level of integration. This review shows the interest for the approach considered throughout the work. A design methodology is presented to cover a system-to-device approach. The active silicon die is the central design part as the capacitive interposer is fabricated by IPDiA and inductors are provided by Tyndall National Institute. The assembly of the converter sub-parts is achieved using an industrial process. The manuscript details a large set of measurements to show the performances of the delivered DC/DC converters as well as its limitations. A 91.5 % peak efficiency at 100 MHz switching frequency has been demonstrated. The measurements results are advancing state-of-the-art as measured efficiency is comparable with the one of converters operating a decade below in terms of switching frequency.

Résumé

L'intégration ultime de convertisseurs à découpage repose sur deux axes de recherche. Le premier axe est le développement de convertisseurs à capacités commutées. Cette approche est compatible avec une intégration totale sur silicium, mais reste limitée en terme de densité de puissance si la charge requiert une importante puissance. Le second axe est l'utilisation de convertisseurs à inductances, qui pâtissent d'imposants composants passifs. Une augmentation de la fréquence de découpage permet de réduire les valeurs des composants passifs requis. Cependant une augmentation de la fréquence implique de fait une augmentation des pertes par commutation, ce qui est contrebalancé par l'utilisation d'une technologie de fabrication plus avancée. Ces technologies plus avancées souffrent quant à elles de limitations au niveau de leur tension d'utilisation.

Convertir une tension de 3,3 V vers une tension comprise entre 0,6 V et 1,2 V apparait donc comme un objectif ambitieux pour un convertisseur inductif, particulièrement dans le cas où les objectifs the taille minimale et de rendement supérieur à +90 % sont visés.

Un assemblage 3D des composants actifs et passifs permet de minimiser la surface effective du convertisseur. Un fonctionnement à haute fréquence est aussi considéré, ce qui permet de réduire autant que possible les valeurs requises pour les composants passifs. Au niveau de l'intégration silicium, il est nécessaire que les condensateurs de découplages soient physiquement proches

des interrupteurs afin de garantir à la fois une tension de sortie propre, un rendement suffisant, de faibles émissions électromagnétiques et une bonne fiabilité du système.

Dans le contexte de l'alimentation « on-chip », la technologie silicium est contrainte par la charge, c'est-à-dire les fonctions numériques. Un technologie 40 nm CMOS de type « bulk » est choisie comme cas d'étude pour une tension d'entrée de 3,3 V. Les transistors 3,3 V présentent une figure de mérite $QG_G \cdot R_{DS_{ON}}$ médiocre, les transistors 1,2 V sont donc sélectionnés. Ce choix permet en outre de présenter une meilleure compatibilité avec une future intégration sur puce. Une structure cascode utilisant trois transistors en série est étudiée et confrontée à une structure standard à travers des simulations et des mesures. De plus une architecture à inductances couplées est analysée car elle permet d'augmenter la fréquence apparente des composants passifs.

Une fréquence de travail de +100 MHz est choisie. La technologie 40 nm propose des capacités MOM et MOS qui affichent des densités trop faibles pour assurer un découplage suffisant. Une technologie de capacités en tranchées est sélectionnée, et fabriquée sur une puce séparée qui servira d'interposeur et recevra la puce active ainsi que les inductances. Les inductances doivent être elles aussi fabriquées de manière intégrée afin de limiter leur impact sur la surface du convertisseur.

Ce travail fournit un objet contenant un convertisseur de type Buck à une phase, avec la puce active retournée (technique « flip-chip ») sur l'interposeur capacitif, sur lequel une petite inductance également est rapportée. Le démonstrateur une phase est compatible pour une démonstration à phases couplées. Les configurations standard et cascode sont comparées expérimentalement aux fréquences de 100 MHz et 200 MHz.

Le présent manuscrit examine l'état de l'art des convertisseurs intégrés à haute fréquence de découpage. Cette revue met en évidence l'intérêt de l'approche suivie au cours de ce travail. Une méthodologie de conception est ensuite proposée, dans une approche « système vers composant ». La conception de la puce active est l'élément central de ce travail, l'interposeur capacitif étant fabriqué par IPDiA et les inductances par Tyndall National Institute. L'assemblage des différents sous-éléments est réalisé via des procédés industriels. Le manuscrit détaille un important ensemble de mesures, montrant les

performances du convertisseur DC-DC délivré, ainsi que ses limitations. Un rendement pic de 91,5 % à la fréquence de 100 MHz a été démontré.

Résumé étendu

Cette partie propose un résumé de synthèse en français du contenu du manuscrit.
This section offers an extended summary of the manuscript content in French.

Introduction générale

La fonction de conversion DC-DC est primordiale pour tout système embarqué électronique. Les convertisseurs DC-DC sont omniprésents à travers une large gamme d'applications, allant de l'électronique grand public à l'automobile. Ils sont nécessaires au fonctionnement des fonctions électroniques embarquées. Le rôle principal de ces convertisseurs est d'assurer une tension continue correcte à ces fonctions électroniques, sous des contraintes de variations de charge, de perturbations en entrée, d'efficacité énergétique, etc. Leur rôle est donc de gérer efficacement l'énergie électrique à disposition et la transmettre au bon moment et en bonne quantité à la charge considérée.

Les spécifications de ces convertisseurs sont majoritairement dépendantes de l'application visée. Il est cependant possible d'énoncer des exigences universelles liées à ces convertisseurs, résumées selon les points suivants : aucune place occupée, aucun coût, aucune défaillance et aucune perte. Ces grands axes mettent en avant les principaux compromis rencontrés lors de la conception des convertisseurs, qui sont la densité de puissance, le coût (surface et nombre de composants), la fiabilité et l'efficacité énergétique. La prépondérance d'un aspect par rapport à l'autre est dépendant de l'application. Par exemple, dans

l'électronique grand public, la fiabilité n'est pas un problème majeur, alors que le coût l'est. Dans les appareils portables (utilisant une batterie), un rendement élevé est l'objectif numéro un car il impacte à la fois la durée de la fonctionnement et la génération de chaleur. L'émergence des circuits intégrés de type « SoC (System-on-Chip) » implique une multiplication des domaines de tensions, et l'énergie distribuée se retrouve au sein d'un « nanogrid » sur puce. Les objectifs sont multiples : tout d'abord permettre aux différents blocs d'opérer indépendamment les uns des autres, et ensuite avoir des convertisseurs qui réagissent rapidement à des variations de charge, permettant ainsi d'adapter au plus juste la puissance fournie à la puissance requise, rendant l'ensemble du système plus efficace énergétiquement.

Ces considérations d'efficacité s'appliquent aussi pour des applications où la fiabilité est la préoccupation prioritaire, comme le secteur automobile. Les voitures d'aujourd'hui contiennent jusqu'à 70 unités de contrôle électroniques, qui utilisent des circuits intégrés tels que des microcontrôleurs. Ceux-ci sont actuellement alimentés via différents convertisseurs, qui occupent beaucoup de place au sein du système. L'objectif est de miniaturiser et d'intégrer ces convertisseurs directement à l'intérieur du microcontrôleur, permettant un gain significatif d'espace et d'énergie, réduisant ainsi les émissions de CO_2 du véhicule. Le travail présenté ci-après s'inscrit dans le cadre du projet PowerSWIPE[1] (EU FP7 318529), qui répond à ces enjeux en rassemblant les compétences et les technologies de laboratoires et d'industriels[2]. Le point central du travail présenté dans le manuscrit est celui du rendement énergétique à haute densité de puissance.

L'objectif principal est de valider une solution d'un convertisseur utilisant une intégration 3D fonctionnant à +100 MHz avec un rendement supérieur à 90 %.

Le chapitre 1 présente l'état de l'art des convertisseurs à haute fréquence de commutation et met en avant les compromis et défis rencontrés lors de la

[1] http://www.powerswipe.eu

[2] Tyndall National Institute (Cork, Irlande), Infineon Technologies AG (Regensburg, Allemagne), Infineon Technologies Austria AG (Villach, Autriche), IPDiA SA (Caen, France) Centro de Electroìnica Industrial, UPM, (Madrid, Espagne), Robert Bosch GmbH (Stuttgart, Allemagne), laboratoire Ampère, Université de Lyon (Lyon, France)

conception de ces convertisseurs. Une conclusion sur les principaux choix de conception est présentée.

Le chapitre 2 couvre la méthode de conception, partant du système jusqu'au composant. Le contrôle est abordé, mais n'est pas développé car ayant déjà été démontré dans la littérature. Le travail est donc restreint à une démonstration liée à la technologie et la conception. Un étage de puissance et la commande associée est considérée, sans les développements liés à la boucle fermée.

Le chapitre 3 est dédié à la conception du circuit intégré. Plusieurs prototypes ont été dimensionnés et conçus, puis fabriqués par les partenaires industriels du projet PowerSWIPE.

Le chapitre 4 rassemble les différents résultats de mesures effectués sur les prototypes fabriqués. Les performances et limitations de chaque convertisseur sont discutées. Les résultats présentés sont conformes aux attentes du projet concernant le convertisseur à haute fréquence de commutation.

Chapitre 1 : État de l'art

Dans ce chapitre sont abordés différents points. Tout d'abord, les choix à faire sont présentés, puis le principe d'opération des convertisseurs DC-DC est expliqué. S'en suit une analyse de performances, basée sur une étude approfondie de l'état de l'art, qui est logiquement conclue par des choix de conception en rapport avec les spécifications.

Questionnement préliminaire

Les considérations pré-conception débutent par une analyse système, en examinant deux architectures antagonistes : l'une utilisant des convertisseurs « off-chip » et l'autre utilisant des convertisseurs « on-chip ». La première architecture est celle classiquement utilisée, permettant une conception et un assemblage simples, mais étant limitée en termes de performances dynamiques et occupant beaucoup d'espace. La deuxième architecture est plus récente, et va de pair avec le développement croissant des « SoCs » complexes. Elle permet une alimentation au plus juste des fonctions intégrées, et les pertes sur pistes sont réduites au minimum. Cependant cette deuxième approche requiert

des composants passifs locaux, qui peuvent être coûteux selon la technologie utilisée.

Le choix des outils de conception (outils CAD) est primordial dans le cas de systèmes multi-domaines. Ici, la conception de circuits intégrés est mêlée à celle des composants passifs. Plusieurs approches peuvent être envisagées. Tout d'abord, l'utilisation d'un outil dédié pour chaque élément du système (SPICE pour les circuits intégrés, éléments finis pour les composants magnétiques, etc.), ce qui permet l'utilisation de modèles dédiés précis, au détriment de la modélisation des interactions. Il est aussi possible d'utiliser un outil générique (langage C ou Matlab par exemple) et d'y modéliser les différents composants ainsi que leurs interactions, mais impliquant de fait une restriction et des simplifications des modèles. La dernière stratégie est d'utiliser un outil dédié, et d'y modéliser les composants qu'il n'intègre pas, comme dans le cas de la modélisation d'inductances non-idéales dans un simulateur dédié aux circuits intégrés. Cette dernière approche permet de bénéficier de modèles précis pour une partie du système, ainsi que de modéliser une partie des interactions qui interviennent au sein de ce même système.

Avant la conception du convertisseur, il est intéressant d'analyser ce qui se fait au niveau de l'industrie. Plusieurs approches ont déjà été envisagées par des acteurs industriels majeurs. Intel à présenté en 2015 ses régulateurs intégrés (FIVR), utilisés pour alimenter leur dernière génération de processeur. D'un autre coté, Texas Instruments propose des convertisseurs DC-DC en boitier, intégrant des composants passifs SMD dans une approche 3D, référée comme un système PowerSiP. Enpirion Power Solutions (filiale d'Altera, elle-même filiale d'Intel) propose quant à elle l'intégration complète des composants passifs au sein d'un convertisseur, résultant un système de type PowerSoC.

Il existe deux grandes familles de convertisseurs : les convertisseurs à sorties isolées, et les convertisseurs non-isolés. Dans chacune de ces familles, on peut distinguer trois grands groupes : les convertisseurs dévolteurs (abaisseurs de tension), les convertisseur survolteurs (élévateurs de tension), et les convertisseurs mixtes, capables d'élever et d'abaisser la tension. Le choix de se positionner dans une de ces familles est guidé par les spécifications, notamment les contraintes de tensions d'entrée et de sortie.

Lorsqu'une structure de convertisseur est choisie, il convient de sélectionner sa fréquence de fonctionnement. Ce choix impacte notablement le fonctionnement du convertisseur, car il a tout d'abord des répercussions sur les composants passifs, mais aussi sur les pertes, ainsi que sur le fonctionnement en boucle fermée. La fréquence de commutation affecte aussi les émissions électromagnétiques du système, paramètre important pour des systèmes où la robustesse est un point clé.

Tout convertisseur génère intrinsèquement des pertes, qu'il convient de minimiser. Il existe plusieurs méthodes décrites dans la littérature permettant de minimiser ces pertes, et ainsi améliorer l'efficacité énergétique du système. Une méthode largement utilisée est celle d'optimiser le cycle de commutation des interrupteurs, en s'assurant que la puissance instantanée dans l'interrupteur est nulle lors de la commutation. Deux méthodes se distinguent : le ZVS (commutation à tension nulle) et le ZCS (commutation à courant nul). Ces deux méthodes peuvent recourir à des composants passifs supplémentaires, permettant de générer des résonances et donc des zéros de tension et de courant dans les interrupteurs. Il est aussi possible d'utiliser la résonnance au sein des circuits de pilotage des interrupteurs, limitant ainsi l'énergie requise pour ces circuits. D'autres techniques permettant d'augmenter le rendement existent, telles que la segmentation des interrupteurs de puissance, ou la segmentation du convertisseur en plusieurs phases, ainsi que l'utilisation des inductances couplées.

Principe d'opération d'un convertisseur

Le principe de fonctionnement d'un convertisseur dépend tout d'abord de sa structure. Ici l'accent est mis sur les convertisseurs abaisseurs non-isolés. Parmi ce groupe, trois grandes familles se distinguent : les convertisseurs à régulation linéaire, à capacités commutées et à inductances commutées. Les architectures classiques de chaque famille sont présentées, avec leurs principales caractéristiques.

Le régulateur linéaire se comporte comme un diviseur résistif. Une résistance variable en série avec la source de tension d'entrée permet d'ajuster la tension de sortie en fonction du courant. La régulation sur ce type de convertisseur peut être très rapide. Cependant, le rendement de ce type de convertisseur

dépend fortement du rapport de conversion, et peut donc être faible si la tension de sortie n'est pas proche de la tension d'entrée. Ils sont donc préférés pour réguler une tension proche de leur tension d'entrée.

Les convertisseurs à capacités commutées utilisent un ensemble de condensateurs et d'interrupteurs. Ils peuvent être modélisés par un diviseur de tension idéal, suivi d'un régulateur linéaire. Le rapport de conversion de ces convertisseurs dépend essentiellement de leur architecture, ainsi que de leur séquence de commutation. Ils présentent l'intérêt de ne pas utiliser d'inductances, ce qui facilite leur intégration sur silicium.

Les convertisseurs inductifs utilisent quant à eux une inductance comme élément de stockage d'énergie. Le filtre de sortie classique d'un convertisseur inductif est un circuit LC. L'inductance permet de lisser le courant, et le condensateur de lisser la tension. Le principe de fonctionnement de ces convertisseurs est de commuter à haute fréquence (vis-à-vis du filtre LC) la tension en entrée du filtre LC, qui effectue une moyenne de celle-ci en sortie.

Le convertisseur trois niveaux est à mi-chemin entre le convertisseur à capacités commutées et le convertisseur inductif. Ce convertisseur utilise un condensateur flottant qui permet de réduire l'amplitude de la tension appliquée en entrée du filtre LC, permettant ainsi un lissage plus efficace de la tension de sortie. La fréquence vue par les composants passifs est aussi plus élevée que la fréquence de commutation, accentuant encore l'effet mentionné précédemment.

Beaucoup d'autres structures de convertisseurs existent, mais ne sont pas présentées ici car elles ne sont pas l'objet du travail ci-après, et ont été analysées dans la littérature.

Analyse de performance

Dans cette section, les compromis de performance des convertisseurs DC-DC sont présentés. Une analyse système est d'abord présentée, basée sur des résultats publiés dans la littérature, puis l'analyse est poussée au niveau composant.

La méthode utilisée pour analyser les performances de l'état de l'art est présentée ci-après :

- Restriction de l'espace d'étude (faible tension ($\leq$5 V), faible puissance ($\leq$5 W), haute fréquence ($\geq$10 MHz)),

- Définition des métriques (fréquence, tension d'entrée et sortie, rendement, etc.),
- Récupération des données, basée sur des résultats de mesures publiés,
- Projection des données dans des plans de comparaison,
- Mise en avant des tendances et compromis.

La projection permet de mettre visuellement en avant les tendances majeures. De ces analyses, il ressort qu'il est nécessaire de prendre en compte le rapport de conversion avant de comparer les autres métriques. En effet, un convertisseur avec un petit rapport de conversion aura plus de difficultés à avoir un rendement plus élevé. La fréquence de commutation à un impact significatif sur le rendement de conversion, mettant en avant la difficulté d'atteindre les 90 % de rendement à haute fréquence. Le technologie de fabrication des composants actifs permet quant à elle d'améliorer le rendement (en utilisant une technologie plus avancée), mais présente des limitations au niveau de la tension d'utilisation.

Du coté composants, il y a trois catégories à distinguer : les inductances, les condensateurs et les interrupteurs. Pour chaque élément, les technologies disponibles sont présentées, avec leurs forces et faiblesses.

Les condensateurs sont des composants très courants en électronique. Ces condensateurs sont disponibles notamment en boitiers SMD, dans plusieurs variantes de taille. Ils présentent un bonne densité, mais souffrent d'une inductance parasite qui dépend principalement de la taille du boitier. Considérant un fonctionnement au delà de 100 MHz pour un condensateur d'une valeur aux alentours de 10 nF, une taille raisonnable de boitier est le 0402. Dans ce cas là, la fréquence de résonance du condensateur est aux alentours de 70 MHz, ne permettant pas un fonctionnement correct au-delà de 100 MHz. Ces composants ne sont donc pas appropriés pour la conception de convertisseurs haute fréquence.

Il existe des technologies de capacités intégrées qui sont les capacités MOS, MOM, MIM et en tranchées. La capacité MOS est l'utilisation de la grille de transistors comme capacités. Une capacité MOM quant à elle est la simple mise côte à côte de lignes de métal connectées à deux signaux différents. Ces

deux types de capacités sont présentes naturellement dans tout procédé de fabrication CMOS. Malheureusement, leur densité reste relativement faible, ne permettant pas de les utiliser pour des applications de découplage sans impacter la surface requise significativement. Le troisième type, la capacité MIM, est généralement une option de procédé CMOS, qui ajoute un niveau de métal intermédiaire, permettant de rapprocher les deux électrodes du condensateur, et donc d'augmenter la densité. Les capacités en tranchées requièrent elles aussi un procédé de fabrication spécifique, avec la nécessité de creuser des tranchées afin d'augmenter la surface effective du condensateur, et donc sa densité.

Concernant les inductances, elles existent tout comme les condensateurs en composants discrets en boitiers SMD. Ces inductances utilisent généralement des matériaux magnétiques pour augmenter leur valeur sans impacter leur volume. Cependant, les matériaux magnétiques présentent rapidement des limites lors de leur utilisation à haute fréquence.

Du coté des inductances intégrées, plusieurs structures existent, comme par exemple les structures solénoïdales, spirales (allongées ou non) ou encore en ligne. Lorsque ces inductances n'utilisent pas de matériau magnétique, elles présentent de bonnes performances à haute fréquence (coefficient de qualité élevé), mais de faibles performances du coté DC (résistance équivalente élevée). Du coté des inductances à matériau magnétique, l'utilisation de techniques comme la stratification permet d'améliorer les performances à haute fréquence tout en conservant celles à basse fréquence. Cependant peu d'inductances magnétiques ont été conçues pour un fonctionnement au-delà de 100 MHz.

Le choix d'interrupteur commence d'abord par un choix de matériau semiconducteur. Le plus classique est le silicium, cependant d'autres technologies existent, comme le GaN (nitrure de gallium), l'AsGa (arséniure de gallium) ou le SiC (carbure de silicium), et présentent à priori de meilleures figures de mérite que le silicium. Ces dernières technologies ne bénéficient cependant pas de la maturation qu'ont les technologies silicium, notamment au niveau de l'intégration de circuits digitaux. L'application visée étant l'alimentation « on-chip », le silicium sera donc la technologie de retenue.

Vient ensuite le choix du type de transistor. Le transistor bipolaire (BJT), le transistor à jonction (JFET) et le transistor à grille isolée (MOSFET) sont

des candidats potentiels. Seulement, toujours selon des considérations pratiques, uniquement le MOSFET est accessible dans les nœuds technologiques avancés et bénéficie des efforts d'optimisation de la technologie. Il sera donc le composant de choix pour la conception.

Conclusion et spécifications

Le système à concevoir est un convertisseur DC-DC au sein d'un système automobile. Il sera placé en aval d'un convertisseur prenant en charge directement la tension de la batterie du véhicule et délivrant 3,3 V. Cette tension est donc supposée suffisamment constante pour ne pas nécessiter une protection particulière contre les surtensions au niveau de l'entrée du convertisseur à concevoir. Ce dernier aura donc une tension d'entrée de 3,3 V, et devra délivrer une tension de 1,2 V, avec un courant nominal de 280 mA. La charge de ce convertisseur est un microcontrôleur, et peut être considéré comme une source de courant. La fréquence considérée est +100 MHz afin d'obtenir un convertisseur ne dépassant pas la surface de 10 mm^2, tous composants compris. Un faible profil est souhaité, autour de 1,2 mm.

Au niveau technologique, plusieurs technologies ont été choisies suite aux analyses précédemment présentées. Pour les composants actifs, une technologie CMOS de type « bulk » est sélectionnée. Cette technologie correspond à celle qui pourrait être classiquement utilisée pour réaliser un microcontrôleur. Cette technologie ne dispose pas de l'option capacité MIM, donc seules des capacités de type MOS et MOM seront disponibles. Leurs densités respectives n'étant pas assez élevées (environ 2 nF/mm^2), il est nécessaire d'utiliser une technologie tierce pour le découplage des tensions. La technologie retenue ici et celle de capacités en tranchées, présentant une bonne densité (autour de 200 nF/mm^2) et de bonnes performances à haute fréquence (inductance parasites de quelques pico-henrys). Du coté des inductances, une technologie d'inductance planaire est sélectionnée pour limiter l'impact de celles-ci sur le facteur de forme du convertisseur. Un procédé technologique permettant l'utilisation à haute fréquence est nécessaire, tout comme une faible résistance équivalente. Le choix s'est donc porté sur des inductances à matériau magnétique laminé. Une technologie d'assemblage 3D a été sélectionnée pour l'interconnexion des différents éléments.

Concernant les fournisseurs technologiques, ils sont divers, et principalement industriels. La technologie CMOS est fournie par Infineon et Global Foundries. Les capacités en tranchées seront fabriquées par IPDiA, qui réalisera aussi l'assemblage 3D. Les inductances seront fabriquées par Tyndall.

Chapitre 2 : Méthode de conception

Ce chapitre présente les analyses qui ont été menées en amont de la conception du convertisseur. Ceci inclut l'analyse haut-niveau de l'architecture, la modélisation des pertes des composants actifs et le dimensionnement du filtre de sortie. Des considérations sur les choix de contrôle sont aussi présentées.

Définition de l'architecture

Plusieurs architectures sont évaluées à travers des équations et des formes d'ondes analytiques dans un premier temps, puis ces résultats sont comparés à des simulations dans un but de validation. Les architectures considérées sont le convertisseur Buck une phase, deux phases et deux phases couplées, ainsi que le convertisseur trois niveaux. Ces convertisseurs sont comparés selon la méthode suivante : les formes d'ondes et équations sont développées en supposant des composants idéaux, puis les pertes sont calculées en ajoutant les composants parasites. Cette méthode est valide tant que les pertes restent limitées, c'est-à-dire tant que le rendement est peu affecté.

Les architectures sont évaluées dans des conditions similaires, qui sont : l'alimentation est en série avec une inductance parasite grande, rendant le courant de cette source constant (permettant donc d'évaluer les pertes du condensateur d'entrée) ; les condensateurs sont suffisamment grand pour ne pas voir leur tension varier lorsqu'ils fournissent (ou reçoivent) du courant ; les interrupteurs sont considérés idéaux ; aucun temps mort ; la charge est une source de courant. L'inductance parasite des condensateurs est omise pour développer les équations. Les équations en régime établi sont exprimées dans le cas de tensions d'entrée et de sortie constantes. Le rendement tend vers 100 %.

Les équations et formes d'ondes sont d'abord écrites pour le convertisseur une phase. L'ondulation en courant est calculée pour un fonctionnement en

conduction continue (CCM). Cette ondulation diminue avec la fréquence et la valeur d'inductance, mais augmente avec la tension d'entrée. Le courant efficace peut ensuite être calculé, car le courant à travers l'inductance suit une forme triangulaire. Le courant dans le condensateur de sortie est directement issu de la composante alternative du courant dans l'inductance. Pour le courant dans le condensateur d'entrée, le calcul est réalisé en distinguant deux phases de fonctionnement. En se basant sur les valeurs de courants, les pertes sont ensuite calculées. Ces pertes dépendent de deux valeurs : le courant de charge et l'ondulation en courant. L'ondulation en courant dépendant elle-même de la fréquence et de l'inductance, les valeurs de pertes peuvent donc être optimisées sur ce point.

Le convertisseur deux phases peut être vu comme deux convertisseurs une phase partageant les mêmes condensateurs d'entrée et de sortie. Le déphasage entre les phases est de 180°. Le courant dans l'inductance est donc calculé de façon similaire. Le courant dans le condensateur de sortie est la somme des valeurs AC du courant de chaque phase. Grâce au déphasage entre ces courants, la résultante est dans tous les cas plus faible que dans le cas d'un convertisseur une phase. Pour le condensateur d'entrée, une décomposition en quatre morceaux est nécessaire pour le calcul. Cependant, en raison du déphasage, les deux premiers morceaux sont identiques au troisième et quatrième. Similairement au convertisseur une phase, les pertes sont calculées. En comparant ces deux architectures, il ressort que la topologie deux phases a des pertes toujours plus faibles que celle à une phase (en CCM).

Le convertisseur deux phases couplées est identique au convertisseur deux phases, à la différence des inductances qui sont couplées. Pour calculer le courant dans les inductances, il convient de poser un système d'équations prenant en compte le coefficient de couplage. Ce système est ensuite résolu pour chaque phase de fonctionnement, c'est-à-dire en quatre morceaux. Cette résolution de quatre systèmes peut être réduite à deux en prenant en compte le déphasage et la similitude des phases. De la résolution de ce système, les valeurs de courant remarquables sont exprimées, et il est aussi possible d'en déduire un coefficient de couplage optimum, c'est-à-dire celui qui minimise l'ondulation en courant. Cette valeur optimale ne dépend que du rapport cyclique. Le calcul du courant efficace peut ensuite se faire en utilisant les valeurs remarquables des courants.

Le courant dans le condensateur de sortie est comme précédemment la somme des courants AC de chaque phase, le calcul étant ici un peu plus complexe car les formes d'onde des courants par phase ne sont plus triangulaires. Le courant dans le condensateur d'entrée est évalué de la même manière que pour un convertisseur deux phases. Les pertes sont ensuite calculées, montrant que dans le cas d'un coefficient de couplage optimum, les pertes sont toujours plus faibles lorsque les inductances sont couplées.

Le convertisseur trois niveaux est ensuite évalué de la même manière. L'ondulation en courant dans l'inductance est plus faible que celle d'un convertisseur de type Buck à une phase. Un composant est ajouté au système (comparé aux structures précédentes) qui est une capacité flottante. Les équations montrent que l'intérêt de cette structure est fortement dépendant de ce composant, qui permet de réduire l'ondulation en courant, mais qui est aussi une source de pertes.

Afin de comparer toutes ces architectures entre elles, des conditions d'évaluation ont été définies (fréquence, tension, courant, valeurs des composants parasites), et les pertes ont été calculées numériquement. Ces résultats ont été comparés à des simulations, justifiant la pertinence de l'utilisation de ces équations. La comparaison des pertes met clairement en défaut le convertisseur trois niveaux. Ceci est dû au condensateur flottant, générant une partie non négligeable des pertes du convertisseur. Le meilleur semble être le convertisseur à deux phases à inductance couplées, qui cependant ne démontre pas un gain significatif vis-à-vis du convertisseur deux phases non couplées.

Le convertisseur à deux phases couplées est tout de même étudié plus en profondeur, notamment l'impact du coefficient de couplage sur l'ondulation en courant. Cette étude est nécessaire car l'évaluation précédente supposait un coefficient optimum à tout point de l'évaluation (donc variable), ce qui n'est pas raisonnablement envisageable. La première étape est d'observer l'évolution du coefficient de couplage optimal avec le rapport cyclique. Cette valeur tend vers -1 quand le rapport cyclique tend vers 0,5. Un autre analyse est nécessaire, celle de l'évolution de l'ondulation en courant en fonction de coefficient de couplage pour différents rapports cycliques. Cette étude montre que pour un rapport cyclique différent de 0,5, lorsque le coefficient de couplage tend vers -1, l'ondulation en courant tend vers des valeurs très grandes (et

très largement supérieures au cas d'un couplage nul). Ceci montre qu'il faut choisir le coefficient de couplage en prenant en compte toutes les possibilités de rapports cycliques pour éviter des instabilités. Une valeur aux alentours de $-0{,}35$ semble être un bon compromis pour une large gamme de rapports cycliques.

La diminution de l'ondulation en courant entraine une diminution du courant efficace, donc des pertes. Cependant, comme l'ondulation ne contribue pas significativement au courant efficace, ce gain est discutable. Les stratégies possible pour effectivement bénéficier d'un gain sont les suivantes : soit réduire les valeurs d'inductances, réduisant ainsi le pertes DC dans un budget d'ondulation en courant constant ; soit réduire la fréquence, réduisant ainsi les pertes par commutations (détaillées par la suite) sans augmenter l'ondulation en courant. Cette approche sera celle retenue.

Stratégies de contrôle

Plusieurs stratégies de contrôle peuvent être appliquées à un convertisseur à découpage. Cet aspect a déjà été étudié et est relativement bien documenté. On peut distinguer trois grandes familles de contrôles : les contrôles de type linéaires, ceux de types non-linéaires et les contrôles hybrides.

Le contrôle de type linéaire peut se faire sur deux grandeurs : la tension ou le courant de sortie. Le contrôle en tension requiert de mesurer la tension de sortie et d'utiliser un amplificateur d'erreur pour comparer cette tension à celle de la référence. La tension d'erreur sert quant à elle à générer le signal de modulation. Un filtre linéaire pour l'amplification d'erreur est requis. Il est généralement construit autour d'un amplificateur opérationnel, de résistances et de capacités permettant le placement de pôles et de zéros. Ce mode de contrôle résulte généralement en un système globalement stable, mais souffre cependant d'approximations, la première étant la non-linéarité intrinsèque du découpage. La stabilité n'est assurée que si la bande passante est largement inférieure à la fréquence de commutation (10 fois plus faible par exemple). De plus, les critères de stabilités sont valides pour le régime établi. Des instabilités à grande échelle peuvent apparaitre dans des conditions transitoires, comme par exemple le phénomène dit de doublage de la période.

Le contrôle linéaire en courant propose différentes approches. La régulation peut se faire sur le pic de courant positif, le pic négatif, ou encore le courant moyen. De manière générale, comme le courant est régulé, le filtre LC de sortie peut être considéré comme une source de courant contrôlée en tension. Le filtre se transforme donc en système du premier ordre à un pôle, plus simple à stabiliser. La régulation en courant rend le convertisseur moins sensible aux perturbations d'entrée. Ce type de contrôle rejette par ailleurs la fréquence de résonance du filtre LC, qui limite les performances en régulation de tension. Une boucle de contrôle en courant bien conçue pourra donc afficher de meilleures performances qu'une boucle de régulation en tension, ainsi qu'une plus faible impédance équivalente de sortie. Le problème central de ce type de régulation est la mesure du courant. Ce problème devient majeur dans le cas d'une importante fréquence de commutation. En effet, un capteur de courant à forte bande passante et faible bruit est difficile à concevoir.

Le pendant de la régulation linéaire est la régulation non-linéaire. Un exemple classique de ce type de régulation est celui basé sur l'ondulation de la tension en sortie. La tension de sortie est directement comparée à une tension de référence via un comparateur hystérétique, assurant ainsi de conserver la tension de sortie dans une fenêtre bien définie. Cependant, cette technique requiert une ondulation en sortie suffisamment élevée pour pouvoir être correctement comparée. Dans le cas de condensateurs de sortie à faible résistance parasite, ce mode de contrôle est vite limité.

Une autre stratégie est de réguler le courant dans une boucle non-linéaire. Un filtre de reconstruction du courant peut être utilisé pour émuler le courant à travers l'inductance (circuit RC permettant d'intégrer la tension), et ce signal est ensuite ajouté à celui de la tension de sortie, pour enfin être comparé à une référence et générer les signaux de commande. Cependant, ce type de convertisseur présente de façon inhérente une ondulation en sortie (ondulation nécessaire pour fonctionner) qui tend vers une valeur nulle lorsque la fréquence augmente. Une fréquence de commutation infinie serait nécessaire pour minimiser l'erreur de tension en sortie. Ce n'est pas pratiquement faisable à cause des délais de propagation et de commutation. De plus, une fréquence trop élevée (ou imprévisible) n'est pas souhaitable, ne serait-ce que pour limiter les pertes en commutation.

Il est possible de mixer la régulation linéaire et non-linéaire au sein d'un même contrôleur. L'idée est d'avoir deux boucles de régulation, une non-linéaire, rapide mais peu précise, et une linéaire, lente mais précise. Sous ce principe trois contrôleurs peuvent être déclinés, basés sur l'endroit de mesure du signal rapide. Ces contrôleurs sont le V^2, le quasi-V^2 and le V^2I_C. Le premier (V^2) ne mesure que la tension de sortie, qui sert de signal d'entrée à la boucle lente et à la boucle rapide. La limitation de ce contrôleur est qu'il fonctionne mal lorsque l'ondulation en sortie est faible. Pour adresser ce problème, la régulation quasi-V^2 utilise le courant dans l'inductance comme signal rapide. L'information rapide peut aussi être mesurée dans la capacité (son courant étant équivalent à celui de l'inductance), on parlera alors de contrôle V^2I_C. D'un point de vue contrôle, ces convertisseurs utilisent à la fois le signal de sortie et sa dérivée pour réguler le convertisseur.

Dans le cas de nos spécifications, la haute fréquence exclut dans un premier temps l'utilisation du courant comme grandeur de régulation. De plus, l'ondulation en sortie doit être faible, les régulations de type non-linéaire sont donc elles aussi mises de côtés. La régulation en tension semble répondre convenablement aux objectifs, d'autant plus que la haute fréquence permet de compenser les limites en bande passante de ce type de régulation.

Modélisation des interrupteurs

L'objectif de cette partie est de définir un modèle d'interrupteur simple permettant d'évaluer la technologie CMOS sélectionnée. Ce modèle permettra aussi d'effectuer un pré-dimensionnement des interrupteurs et d'estimer leurs pertes en conduction et commutation.

Le modèle choisi se base sur un circuit équivalent du transistor utilisant des résistances et capacités. Un MOSFET peut être modélisé par un composant à quatre terminaux, qui sont le drain, la grille, la source et le corps. Une résistance modulable est présente entre le drain et la source (R_{DS}), le transistor étant considéré uniquement dans son régime linéaire. La modulation s'effectue par la tension entre la grille et le corps. Quatre capacité sont définies : la capacité drain-source (C_{DS}), la capacité grille-source (C_{GS}), la capacité grille-drain (C_{GD}) et la capacité grille-corps (C_{GB}). Le corps étant

connecté électriquement à la source, le modèle se simplifie donc à trois terminaux et trois capacités (les capacités grille-source et grille-corps étant en parallèle). Bien que ce modèle soit déjà fortement simplifié, un modèle plus condensé serait souhaitable. La capacité grille-drain est donc ramenée à la source (on se retrouve avec une capacité C_G), supprimant un paramètre du modèle, et permettant de modéliser les pertes en entrée indépendamment des conditions de sortie de l'interrupteur.

Les pertes de ce modèle sont donc directement des pertes de charge et décharge de condensateur à l'entrée, des pertes par effet Joule dans la résistance et des pertes de charge et décharge de condensateur dans la capacité de sortie. Les équations des pertes peuvent donc être développées de façon relativement simple en fonction de la tension de commande, de la tension d'entrée, du courant efficace et de la fréquence.

L'étape suivante est donc d'extraire les valeurs des paramètres du modèle, basé sur la technologie sélectionnée. De plus, la technologie 40 nm comprend plusieurs types de transistors, qu'il convient d'évaluer et comparer afin de choisir le plus approprié. Pour chaque type de transistor, la résistance drain-source, la capacité drain-source et la capacité grille-source ont été mesurées pour différentes valeurs de tension de commande. Les capacités sont évaluées via des simulations transitoires, par intégration du courant, et la résistance drain-source est évaluée via une simulation DC. Ces simulations sont rapides et permettent de caractériser l'ensemble des composants disponibles en quelques secondes.

Les transistors peuvent ensuite être comparés entre eux. Trois types de transistors ont été caractérisés : les transistors 5 V, 3,3 V et 1,2 V. les différences majeures sont leur longueur minimale de canal et l'épaisseur de l'oxyde de grille. Les transistors 1,2 V ne peuvent clairement pas répondre aux spécifications (tension d'entrée de 3,3 V), mais sont tout de même analysés comme point de référence de la technologie. Les valeurs des paramètres sont extraits par µm de largeur de canal. Les résistances sont donc en kΩ µm et les capacités en fF/µm.

En traçant l'évolution des paramètres (C_G, C_{DS} et R_{DS}) avec la tension de grille, plusieurs remarques peuvent être faites. Tout d'abord, plus le transistor peut fonctionner à tension élevée, plus sa capacité de grille augmente.

Cette capacité est aussi relativement similaire quelque soit le type de transistor considéré (type P ou type N). La capacité drain-source est quant à elle plus faible que la capacité grille, et ne présente pas de variation liée à la tenue en tension, mais uniquement liée au type (P ou N) de transistor. La résistance varie quant à elle assez logiquement, étant plus élevée pour les transistors haute tension que pour les transistors faible tension. À chaque fois le transistor de type P est environ trois fois plus résistif que celui de type N, à cause de la différence de mobilité des électrons par rapport aux trous.

Basé sur les paramètres de la technologie, il est en outre possible d'évaluer la taille optimale de transistor, celle permettant de minimiser les pertes. De cette évaluation il ressort que la taille optimale peut être exprimée simplement basée sur la résistance et la capacité de grille (paramètres technologiques) ainsi que le courant efficace et la fréquence de commutation (spécifications).

L'analyse des données dans le plan (R_{DS}, Q_G) permet d'évaluer directement la performance du transistor, en négligeant cependant la capacité drain-source. Ceci est acceptable dans le sens ou la valeur de cette capacité varie peu pour tous les transistors considérés. L'analyse des données dans ce plan montre clairement que le transistor 1,2 V présente les meilleures performances. Cependant, il ne permet pas de supporter la tension d'entrée requise. Un transistor hypothétique construit avec trois transistors 1,2 V en série est ajouté au plan. Ses paramètres sont calculés à partir du transistor 1,2 V, avec une résistance multipliée par trois et une capacité d'entrée multipliée par trois aussi. Ce transistor hypothétique présente de meilleures performances que le transistor 3,3 V, il parait donc intéressant d'exploiter cet aspect.

Un étage de puissance de type cascode utilisant trois transistors en série est donc envisagé. Cette structure est détaillée dans le chapitre suivant.

Suivant les formules développées pour évaluer la technologie, il est possible de calculer les pertes est d'estimer le rendement de l'étage de puissance. Ceci a été fait dans le cas des spécifications de conception et de la technologie sélectionnée. L'ondulation en courant dans l'inductance est négligée car c'est un faible contributeur au courant efficace. L'évaluation des pertes permet d'affirmer d'ores et déjà que l'objectif d'un rendement de 90 % sera difficile, le budget de pertes étant totalement utilisé par les composants actifs.

Filtre de sortie et capacités de découplage

Concernant les composants passifs, ils ont de la même manière été modélisés, puis ce modèle a été utilisé pour les dimensionner. Ces composants comprennent les condensateurs en les inductances.

La technologie de condensateurs utilisée est celle d'IPDiA dénommée 3D-PICS. Les condensateurs sont des capacités de type tranchée sur silicium. Ce condensateur peut être modélisé par un circuit équivalent. Il comprend trois terminaux, deux pour l'accès à la capacité, et un troisième pour le contact du silicium (corps). Une jonction parasite est présente entre un terminal du condensateur et celui du corps. De plus, des capacités parasites présentes entre chaque terminal d'accès et le corps sont présentes. Une résistance en parallèle de la structure est utilisée pour modéliser les courants de fuite. Une résistance série est aussi présente. Des inductances d'accès sont aussi présentes à chaque terminal d'accès.

La diode parasite et les capacités terminal-corps sont importantes à considérer dans une application nécessitant des condensateurs flottants. De le cas présent (découplage de tension continue par rapport à la masse), le corps est directement connecté à un terminal d'accès du condensateur, neutralisant la jonction parasite. Le modèle peut donc être simplifié à un modèle RLC classique, la résistance modélisant les courants de fuites étant suffisamment élevée pour ne pas avoir d'impact sur le fonctionnement du condensateur.

La modélisation d'inductance à matériau magnétique est assez bien étudiée. Plusieurs modèles prenant en compte des effets comme la température ont été développés. À haute fréquence cependant ces modélisations sont très rapidement limitées. La structure considérée ici est une inductance de type spirale allongée (ou « racetrack ») à corps magnétique. Un problème des matériaux magnétiques à haute fréquence est leur effet de peau. Un moyen de limiter ce problème est l'utilisation d'un matériau magnétique laminé, rendant le procédé de fabrication plus complexe et coûteux.

La modélisation de ces inductances à haute fréquence est très complexe et n'est pas le but premier de ce travail. Le courant à travers l'inductance est principalement continu, donc un modèle simple d'inductance a été utilisé pour le dimensionnement. Ce modèle est un simple circuit RL série. La résistance parasite est supposée proportionnelle à la valeur de l'inductance.

Cette résistance combine à la fois l'effet résistif dû a la trace de cuivre, et les effets du matériau magnétique transposés en résistance équivalente. Pour les inductances couplées, un coefficient de couplage est introduit.

Le filtre de sortie est dimensionné par la suite, en utilisant les modèles présentés précédemment. Cependant, en raison de l'absence de spécifications précises de fonctionnement transitoire, et de la limitation à la boucle ouverte pour des raisons pratiques d'accès au silicium, le dimensionnement est partiel, basé sur des considérations en régime établi.

Dans le cas d'un convertisseur à une phase, le filtre comprend uniquement une inductance et un condensateur. En régime établi, l'ondulation est un paramètre important. Sa valeur fixe la limite entre le fonctionnement CCM et DCM. L'objectif est de fonctionner le plus souvent possible en CCM donc de limiter au maximum cette ondulation en courant. Le courant de charge minimal étant 50 mA, l'ondulation maximum associée est donc de 100 mA Ceci résulte en une inductance minimale de 40 nH à 200 MHz.

Cependant une inductance trop élevée présente des inconvénients. Étant donné que la résistance série de l'inductance est proportionnelle à sa valeur, une trop forte valeur rendrait l'inductance trop résistive. La valeur donnée par le fabricant et de 5 mΩ/nH. Sur ces considérations, la valeur d'inductance est donc réduite à 30 nH. Le rendement à faible courant a été sacrifié pour maximiser le rendement à plus fort courant.

Au sujet du condensateur de sortie, une valeur de 15 nF a été choisie. Cette valeur permet d'atteindre les performances de précision requises (ondulation en régime établi). Au niveau du comportement fréquentiel, ce condensateur doit pouvoir fonctionner à une fréquence de 200 MHz. Sa fréquence de résonnance doit donc être supérieure à 200 MHz, donc une inductance parasite inférieure à 40 pH. Au niveau de la résistance parasite, elle doit être minimisée au maximum, à la fois pour limiter l'ondulation en tension et pour limiter les pertes. Cependant, la contrainte au niveau de la fréquence prévaut car elle conditionne le fonctionnement correct du convertisseur.

Les valeurs de composants passifs choisies ont été validées via des simulations SPICE. Les formes d'ondes montrent un fonctionnement correct du système.

Le filtre de sortie pour le convertisseur à inductances couplées requiert

une attention plus spécifique. La sensibilité de l'ondulation en courant au coefficient de couplage et au rapport cyclique est problématique. Une structure générique d'inductances couplées avec une inductance de sortie a été utilisée pour optimiser ce filtre. Trois cas ont été distingués : coefficient de couplage nul (équivalent à deux phases classiques), pas d'inductance de sortie (équivalent à un couplage classique) et des inductances couplées avec un inductance de sortie. Le premier cas sert de référence, permettant de quantifier le gain de chaque autre cas. L'optimisation a montré que l'inductance de sortie aide à s'affranchir de la sensibilité du coefficient de couplage vis-à-vis du rapport cyclique. De plus les performances sont meilleures que de simples inductances couplées. Cette structure de filtre de sortie est donc privilégiée.

Concernant les condensateurs de découplage de la tension d'entrée, leur contrainte est de pouvoir fournir des pics de courants significatifs sans pour autant devenir instable et voir leur tension varier significativement. Ces condensateurs doivent donc avoir une inductance parasite très faible, et une valeur de capacité suffisante pour garder une tension constante. Une valeur trop élevée n'est pas non plus souhaitée car ceci réduirait leur fréquence de résonance, limitant ainsi leur performance à haute fréquence.

Conclusion et objectifs de conception

Plusieurs architectures ont été évaluées et comparées via des équations analytiques. Le convertisseur de type Buck à deux phases couplées semble être un bon candidat en respect des spécifications. La technologie des composants actifs a été évaluée, démontrant la supériorité des composants faible tension. Concernant les composants passifs, les filtres de sortie ont été dimensionnés, tout comme les condensateurs de découplage.

Au niveau des composants actifs, la conception devra valider plusieurs hypothèses. Tout d'abord les modèles utilisés devront être confrontés aux modèles SPICE puis aux résultats de mesure. De plus, la structure d'étage de puissance cascode doit être validée expérimentalement, aucune publication à ce jour ne présentant de tels résultats. Enfin, une comparaison du fonctionnement à 100 MHz et 200 MHz est nécessaire.

Quatre circuits seront donc conçus :

- Étage de puissance standard avec des transistors 3,3 V, fréquence de 200 MHz, 280 mA de courant de charge
- Étage de puissance standard avec des transistors 3,3 V, fréquence de 100 MHz, 140 mA de courant de charge
- Étage de puissance cascode avec des transistors 1,2 V, fréquence de 200 MHz, 280 mA de courant de charge
- Étage de puissance cascode avec des transistors 1,2 V, fréquence de 100 MHz, 140 mA de courant de charge

Du côté des composants passifs, plusieurs éléments seront conçus. Un interposeur capacitif, comprenant quatre condensateurs, un motif permettant de recevoir le circuit intégré et une empreinte pour la connexion d'une inductance commerciale. Des inductances planaires seront aussi conçues pour valider l'intérêt des inductances couplées. Deux structures d'inductances couplées seront conçues afin de valider l'intérêt d'une inductance de sortie sur le filtre LC.

Ces éléments seront conçus en parallèle, et testés indépendamment les uns des autres dans le but de valider chaque étape technologique, puis assemblés et caractérisés au niveau système.

Chapitre 3 : Conception des circuits intégrés

Ce chapitre couvre l'ensemble de la conception des circuits intégrés. Ceci est un point majeur du travail effectué, et reprend l'aspect circuit ainsi que les considération de dessin des masques. L'approche proposée ici est de type « top-down », c'est à dire que la conception est présentée en partant du système et en allant vers le composant. Suivant les considérations d'optimisation circuit et de dessin des masques, quelques remarques de conception liées au placement sur la puce sont présentées.

Vue système globale

Le système considéré est donc un convertisseur DC-DC non-isolé de type Buck. Il peut être découpé en 4 sous-systèmes : le « level-shifter », les drivers, l'étage de puissance et le filtre de sortie. Comme différents convertisseurs sont conçus

(différentes structures d'étage de puissance, différentes fréquences et courants), certains éléments seront différents, d'autres identiques pour tous les convertisseurs. Le filtre de sortie étant réalisé par les composants passifs, sa conception n'est pas détaillée ici.

Détails de conception

Deux étages de puissance sont considérés : un standard (avec des transistors 3,3 V) et un cascode (avec des transistors 1,2 V en série). Ces deux étages de puissance ont été optimisés avec les mêmes outils, dans les mêmes conditions. Une structure de driver idéal a été utilisée pour commander et optimiser les étages de puissance considérés. Ce driver idéal permet notamment de mesurer les pertes liées à la commande de l'étage de puissance (charge de grille). Il émule aussi la transconductance et la saturation qu'a un réel inverseur.

Le premier étage de puissance considéré est le standard. Il est constitué d'un P-MOSFET pour l'interrupteur connecté à l'alimentation, et d'un N-MOSFET pour l'interrupteur connecté à la masse. L'optimisation consiste au choix de la taille optimale des transistors, leur tension de commande, ainsi que du réglage des délais optimaux des signaux de commande. Cette optimisation est menée au sein de l'outil *Global Optimization* dans l'environnement de conception Cadence. La procédure d'optimisation a été lancée plusieurs fois (avec différents points de départ) afin de vérifier la stabilité des résultats. Le circuit a été optimisé pour 100 MHz et 200 MHz, ainsi que pour 70 mA, 140 mA et 280 mA (soit au total 6 points d'optimisation). La taille optimale des transistors varie quasi linéairement avec le courant de charge. La tension de commande optimale est aux alentours de 2 V. Les tailles de transistors choisis pour la conception sont ensuite arrondies (dans un souci de simplifier l'implémentation). L'impact de cette approximation sur les pertes n'est pas significatif.

L'étage de puissance cascode est optimisé selon la même méthode, avec les mêmes outils et dans les mêmes conditions. Cet étage de puissance compte cependant plus d'éléments, rendant l'optimisation plus coûteuse (temps de calcul), et légèrement plus variable. Des tendances globales peuvent quand même être dégagées, comme par exemple un impact relativement insignifiant de la

taille des transistors présents à l'intérieur de l'étage de puissance. Les résultats d'optimisation sont donc récupérés et les valeurs de conception choisies en conséquence. Ces valeurs sont arrondies pour simplifier la conception.

Afin de commander correctement les étages de puissance, il est nécessaire de concevoir des circuits de commande (driver) qui fourniront le courant nécessaire pour commander l'étage de puissance, et qui prendront en charge les délais requis pour la commande. Afin d'assurer des délais corrects, plusieurs cellules « standards » on été conçues. Ces cellules permettent de retarder soit le front montant, soit le front descendant d'un signal de 100 ps. Une troisième cellule ne générant aucun délai est aussi utilisée, permettant de compenser lorsque c'est nécessaire la propagation des signaux à travers les deux circuits précédents. Ces cellules sont ensuite utilisées pour générer des délais multiples de 100 ps. Une cellule d'entrée est utilisée pour les circuits de commande, permettant de rendre l'entrée des circuits de commande relativement figée en terme d'impédance.

Une cellule clé pour le bon fonctionnement du circuit est le « level-shifter ». Cette cellule assure la génération de signaux de commandes synchronisés avec des niveaux de tension corrects. Deux structures de level-shifter ont été comparées. Une structure à verrouillage (de type « latch »), et une structure basée sur un comparateur. La deuxième structure permet d'assurer un circuit plus rapide et une meilleure synchronisation des signaux de sortie, c'est donc celle qui est retenue. Deux level-shifter différents ont été conçus : un pour l'étage de puissance standard (avec deux sorties) et un pour l'étage de puissance cascode (avec trois sorties).

Le level-shifter requiert une source de courant pour fonctionner correctement. Cette source doit être relativement précise et doit pouvoir démarrer sans l'aide de circuits extérieurs. La structure choisie et conçue permet de générer une référence de 44 µA en ne nécessitant que 420 nA pour sa polarisation. La stabilité en température et la robustesse vis-à-vis de la tension de sortie a été évaluée en simulation.

Considérations de dessin des masques

Concernant la phase d'implémentation, plusieurs contraintes et spécificités du circuit sont à prendre en compte. Ces considérations sont présentées ici

par thématique, et ont été appliquées tout au long de la phase de dessin des masques.

Tout d'abord, il convient de présenter chaque composant utilisé (transistor) et expliquer comment chaque structure (type P, type N, type N isolé) se présente. Ces structures étant implémentées sur un substrat commun de type P, il faut en outre modéliser les interactions entre chaque composant et le substrat. Chaque transistor existe en version 1,2 V et 3,3 V, la différence étant l'épaisseur d'oxyde et la longueur minimale de grille.

Chaque composant étant couplé avec le substrat, il est nécessaire de réduire au maximum le bruit généré lors de la commutation de chaque élément. L'utilisation d'anneaux de garde autour de chaque composant permet de drainer au plus vite les courants parasites pouvant transiter par le substrat. Ces anneaux de gardes doivent être réalisés en respectant des contraintes de tailles. Dans certains cas, un anneau double est nécessaire, afin d'isoler efficacement le composant du reste du circuit.

Les structures de transistor présentées sont agencées en doigts parallèles dans le cas de transistors larges (ce qui est le cas pour les transistors de puissance). Une structure inter-digitée a pour conséquence un transistor ayant deux fois plus de doigts de grilles que de doigts de drain ou source. Ceci impacte la taille du composant, mais aussi la résistance liée au métal.

La technologie considérée comporte huit niveaux de métal, chaque niveau ayant sa propre résistance (liée à son épaisseur/largeur). Cette résistance est caractérisée latéralement dans le manuel de conception, mais aucune info n'est présente sur la résistance verticale de cet empilement, ce qui ne facilite pas la conception. À la résistance des couches de métal s'ajoute celle des vias. En raison de leur forte résistance et des limites en termes de densité, leur résistance n'est pas négligeable non-plus.

Les capacités parasites entre deux éléments de routage peuvent être estimées a priori avec des formules données. Ces capacités sont critiques pour des points comme le nœud V_{LX}, qui commute à haute fréquence et à pleine tension. Le routage côte à côte est donc à inspecter prudemment afin de ne pas créer des capacités parasites trop importantes.

Il est proposé d'élargir les contacts de drain et de source des transistors afin de limiter l'impact du métal sur la résistance de l'interrupteur. Ceci permet de

multiplier par plus de 2 les contacts sur le drain et la source des composants, et autorise l'utilisation de lignes de métal plus larges, donc moins résistives, sans augmenter les capacités parasites.

L'empilement alterné des vias permet aussi une meilleure répartition du courant, et donc une plus faible résistance équivalente lorsque qu'il s'agit de remonter (ou descendre) l'empilement des couches métalliques. Ceci a été évalué avec de simples formules analytiques, et implémenté lors du dessin des masques.

L'alternance des vias permet aussi de diminuer les capacités parasites lorsqu'il s'agit de fils différents mis côte à côte. De plus, le nombre global de vias étant inchangé, la résistance n'est pas impacté. Les capacités parasites sont aussi limitées en préférant l'utilisation de peu de larges lignes de métal au lieu de beaucoup de lignes de métal plus fines. Le compromis dans ce cas est d'éviter d'avoir un chemin trop long pour accéder à n'importe quel point du transistor, sans multiplier les doigts fins.

Lors de tout dessin de masque qui requiert de la précision, la notion de « matching » est incontournable. Des techniques de matching classiques ont été utilisées ici dans le cas du dessin des drivers, du level-shifter et de la source de courant. La première est l'utilisation de structures dites factices (dummy). Ces structures assurent un environnement homogène pour le composant considéré. La deuxième technique est celle du barycentre commun (dite « common-centroid »). Dans ce cas là, les composants sont éclatés en plusieurs morceaux élémentaires identiques, puis répartis de façon homogène, tous les composants ayant le même barycentre. Ceux deux techniques ont permis d'avoir une conception plus robuste aux variations de procédé de fabrication.

Masques des circuits

Cette partie présente les dessins des masques de chaque cellule conçue. L'ordre de présentation suit la propagation des signaux au sein des convertisseurs : de l'entrée d'horloge à la sortie de puissance. Les images sont détaillées à partir de la page 134 dans le chapitre 3.

Considérations au niveau puce

Le convertisseur étant dessiné, il est nécessaire de prendre des précautions lors du placement de ce convertisseur sur la puce elle-même. Ces précautions sont liées au placement lui-même, devant être compatible avec la position des entrées/sorties, contraintes par l'interposeur. Des condensateurs ont été embarqués sur la puce dans l'espace non-utilisé, il convient donc de les répartir judicieusement pour un fonctionnement optimal. Finalement, le routage du plus haut niveau de métal doit lui aussi être judicieux pour limiter la résistance ajoutée, ainsi que les couplages non-souhaités.

Dans un souci d'économie de silicium et de maximisation des tests possibles, deux convertisseurs sont embarqués par puce. Cependant, lors de l'assemblage, un seulement sera actif, l'autre étant non-connecté. Il faut donc avoir un placement avec une symétrie centrale, permettant de choisir quel convertisseur connecter au moment de l'assemblage sans devoir changer d'interposeur. Le placement sur la puce doit aussi minimiser les résistances parasites. Le convertisseur est donc placé au plus près des connexions de la tension d'entrée et de la masse. Ceci permet aussi de limiter les inductances parasites, et donc ne pas dégrader les performances en commutation. Le placement des convertisseurs standards et cascodes est similaire, car ces convertisseurs ont été conçus selon le même schéma, ils ont donc des entrées/sorties similaires.

Des capacités de type MOM ont été placées sur la puce, là où la place était disponible. Ces capacités sont construites avec les cinq premiers niveaux de métallisation, auxquels ont été ajoutés des niveaux supplémentaires pour pouvoir les connecter facilement entre elles. Il a été possible d'embarquer environ 2 nF au total par puce. La moitié de cette valeur a été réservée pour le découplage de la tension d'alimentation principale, le reste pour les circuits de commande (trois sources de tensions). La répartition géographique varie selon le type de convertisseur considéré (standard ou cascode), mais les valeurs sont très similaires.

Le routage de niveau haut est fait avec le dernier niveau de métal, le plus épais. Ce niveau est donc crucial pour limiter les résistances d'accès aux composants. Les connexions aux capacités sont renforcées par ce dernier niveau, et les transistors de puissance sont recouverts au maximum de ce métal.

Conclusion

L'ensemble des circuits actifs utilisés dans ce travail ont été présentés précédemment. Deux puces avec des fonctionnalités similaires mais des implémentations très différentes ont été conçues. La similarité permettra de comparer objectivement les deux structures considérées (standard et cascode) et de tirer des conclusions solides.

Le dessin des masques est une étape majeure de la conception, lors de laquelle la performance d'un circuit peut être fortement dégradée. Il convient de respecter des règles et d'optimiser le dessin en conséquence. Concernant le matching, une approche classique a été utilisée.

Finalement, les problématiques de positionnement sur la puce, et d'optimisation globale ont été présentées, avec les contraintes spécifiques du cas présent. Au final, deux puces ont été conçues, avec chacune deux convertisseurs embarqués, permettant plusieurs configurations de test.

Chapitre 4 : Tests et résultats de mesures

Ce chapitre présente les différents résultats de mesure qui ont été obtenus sur les différents éléments constituant le convertisseur, ainsi que sur le convertisseur complet. Les particularités des tests sont présentées, ainsi que les problèmes liés à la mise en œuvre des tests. Les mesures sur les inductances et les capacités sont présentées, puis les mesures du convertisseur sont présentées et comparées aux résultats de simulation.

Spécificités des mesures

La difficulté majeur des mesures est le fonctionnement à haute fréquence (+100 MHz). Beaucoup d'harmoniques haute fréquence sont présentes dans les signaux mesurés. Une mesure précise de celles-ci requiert des appareils avec une grande bande passante. De plus, à ces fréquences, une inductance ou une capacité parasite minime devient significative.

L'impédance des outils de mesure peut aussi poser problème. Une sonde de tension possède généralement une capacité d'entrée, qui impactera le circuit lors de sa connexion. De fait, il est impossible d'avoir accès de façon certaine

au « vrai » signal, car la mesure altère le signal lui-même. Les mesures sont aussi à faible tension, ce qui implique des mesures quatre points, qui peuvent être difficiles à réaliser à cause de la taille des éléments mesurés.

Un impédance-mètre est utilisé pour la caractérisation des composants passifs. Cet impédance-mètre est un Agilent 4294A, capable d'effectuer des mesures jusqu'à 110 MHz. Il est associé à une table de mesure sous pointes pour une prise de contact précise, ainsi que des pointes de type « True-Kelvin ». Une évaluation de la précision de l'appareil a été faite, et il a été conclu que la mesure d'inductances et de capacités est relativement précise.

Les mesures temporelles sont réalisées avec des sondes CT6 (de Tektronix) pour le courant et TAP1500 (de Tektronix) pour la tension. Un oscilloscope large bande (2,5 GHz) est utilisé pour visualiser les différents signaux. Un générateur d'impulsions Agilent 81132A est utilisé pour la génération des signaux d'horloge. Un amplificateur TI TH4302 est parfois ajouté pour augmenter la capacité en courant du générateur.

Les mesures de puissances sont effectuées en continu pour éviter toute erreur liée aux déphasages des appareils de mesure. Ceci est réalisable au niveau de chaque source de tension utilisée. Une source électronique permet de mesurer la puissance de sortie, tout en autorisant des changements de charge faciles.

Interposeur capacitif

L'interposeur capacitif comprend cinq capacités, ainsi qu'une matrice de plots pour la connexion du circuit intégré. Une empreinte 0402 a été ajoutée pour la connexion d'une inductance commerciale. Les capacités de découplage ont été mesurées par le fabricant. Toutes les capacités affichent une fréquence de résonance supérieure à 330 MHz, ainsi que des valeurs très proches de celle de conception. Les éléments parasites critiques sur cet interposeur sont l'inductance entre la capacité d'entrée et le plot de connexion du circuit intégré et la capacité parasite avec la masse du nœud V_{LX}. L'inductance parasite a été minimisée par conception (avec une longueur de piste inférieure à 150 µm) et est trop faible pour pouvoir la mesurer précisément. La capacité parasite de V_{LX} a été mesurée et est d'environ 6,5 pF.

Inductances magnétiques intégrées

Les inductances magnétiques intégrées conçues pour le circuit sont au nombre de quatre. Deux sont des inductances simples, deux sont couplées avec différents coefficients de couplage. De plus, deux inductances commerciales de Coilcraft sont aussi utilisées.

Les inductances ont d'abord été mesurées avec l'impédance-mètre. Toutes les inductances ont suivi la même procédure de calibration/compensation avant chaque test. On retient de ces mesures que les valeurs effectives sont légèrement plus faibles que celles conçues au départ. Les valeurs d'inductance commencent à chuter aux alentours de 7 MHz pour toutes les inductances, mais restent relativement élevées à 110 MHz. La résistance suit un comportent inverse. En comparaison, les inductances commerciales présentent une résistance plus faible, mais un comportement en haute fréquence moins bon.

Les inductances intégrées ont ensuite été mesurées dans le domaine temporel pour évaluer leurs performances dans des conditions plus proches de l'application souhaitée. L'amplificateur TI THS4302 a été utilisé pour émuler un étage de puissance et charger en courant les inductances. Les formes d'ondes de tensions et courants ont été mesurées, et il a été possible de retrouver une valeur d'inductance et de résistance en intégrant la tension aux bornes de l'inductance. Cette même méthode d'identification a été utilisée sur les inductances couplées, permettant aussi de remonter au coefficient de couplage des enroulements. Les résultats sont cohérents avec les mesures faites avec l'impédance-mètre. Ceci valide donc la caractérisation harmonique de ces composants pour une utilisation dans un système de type hacheur.

Convertisseur

Les premières mesures effectuées sur le convertisseur ont été faites en reportant le circuit intégré directement sur un PCB, et en utilisant des condensateurs commerciaux (Murata) de valeurs équivalentes à celles de l'interposeur. Ces mesures ont tout d'abord permis de valider la fonctionnalité du convertisseur, sans risques liés à l'assemblage 3D. Un fonctionnement correct a été observé, autant pour la tension que le courant dans l'inductance. Des oscillations parasites ont été observées. Ces problèmes sont discutés plus en profondeur dans le

cas de l'assemblage 3D. Un impact non-négligeable des sondes sur les formes d'onde a aussi été mis en avant, confirmant les difficultés de mesures mises en avant dans la partie précédente.

Les mesures temporelles ont permis d'estimer la valeur de l'inductance parasite de la capacité de sortie. Cette inductance génère une tension carrée aux bornes du condensateur de sortie. Ceci confirme les limitations des condensateurs céramiques pour les applications hautes fréquences.

Un banc de mesure des performances a été mis en place, permettant de mesurer l'ensemble des tensions et courants aux entrées/sorties du convertisseur, ainsi que le rapport cyclique et la fréquence du signal de commande. Ceci permet de calculer assez simplement le rendement du système. Il permet aussi d'évaluer la fonction de transfert statique du convertisseur, c'est-à-dire l'évolution de la tension de sortie en fonction du rapport cyclique. Cette évolution permet de visualiser assez rapidement si le convertisseur fonctionne de façon prédictible ou non.

Dans le cas de l'assemblage sur PCB, des mesures instables ont été relevées, démontrant la non-efficacité du découplage avec les condensateurs commerciaux. De plus, ces instabilités limitent les conclusions pouvant être tirées au sujet du rendement et des pertes du convertisseur. Il est nécessaire de restreindre l'espace d'étude (fréquence et courant de sortie) pour avoir des résultats cohérents.

Les pertes des circuits de commande évoluent à peu près linéairement avec la fréquence, comme on peut l'attendre. Le rendement du convertisseur est maximal aux alentours de 150 mA de courant de charge pour le convertisseur opérant à 100 MHz. Ce résultat était attendu, car le convertisseur a été optimisé pour 140 mA.

L'analyse est ensuite faite sur le circuit assemblé sur interposeur. Ces tests permettent deux comparaisons primordiales : tout d'abord la comparaison de la même puce avec et sans interposeur, puis la comparaison de deux puces différentes (standard et cascode) sur interposeur. L'assemblage 3D est connecté en utilisant des fils de bonding sur un PCB. Aucun composant passif n'est ajouté. Il est possible de modéliser l'assemblage puce/interposeur/PCB par un circuit équivalent, mettant en évidence un multitude de couplages parasites, limitant les mesures possibles.

Lorsque l'on compare le fonctionnement du convertisseur cascode avec le convertisseur standard, il est impossible d'après les formes d'ondes en tension (nœud V_{LX} et V_{OUT}) de différencier l'un de l'autre. Ceci confirme le fonctionnement de l'étage de puissance cascode comme étant équivalent à un étage de puissance standard. La mesure des tensions de référence permet aussi de mettre en évidence une meilleure stabilité des tensions du côté du convertisseur cascode. Ceci vient du fait que le convertisseur cascode requiert moins de courant, donc perturbe moins les capacité de découplage.

Comme dans le cas de l'assemblage sur PCB, la tension de sortie a été mesurée en fonction du rapport cyclique. Dans le cas de l'assemblage 3D, le comportement est très prédictible, aucune mesure incohérente n'est remarquée. Ceci confirme l'intérêt de l'interposeur et des capacitées en tranchées pour du découplage à haute fréquence.

La comparaison des pertes mesurées avec les simulations PLS montre une bonne estimation des pertes par la simulation. Cette estimation est plus mauvaise à faible fréquence, car la simulation ne modélisant pas l'inductance, aucune perte liée à l'ondulation en courant n'a été prise en compte.

Finalement, les rendements globaux sont calculés et comparés les uns aux autres. Le convertisseur cascode présente un rendement largement supérieur au convertisseur standard. Un rendement pic de plus de 90 % est démontré.

Des mesures à l'aide d'une caméra thermique ont été effectuées. Ces mesures ont seulement un objectif de mesures qualitatives. Elles mettent en évidence l'échauffement de l'inductance avec la fréquence (pertes liées au matériau). Les pertes des circuits de commande échauffent aussi la puce à haute fréquence.

Finalement, une comparaison avec l'état de l'art est présentée. Celle-ci montre l'intérêt du convertisseur cascode, en présentant des rendements similaires aux convertisseurs opérant à 10 MHz en fonctionnant une décade au-dessus. Le convertisseur standard quant à lui présente des performances conformes à l'état de l'art.

En conclusion, la démonstration d'un ensemble de technologies et procédés a été faite, chaque élément ayant été caractérisé. Le convertisseur assemblé démontre des performances supérieures à celles présentes dans l'état de l'art, validant ainsi les choix de conception faits en amont.

Conclusion générale

Le travail présenté supporte la démonstration d'un SMPS à haute fréquence de commutation, avec un rendement significatif. Le chapitre 1 a permis d'identifier l'idée d'un convertisseur à plusieurs phases couplées. Dans le cadre du projet, l'objectif était donc de valider expérimentalement la faisabilité d'un tel convertisseur. Des considérations initiales ont permis de mettre en avant l'intérêt d'un étage de puissance de type cascode. De plus, la littérature ne fournissait aucun résultat sur cette structure.

Résumé des contributions

Le convertisseur cascode proposé adresse des défis clés rencontrés au sein des convertisseurs intégrés. Les contributions sont les suivantes :

- Le choix d'une architecture de convertisseur est un aspect clé. Des considérations à ce sujet ont été développées et présentées dans le chapitre 2, dans le cas d'un fonctionnement à haute fréquence.
- Qu'elle soit choisie ou imposée, la technologie des composants actifs impacte fortement le convertisseur. Une méthode pour analyser cette technologie et choisir en conséquence est développée dans le chapitre 2. Bien qu'utilisant des modèles simples, cette méthode a démontré son efficacité.
- Un étage de puissance innovant a été validé dans le chapitre 4 après avoir été conçu dans le chapitre 3. Un gain de performance significatif a été démontré en comparaison d'une approche classique pour une technologie similaire.
- Un assemblage 3D original a été testé dans le chapitre 4 et comparé à une approche classique, justifiant l'intérêt de l'approche 3D pour la haute fréquence.
- Finalement la comparaison avec l'état de l'art établit que l'étage de puissance cascode est capable de performances similaires à celles de convertisseurs opérant une décade plus basse, permettant donc un gain en surface et en densité de puissance.

Le travail présenté adresse le principal problème de la conception de convertisseur DC-DC utilisant des technologies faible tension (CMOS numérique). Cette stratégie étend les possibilités de l'alimentation sur puce, sans pour autant être incompatible avec une approche d'alimentation sur PCB.

Perspectives

L'accès au silicium étant limité, la restriction à une structure en boucle ouverte pour la validation de l'étage de puissance cascode était plus judicieuse. Ceci a aussi permis d'évaluer correctement l'assemblage 3D. Cependant le travail réalisé ne peut être qualifié de définitif. Les problématiques à court terme doivent être adressées dans un travail futur. Il convient ensuite de projeter le concept développé ici dans un système plus complet, au sein d'activités à moyen et long terme.

Les activités à très court terme sont celles ne pouvant être réalisées sans aucune re-conception des circuits passifs actifs. L'optimisation de l'environnement de test devrait permettre d'améliorer la qualité des mesures, notamment dans le domaine temporel. L'impact des composants parasites a été démontré, et celui-ci doit être minimisé autant que possible. Le test utilisant deux phases et les inductances couplées peut être réalisé directement via un assemblage sur PCB des différents éléments. Bien que non-optimal, ce test permettra de valider le concept des inductances couplées.

Une re-conception rapide du circuit actif permettra d'intégrer la boucle de régulation, et le convertisseur pourra être évalué en termes des performances dynamiques. Plusieurs méthodes de contrôle peuvent être envisagées afin d'optimiser les performances.

Il est possible d'inclure dans cette même re-conception un circuit permettant de générer de façon interne les références de tension requises. Une convertisseur à capacités commutées 3:1 de type « ladder » semble approprié pour cette fonction. L'impact sur le rendement devra être évalué.

L'étape suivante est l'optimisation de l'assemblage 3D. Ceci permettra tout d'abord de l'optimiser pour les mesures. De plus, les composants sont actuellement reportés sur l'interposeur, et non pas co-intégrés. Réaliser cette co-intégration permettra d'obtenir un interposeur quasi-définitif. Cet interposeur

devra aussi pourvoir accueillir un convertisseur deux phases. Une extension du nombre de phases (4, 8 ou plus) peut également être envisagée.

Il devient nécessaire d'optimiser le circuit actif. L'analyse de la fiabilité du circuit est une étape majeure qui doit être adressée. Une évaluation de compatibilité électromagnétique est nécessaire. Des protections ESD robustes doivent être mises en place pour garantir la robustesse du circuit. Une co-conception avec l'interposeur semble alors être une nécessité.

Á plus long terme vient la démonstration d'un convertisseur de type PMU avec toutes ses fonctionnalités. Un aspect majeur négligé jusqu'à présent est le fonctionnement en DCM de la structure proposée. Le circuit présenté ne permet pas ce type d'opération. Une modification de l'étage de puissance devient donc nécessaire, ainsi que l'implémentation d'un superviseur permettant de gérer les modes de fonctionnement.

L'ajout d'un chemin d'énergie additionnel renforcera les performances dynamiques, notamment dans le cadre d'un fonctionnement de type DVS. L'utilisation d'un interposeur propose un cadre de travail adéquat pour l'ajout de composants passifs, qui sont souvent requis dans ce type d'approche.

Le pendant du PMU est l'utilisation de ce convertisseur au sein d'un SoC pour de l'alimentation sur puce. La charge digitale devra être inclue avec le convertisseur. La difficulté sera ici plus liée à l'interposeur, en raison des multiples entrées/sorties des fonctions numériques.

General introduction

DC-DC conversion is a key functional block in almost any embedded electronic system. DC-DC converters are found in a various range of applications, including consumer electronics, automotive, portable devices, etc. The need for integrated DC-DC converters comes from the fact that more and more electronic functions are embedded into electrical devices. These electronic functions are achieved using dedicated integrated circuits that requires a constant, low-voltage DC power supplies. The DC voltage buses are distributed at the level of the platform that receives the integrated circuits that build the various functions of the system. The control of one DC voltage bus indeed requires a DC-DC converter as the primary energy source of the system is different from the one needed by an integrated circuit. The DC-DC converters are generally gathered into a so-called Power Management Units (PMUs). Power management can be seen as ICT – Information and Communication Technologies – for energy processing: power management is required to ensure that energy is locally and in real time, used in an efficient and smart manner.

DC-DC converter requirements

Requirements for these DC-DC converters are application-dependent. However an universal power management specification would be that a DC-DC converter takes up no space, cost nothing, last forever and has zero power

loss. These universal specifications lead to the major trade-offs seen in DC-DC conversion: power density, cost (area and bill of materials), reliability and power efficiency. The weights put on these key metrics are application-dependent. For instance, on the consumer electronic side, reliability is not a major concern, whereas design is cost-driven. In portable devices (hand-held consumer electronics) efficiency is the number one concern as it impacts both the battery lifetime and the heat generation inside the device. The key here is to limit the losses as much as possible. Besides the cost concern can be translated in a footprint issue. In the case of portable devices, reducing the size of the PMU might allow to embed more battery volume, making the device last longer.

The functional integrated circuits are growing in terms of blocks and heterogeneity. They are called Systems on Chip (SoCs). They necessitate more internal power domains linked to more DC voltage buses. Energy distribution can be seen as distributed through a power supply grid: that can be assimilated as a nano-grid on-chip. The interest is to serve independent DC voltage buses on the one hand. On the other hand, it comes the concerns of specific transient performances. Having a DC-DC converter that can react fast to a load, line and/or reference change is a key enabler for high efficiency processing. A fast power supply can adapt its output voltage closely to the load needs and supply just the power required for the processing to occur, reducing the wasted energy when only small computing resources are needed.

In other applications fields, reliability becomes number one concern. This is the case in automotive and aeronautics. However even in reliability-driven fields, the need for integration is present and efficiency and footprint remain major issues.

Industry status

Major consolidations in industry took place in the recent years. Integrated circuit design and manufacturing companies seem to buy power supply companies to strengthen their market position. This is the indicator that power supply is becoming a key function and need to be well controlled to ensure an optimum system. In 2012, Qualcomm, a major player in the SoC world, bought

Summit Microelectronics, a leading developer and provider of programmable power integrated circuits. Qualcomm also bought Nujira in 2015. Nujira was a company developing power supplies dedicated to envelope tracking, a key function for efficient RF communication. In 2013, Altera, a famous manufacturer of reconfigurable digital circuits, bought Enpirion for on-chip power conversion. Intel then bought Altera in 2015. In 2013 Maxim Integrated, that designs and sells integrated analog and mixed-signal circuits, bought Volterra Semiconductor, a fabless semiconductor company that designed mixed-signal integrated circuits used in power management applications. In 2014, Infineon bought International Rectifier, and in 2015, Micrel was acquired by Microchip. Finally even if it is not motivated by the same idea of competence acquisition, the merging of Freescale in NXP leads to the same results.

PowerSWIPE project

Today's cars contain up to 70 electronic control units, using sophisticated silicon chips known as micro-controllers. Currently, these micro-controllers are supplied with a range of different voltages from power supplies which take up a lot of space and waste energy. The vision for automotive control units in 2020 is that these power supplies will be miniaturized and integrated directly with the micro-controller chip, thereby dramatically saving space and weight while at the same time reducing energy use, CO_2 emissions and manufacturing costs of next generation automotive electronics systems.

Nowadays micro-controllers in Engine Control Units (ECUs) are supplied using mostly linear regulators, that have low power processing efficiency. The road-map is to go from linear regulators to Switched-Mode Power Supplies (SMPSs) without impacting the footprint and the cost of the final solution. The PowerSWIPE project[3] – EU FP7 318529 – addresses this challenge by proposing the combination of several institutes and companies[4] that can supply cutting edge technologies to address power supply integration.

[3] http://www.powerswipe.eu

[4] Tyndall National Institute (Cork, Ireland), Infineon Technologies AG (Regensburg, Germany), Infineon Technologies Austria AG (Villach, Austria), IPDiA SA (Caen, France) Centro de Electroñica Industrial, UPM, (Madrid, Spain), Robert Bosch GmbH (Stuttgart, Germany), Ampère laboratory, University of Lyon (Lyon, France)

The present work is part of this project and addresses the concern of high efficiency while pushing the power density.

Manuscript content

The main goal is to validate a solution of power supply using 3D integration to operate at 200 MHz with a peak efficiency larger than 90 %.

Chapter 1 reviews the state-of-the-art, to highlight the ingredients of high-switching frequency buck converters. A conclusion lists the principal choices of architectures to preserve efficiency while pushing the switching frequency.

Chapter 2 covers the design methodology from system-level to component-level. Control of high-switching frequency SMPSs has been demonstrated in literature. The work is then restricted to a demonstration related to technology and design. A broad power stage is considered without the close-loop concern.

Chapter 3 is dedicated to Integrated Circuit (IC) design. Various prototypes have been designed. The fabrication of these prototypes has been the responsibility of industrial partners in the PowerSWIPE project.

Chapter 4 gathers all components experimental characterizations and measurements on prototypes. The performances and the limitations of each converter option have been discussed. The results correspond and even overpass the project expectations concerning the high-switching frequency SMPS.

Chapter 5 summarizes the key achievements of this work, along with the associated perspectives. The achievements include the demonstration of the proper operation of the three-MOSFET cascode power stage, as well as the efficiency figures obtained that go beyond the current state-of-the-art.

Chapter 1

State-of-the-art

Contents

This chapter details the major concerns faced when designing an integrated DC-DC converter, focusing on the System on Chip (SoC) and System in Package (SiP) approach. These concerns are presented toward the design specifications. They include a discussion on system level, as well as some major design choices, e.g. the switching frequency and the existing efficiency

enhancement strategies. Current commercial trends are briefly presented. DC-DC converters principle of operation is depicted, assuming a linear behavior of the components. A review of state-of-the-art DC-DC converters is then presented, with a discussion about relevant metrics. Performance analysis is also pushed to the component-level, discriminating passive and active components, as well as assembly and packaging aspects. Based on all the developed considerations, specifications are then refined and various technological constraints are presented.

1.1 Primary concerns

When designing a DC-DC converter for an integrated electronic system, many concerns need to be addressed. The first one is the system architecture of the full system, i.e. the number, locations and footprints of the DC-DC converters. Then regarding the converter itself, design choices need to be performed in order to achieve the targeted performances. A glance at the state-of-the-art in the industry is projected, showing how these concerns are addressed in commercial products.

1.1.1 System level considerations

At system level, given an application with various voltage domains (e.g. a complex SoC) it is necessary to choose between two major arrangements:

- A system with many off-chip converters, each one supplying a voltage domain,
- A system with one off-chip converter and many local (on-chip) converters.

These two approaches are depicted in Figure 1.1 and Figure 1.2 respectively. This change in paradigm is companion to the development of large SoCs where many power domains are mandatory to master the power consumption [Kim08]. For instance, Dynamic Voltage Scaling (DVS) helps achieving better energy efficiency but requires good power supplies performances.

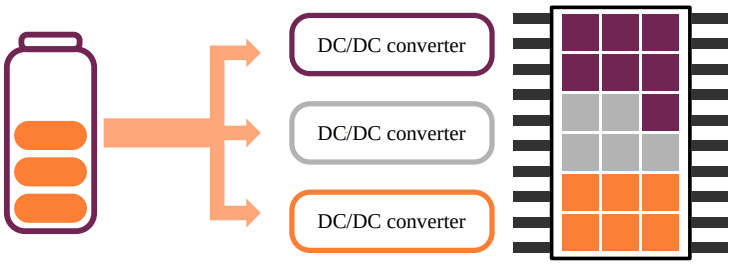


Figure 1.1 – System with off-chip DC-DC converters serving a multi-power domain SoC.

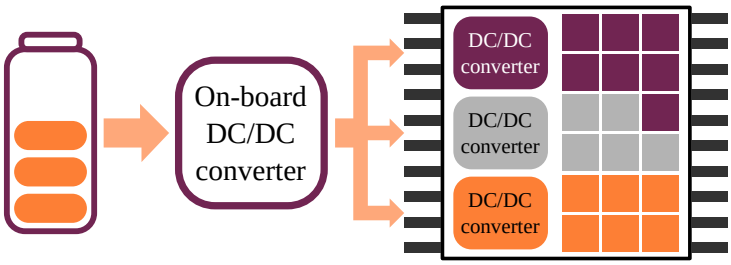


Figure 1.2 – System with on-chip DC-DC converters embedded along the power domains in the SoC.

Both approaches present benefits and drawbacks. For the first approach (using many on-board DC-DC converters and no local converters) the major drawbacks are:

- The important need for decoupling, requiring many capacitors and magnetic components as well,
- Non-negligible Printed Circuit Board (PCB) traces losses when supplying a large current to the load,
- Limited transient performances that limit DVS operation.

They are however interesting in some ways:

- The passive components are on-board, allowing for easy mounting, multi-source and industrial adaptation,

- The converter can be manufactured using the most suitable technology, without any additional external constraint.

This approach has been the one classically used in any electronic system, leaving the Integrated Circuit (IC) design to the analog/digital designers and the power design to the system/power designers. In this approach, power is seen as a commodity, that the IC designer can use. Unfortunately market calls for a higher factor of segmentation of the powering functions due to increasing functionalities. Seamless integration is now a key stone.

The second approach (using one board DC-DC converter and many on-chip DC-DC converter) is more recent, and exhibits some major advantages:

- They can help achieving PCB area savings,
- Transient performances can be enhanced thanks to a much closeness to the load, leading to an accurate feedback,
- Losses in PCB traces can be reduced drastically.

Drawbacks also exist in this approach:

- There is a need for "local" passive components, inductors and capacitors, which can be costly when integrated in a deeper manner,
- The technology of on-chip converter is the one of the IC, e.g. a low voltage digital Complementary Metal-Oxide-Semiconductor (CMOS) technology, not well suited for power issues.

In the second approach, power becomes a key functionality of the full design. It is no longer possible to have the IC designers working independently of the system designers.

1.1.2 Design tools and CAD

An important aspect to power supplies design is the choice of the Computer Aided Design (CAD) tools that are utilized for designing the system. In the case of a DC-DC converter, the full system design usually requires heterogeneous optimization tools. A typical DC-DC converter is composed of an active

switching part, inductor(s) and capacitor(s), each part requiring specific design care. Several approaches can be used to address such a complex design issue. At one end there is the use of a dedicated, specialized tool for each system part, and the other end is the use of an integrated design tool that takes into account all parts of the system.

The first approach benefits from accurate, dedicated models. For instance, active circuit can be done using fine transistor modeling using Simulation Program With Integrated Circuit Emphasis (SPICE), inductance and capacitance optimization using finite element analysis tools and magnetic-centric softwares. The main issue of this approach is that no tool is aware of the others, making it difficult to achieve optimal system level performance. A system level optimization using this approach requires iterative design of each part.

The objective of the second method (integrated design tool) is to address the system level performance from the beginning. However it requires models for each part of the system that can be understood by the same tools. This is usually achieved at the expense of complexity, making the models less accurate for each part (compared to the use of dedicated tools and models).

In between those two extreme cases, there are several methods that are also conceivable. One method often used is to model some parts using the tools dedicated to another one, for instance modeling the magnetic inductors and capacitors using the transistor level simulation-tools in SPICE environment. Doing this makes capacitors and inductors models less accurate – e.g. magnetic behavior is lost, as well as voltage breakdown of capacitor – but ease the system design. Some tools can also dialog together, allowing for instance to mix finite element simulation with SPICE simulation.

1.1.3 Commercial trends

In the industry, some significant trends can be seen in the integrated DC-DC conversion world. Major players in the industry have recently demonstrated products.

Intel has presented its new processor family (codenamed Haswell), that includes Fully Integrated Voltage Regulator (FIVR) [Kur15] – along with many other innovations. These FIVRs are multiphase buck converters implemented close to the digital on-die load, allowing for fast, fine grain voltage control of

the load. Converter phases are switching at 140 MHz. Passive components are implemented at the PCB level, using air-core PCB trace inductor and Metal-Insulator-Metal (MIM) capacitors.

Texas Instruments proposes standalone DC-DC converters that are fully integrated in package [TI11]. This converter integrates both the IC, the capacitors and the inductor in the same package. Passive components are stacked on top of the IC. This is the Power Supply in Package (PowerSiP) approach. The goal is to increase the power density of on-board DC-DC converters.

Enpirion Power Solutions company (subsidiary of Altera, itself property of Intel) is proposing another approach. Their idea is to go to a monolithic, fully integrated DC-DC converter [Lot11]. This can be referred as the Power System on Chip (PowerSoC) approach. Power density is again one of the major concern here, but this approach requires more integration efforts.

1.1.4 Converter structure

Many DC-DC converter structures are available for DC voltage conversion. They are divided in two major categories:

- Isolated DC-DC converters,
- Non-isolated DC-DC converters.

In addition to convert a DC voltage to another one, an isolated DC-DC converter provides a galvanic isolation between the input and the output power. The isolation is not something that is always needed (or wanted) so the decision to go for one category or another is strongly application dependent.

Many converter structures exist in each category. In each category, they can be discriminated in three sub-categories regarding their main functionality:

- Step-down capable converters,
- Step-up capable converters,
- Step-down and step-up capable converters.

This choice is dictated by the input and output voltage range required for the application.

Any structure comes with its share of trade-offs between various performance aspects. For instance, some structures will give better efficiency by sacrificing a bit the transient performances, or some others will give a better transient response at the expense of ElectroMagnetic Interference (EMI). Therefore the selection of the structure is a key step in the design process as it lays out the global performance trade-offs of the system.

1.1.5 Operating frequency

Once the choices for an architecture and a structure have been made, one needs to decide at which frequency the converter will operate. This is a crucial decision as it will have a major impact on the design, as well as on many metrics of the converter [Nev14]. A converter switching at high frequency will require smaller passive component values (compared to one switching at lower frequency). This implies that these passive components can be smaller, thus the total footprint of the converter is reduced, increasing its power density. Figure 1.3 depicts the expected gain in area and volume when going to higher frequency. This shows the effect of using smaller components first, and then being able to integrate them inside the chip package itself.

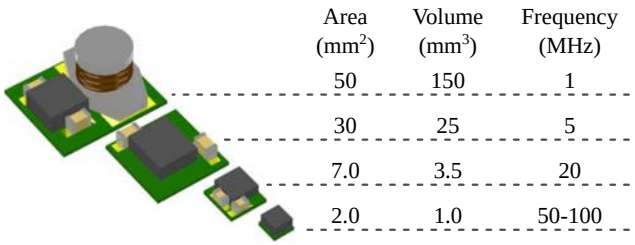


Figure 1.3 – Expected area and volume reduction at high frequency [Wan10].

However increasing the switching frequency is known to increase the losses [Gil02], leading to an inefficient conversion and generating unwanted heat that must be addressed with an induced cost.

Switching frequency also has an impact on the EMI performance of the system [Aul13] and on the size of required EMI filters for the system to comply

to norms. As the operating frequency is higher, the components required to filter the perturbations can be reduced, increasing the overall compactness.

Increasing the frequency makes the converter faster to react to a load or a reference change, improving transient performance without having to use complex control strategies. The current in the inductor can change faster, as its value decreases with frequency, allowing for faster $\mathrm{d}i/\mathrm{d}t$.

The main trade-off is then on how much efficiency points a designer is willing to pay in order to improve some of the previously mentioned metrics.

1.1.6 Strategies for efficiency enhancement

In order to improve the efficiency of the DC-DC converters, many strategies have been proposed in literature. For high frequency conversion, these strategies are aiming to mainly reduce the switching losses of the converter. Some techniques are presented below. These techniques are not exclusive. They can be combined together to increase efficiency, usually at the expense of complexity. For instance the converter proposed in [Abe07] combines Zero Voltage Switching (ZVS) strategy in a multiphase structure.

1.1.6.1 Switching operation optimization

One way of reducing the losses is to analyze and optimize the switching cycle of the power devices. The interest of ZVS has been demonstrated in [Abe07], presenting efficiency figures of two similar converters, one with ZVS operation and one without. The ZVS converter presents a much better efficiency than its non-ZVS counterpart. Basic ZVS behavior is to turn on the power switch when the voltage across its terminals is equal to zero. This reduces losses as the $V \cdot I$ product is null during turn on.

Another similar well known approach is to go to Zero Current Switching (ZCS). The principle of this method is to turn off the power switch when the current through it is equal to zero. Again the goal is to have a $V \cdot I$ product null during turn-off. This behavior can be forced using a resonant or quasi-resonant operation of the converter in order to have the current naturally decreasing before the switching operation.

Additional passive components are required to introduce the necessary resonance. At high operating frequency, parasitic components are considered.

Unfortunately CMOS technology is affected by variability that makes the control of capacitor and inductor value difficult, resulting in a quite impractical approach.

1.1.6.2 Power switch drivers' optimization

The drivers in a DC-DC converter are generating a significant amount of losses. Some techniques can be used to reduce their losses.

A resonant gate driver has been proposed in [Bat12a]. It allows to reduce the gate drive losses by reusing some of the electrical charges needed for turning on and off the power switches. A significant efficiency enhancement is demonstrated at the expense of power density.

Another technique is to reduce the voltage swing of the drivers in order get the optimum trade-off between switching and conduction losses of the main switch. This has been presented in [Kur04], demonstrating a +3.9 % efficiency gain compared to a classical design.

1.1.6.3 Further optimization strategies

Many other strategies have been proposed. The use of multiphase converter helps keeping a high efficiency over a wide load range by using a phase shedding scheme. The goal is to use each phase near its optimum load current. This approach has been demonstrated in [Kim15; Bur14; Son14b; Hua13].

The segmentation of the converter can also be considered at the component level. The goal is to get the best achievable efficiency over the maximum number of operation points, i.e. various load current and output voltage configurations. This technique has been used in [Mar14; Aro13].

In multiphase converters, it has been proposed to use coupled inductors in order to reduce the current ripple, thus reducing the conduction losses of the converter. Reducing the current ripple can also allow to reduce the switching frequency, thus reducing the switching losses. Various coupled structures have been tested in [Pen13; Stu13; Wib08a; Wib08b].

1.2 DC-DC principle of operation

This section present the principle of operation of some DC-DC converter structure. The presented structures are limited to few relevant non-isolated DC-DC converters. The focus is on step-down capable converter. The goal is to provide a quick insight into the converter structures and the circuit behavior. Three major DC-DC converter families are presented: linear voltage converter, switched-capacitors converters and inductive converters.

1.2.1 Linear voltage converter

This family of DC-DC converters acts as a resistive divider. Excess power is dissipated through a variable resistor in order to ensure a regulated output voltage. Figure 1.4 depicts a streamlined linear voltage regulator circuit. The output voltage is controlled by varying the R_{VAR} resistor in order to have an output voltage equal to the reference voltage.

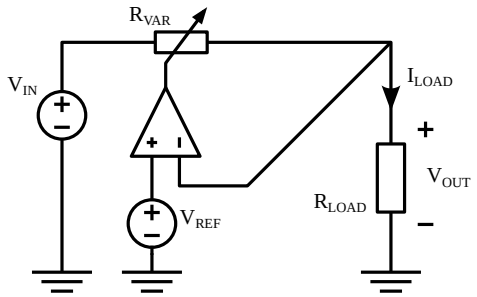
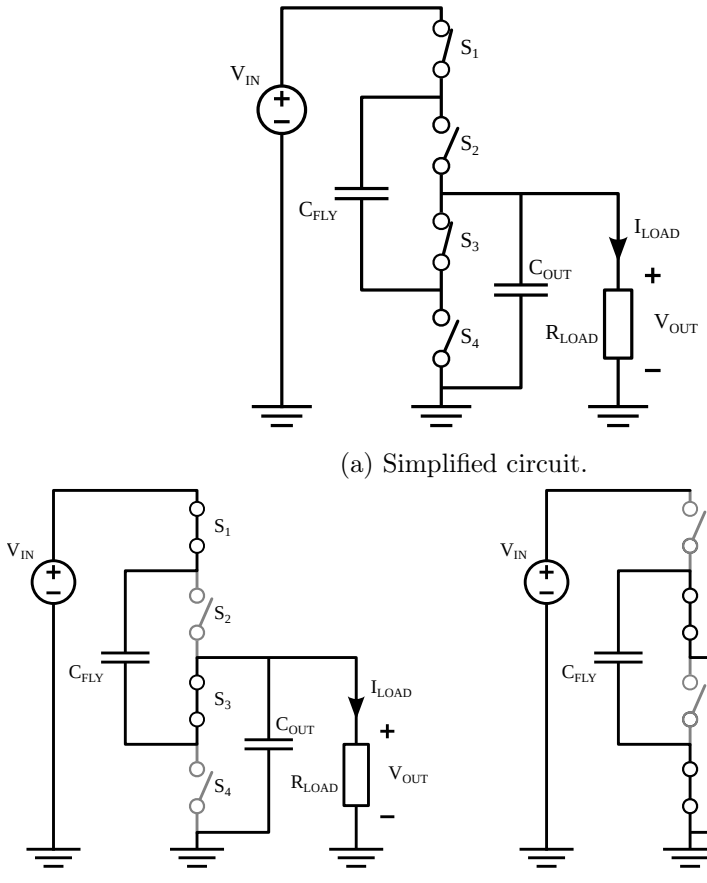


Figure 1.4 – Linear voltage regulator simplified circuit.

There are no switching components in such a regulator, allowing for low noise regulation. Regulation can also be very fast. It is mainly dependent on the bandwidth of the feedback loop [Cou13]. However since it acts as a resistive divider, efficiency is strongly related to conversion ratio. This implies that the conversion efficiency is very low when the voltage drop across the converter is close to the input voltage. Therefore these converters are mainly used to regulate an output voltage close to the input voltage, giving them the name of Low Drop-Out (LDO) regulator.

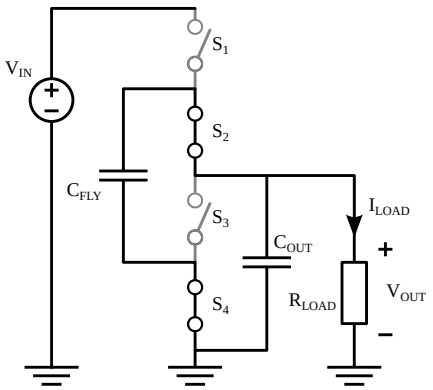
1.2.2 Switched-capacitor DC-DC converters

A switched-capacitor DC-DC converter (also referred to as charge pump) utilizes a set of switches and capacitors to divide a voltage. The division factor is architecture-dependent but it is possible to have reconfigurable structures, allowing for multi-ratio conversion.



(a) Simplified circuit.

(b) Circuit in phase 1.



(c) Circuit in phase 2.

Figure 1.5 – A 2-to-1 switched-capacitor converter.

Figure 1.5 is a 2-to-1 switched-capacitor converter. It consists in a set of 4 switches (S_1, S_2, S_3 and S_4) and 2 capacitors (C_{FLY} and C_{OUT}). Switches are driven with 50 % duty cycle.

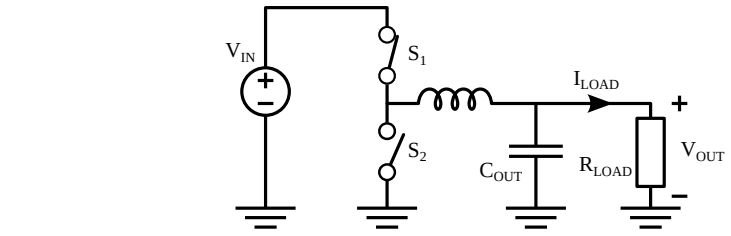
During phase 1 (depicted in Figure 1.5b) the two capacitors are charged in series, each one seeing half the input voltage. Capacitors are then placed in parallel during phase 2 (Figure 1.5c), both supplying current to the load.

The interest for this family of converters comes from the absence of inductor, making their integration easier and CMOS compatible (no need for magnetic components). It is also possible to regulate the output voltage of these converters [Sou14]. When regulated, these converters behave like an ideal voltage divider followed by a linear voltage regulator.

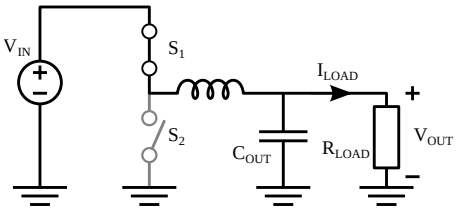
1.2.3 Inductive DC-DC converters

1.2.3.1 Classical inductive Buck-type converter

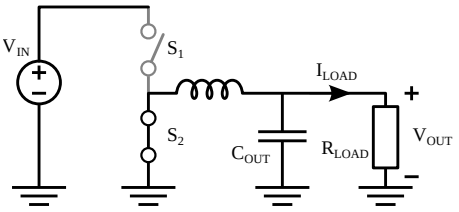
An inductive DC-DC converter combines an inductor and a capacitor. The inductor is used for current filtering and the capacitor for voltage filtering. Figure 1.6 depicts a simplified circuit of a synchronous Buck converter. Switches S_1 and S_2 are complementarily driven (when one is closed, the other one is opened).



(a) Simplified circuit.



(b) Circuit in phase 1.



(c) Circuit in phase 2.

Figure 1.6 – Buck type regulator converter in continuous conduction mode.

During phase 1 (Figure 1.6b), the high-side switch (S_1) is closed and the low-side switch (S_2) is opened. The voltage at the input of the inductor is V_{IN} and the current through the inductor is increasing as V_{OUT} is lower than V_{IN}. In phase 2 (Figure 1.6c), the low-side switch is closed and the high-side switch opened. The voltage at the input of the inductor is then 0 V, making the current in the inductor to decrease.

Voltage regulation of the output is done by varying the duty cycle of the switches. Theoretically, with all components considered ideal, the efficiency of this converter is close to 1. This converter is further discussed in Section 2.1.

1.2.3.2 Three-level DC-DC converter

A three-level converter lies in between an inductive converter and a switched-capacitor converter. Figure 1.7 presents a simplified circuit of a 3-level converter. The output filter is the same as the one in a classical inductive converter (LC filter) but the voltage applied at the input of the filter is not. A flying capacitor is used to reduce the voltage swing at the input of the inductor. A voltage of V_{IN}, $V_{IN}/2$ and 0 V can be applied at the input of the inductor, allowing to reduce the current ripple. This converter is further discussed in Section 2.1.

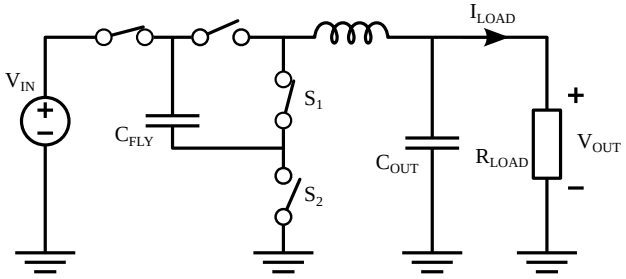


Figure 1.7 – Three-level converter simplified circuit.

1.2.3.3 Other structures

Many other inductive DC-DC converter structures exist such as the Bridge converter, Buck[2], the Watkins-Johnson converter, etc. As the design of such

converters is not the object of this work, they are not presented here. These converters are presented and compared in terms of required passive components in [Wen11c].

1.3 Performance analysis

The objective of this section is to carry out a performance analysis on the various aspects of DC-DC converters, first at the system level, considering the full converter, and then at the component level, i.e. the passive and the active devices. The passive components include the inductors and the capacitors, and the active devices are the switches of the converter. The assembly and packaging technologies are also discussed. Then these considerations are applied to our specifications and pre-design choices are presented.

1.3.1 System view

In this part, the DC-DC converter is seen with several performance metrics as a black box that converts one voltage to another, given a set of specifications. The goal of this high-level analysis is to detect the main trends and trade-offs on DC-DC converters. Before going into the analysis, the scope of the study and the methodology are presented. A discussion on relevant performance metrics is proposed. Then some relevant literature results are further discussed.

1.3.1.1 Scope of the analysis

The performance analysis is carried out on published demonstrators results. Considered demonstrators are integrated inductive DC-DC converters. The review focuses on steady-state performances, conversion efficiency being the main indicator. In order to have comparable converters, the scope of the review has been limited to low input voltage (below 5 V), low output power (below 5 W), high switching frequency (above 10 MHz) non-isolated step-down inductive DC-DC converters, with experimental measurement data. Table 1.1 summarizes the scope of the review.

Table 1.1 – Scope of the review.

	Value	Unit
Number of papers	37	-
Year range	2004 - 2015	-
Frequency range	10 - 660	MHz
Technology node range	22 - 500	nm
Input voltage range	1.1 - 5	V
Output voltage range	0.6 - 3.3	V
Power range	55 - 5000	mW

1.3.1.2 Methodology

The first step is to define metrics that can cover the majority of converters without loosing too much information. Transient aspects have been knowingly excluded from this analysis as transient performances are very dependent on the test conditions. Transient considerations will be discussed later in the manuscript. Thermal aspects are also not considered as the studied DC-DC converters present losses well below 10 W/cm^2 so thermal drain approaches are generally sufficient.

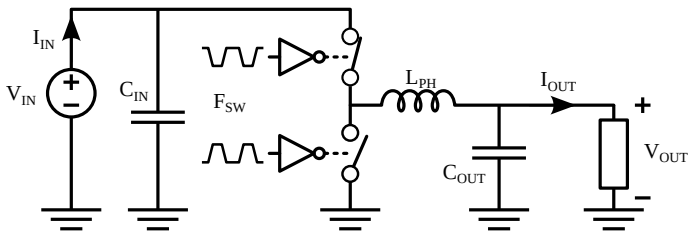


Figure 1.8 – Basic metrics for steady-state evaluation of a buck-type converter.

The discussed fundamental metrics are the followings: the input and output voltages, the input and output currents, the output inductance and capacitance and the switching frequency. Basic metrics are depicted on Figure 1.8. In addition to that, the technology node and the total converter area (when

Table 1.2 – Metrics for the review.

Name	Symbol	Unit	Definition
Efficiency	η	%	P_{OUT}/P_{IN}
Switching frequency	F_{SW}	MHz	-
Technology node	-	nm	-
Input voltage	V_{IN}	V	-
Output voltage	V_{OUT}	V	-
Output current	I_{OUT}	mA	-
Conversion ratio	α	-	V_{OUT}/V_{IN}
Output power	P_{OUT}	mW	$V_{OUT}\times I_{OUT}$
Output capacitance	C_{OUT}	nF	-
Number of phases	N_{PH}	-	-
Phase inductance	L_{PH}	nH	-
Filter corner frequency	F_{LC}	GHz	$1/2\pi\sqrt{L_{PH}C_{OUT}}$

available) are also discussed. Additional metrics can be derived from these elementary metrics, such as conversion ratio, output power, power conversion efficiency or even more intricate indicators such as the Efficiency Enhancement Factor (EEF) defined in [Wen08]. These metrics can be divided into three groups: the functional specifications (input and output voltage, output current and technology node), the performances (efficiency and area) and the design parameters for the rest of the metrics. All the metrics are summarized in Table 1.2.

Once the metrics are identified and extracted from selected publications, they are plotted against each other, allowing one to highlight the possible trends and trade-offs.

1.3.1.3 Landscapes

Figure 1.9 plots for each studied converter its output filter natural frequency (y-axis) versus its switching frequency (x-axis). Dots are parametrized with

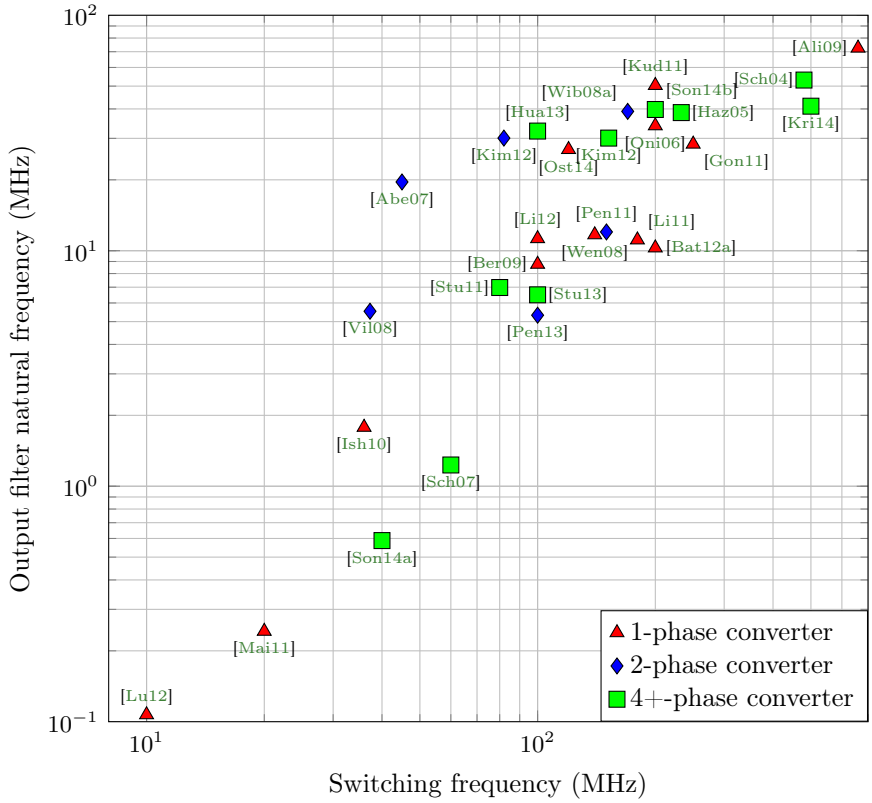


Figure 1.9 – Output filter natural frequency versus switching frequency.

the number of phases of the converter. The plot clearly shows that increasing the switching frequency leads to an increase in the output filter natural frequency, thus reduces the component values of the output filter (output inductance and/or capacitance). Reducing the components values enables to select smaller ones, thus it is a step toward more integration (either in package or monolithically).

However going to a higher switching frequency increases the switching losses, reducing the converter efficiency. This impact is deduced from Figure 1.10, where the efficiency is plotted along with the switching frequency. The dots are parametrized with the conversion ratio. For a given conversion ratio, the efficiency tends to drop when the switching frequency increases.

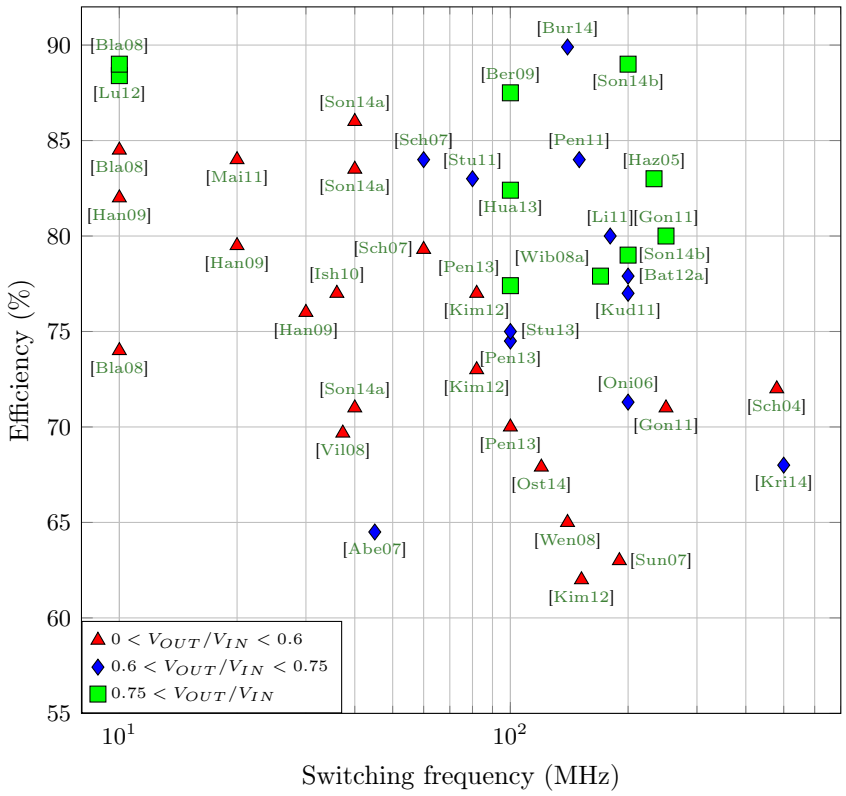


Figure 1.10 – Efficiency versus switching frequency, parametrized with conversion ratio.

Another reading of this plot is the impact of the conversion ratio on the efficiency, at a given switching frequency: converters with lower conversion ratio tend to have a lower efficiency. This trend can be interpreted by evaluating the efficiency gap between the converter and a hypothetical linear converter operating in the same conditions. In a first approximation, the efficiency of a linear converter is equal to the conversion ratio. For a given converter, having a high efficiency will put it further from the linear case if the conversion ratio is small.

In order to be able to compare various converters against one another, it becomes necessary to use a figure of merit taking into account both the

efficiency and the conversion ratio. The EEF calculation (in %) is detailed in Paragraph 1.3.1.4.1.

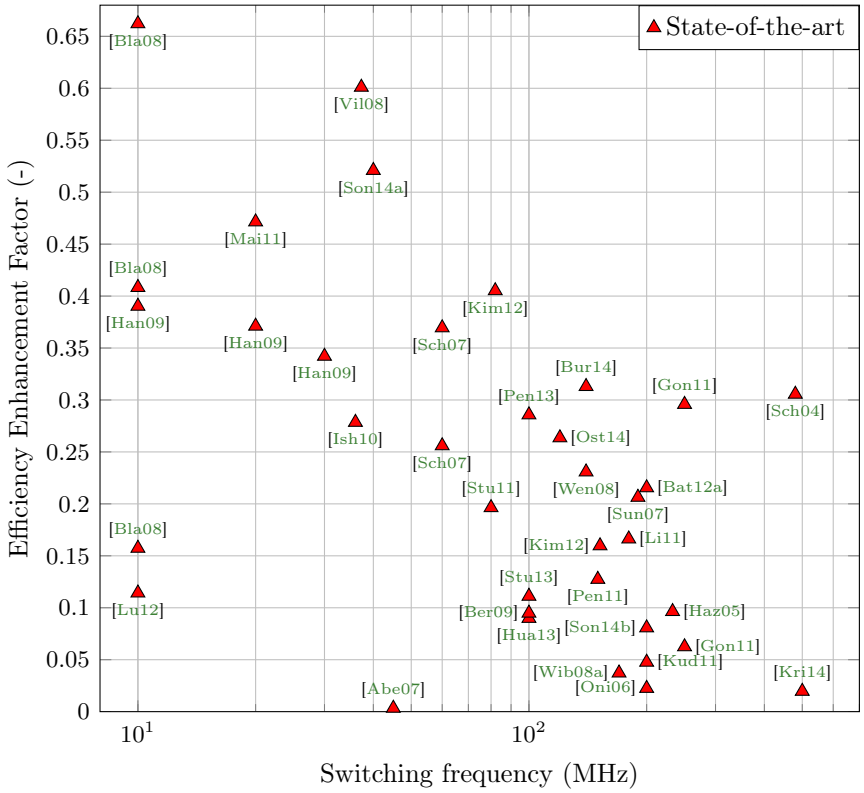


Figure 1.11 – Efficiency Enhancement Factor versus switching frequency.

Figure 1.11 plots the EEF of each converter (calculated according to Equation (1.2)) against the switching frequency. The maximum achieved EEF tends to reduce when the switching frequency increases, confirming the negative impact of switching frequency on conversion performance.

The landscape in Figure 1.12 presents the converter efficiency with respect to the output power. Most of the converters are targeting the 100 to 1000 mW power range. When considering the impact of output power on conversion efficiency, no trend can be identified. This means that output power is not a decisive metric for power efficiency.

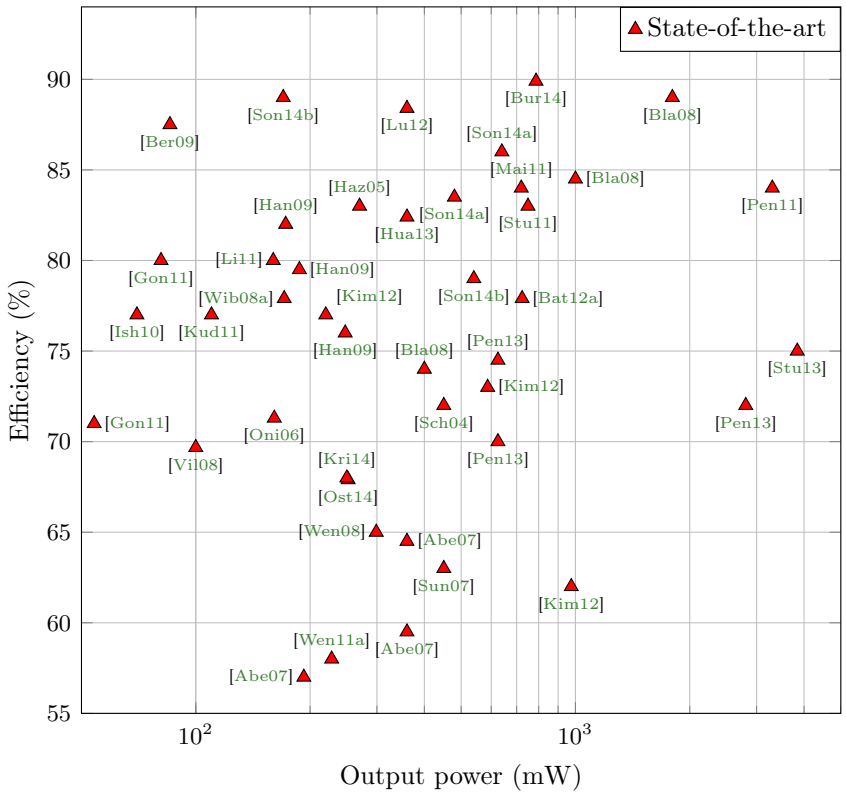


Figure 1.12 – Efficiency versus output power.

When looking at integrated DC-DC converters, a crucial parameter is the manufacturing technology of the active components.

Figure 1.13 and Figure 1.14 illustrate how the technology impacts the converters. Figure 1.13 pictures the efficiency of each converter against its manufacturing technology (active components). The points are parametrized with the switching frequency, as it impacts the efficiency. The global trend is that more advanced technologies enable higher efficiencies. Furthermore the use of more advanced technologies also allows using higher switching frequencies.

However as technology shrinks, converters tends to operate with a lower input voltage. Figure 1.14 plots the input voltage of the converters with respect to their manufacturing technology. There is a noticeable trend that

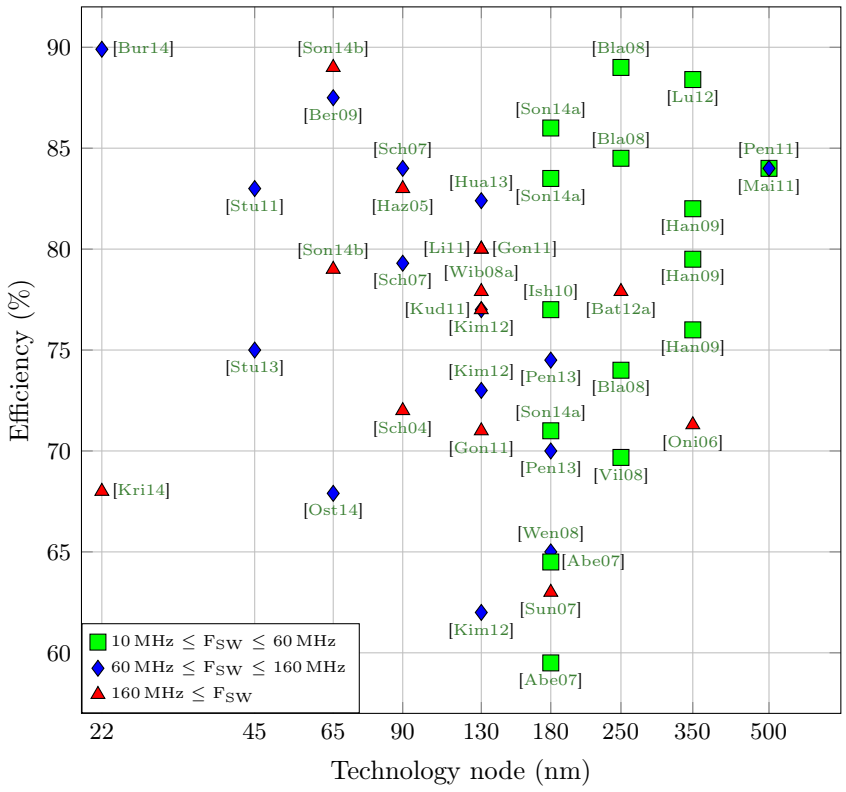


Figure 1.13 – Efficiency versus technology node, parametrized with switching frequency.

the maximum input voltage for each node is decreasing with the shrinking at silicon level. Transistors in advanced technologies have shorter gate length and thinner gate oxide, thus the maximum operating voltage is reduced.

Major design trade-offs appear to be the following: for a given set of specifications (input and output voltages, output power), a high switching frequency is required to reduce the output filter (in terms of components values). If the step-down conversion ratio is small, achieving high efficiency is hard, especially if the switching frequency is really high. However using an advanced technology helps reducing the losses and achieving high efficiency, but challenges arise when the converter input voltage is higher than the nominal technology voltage.

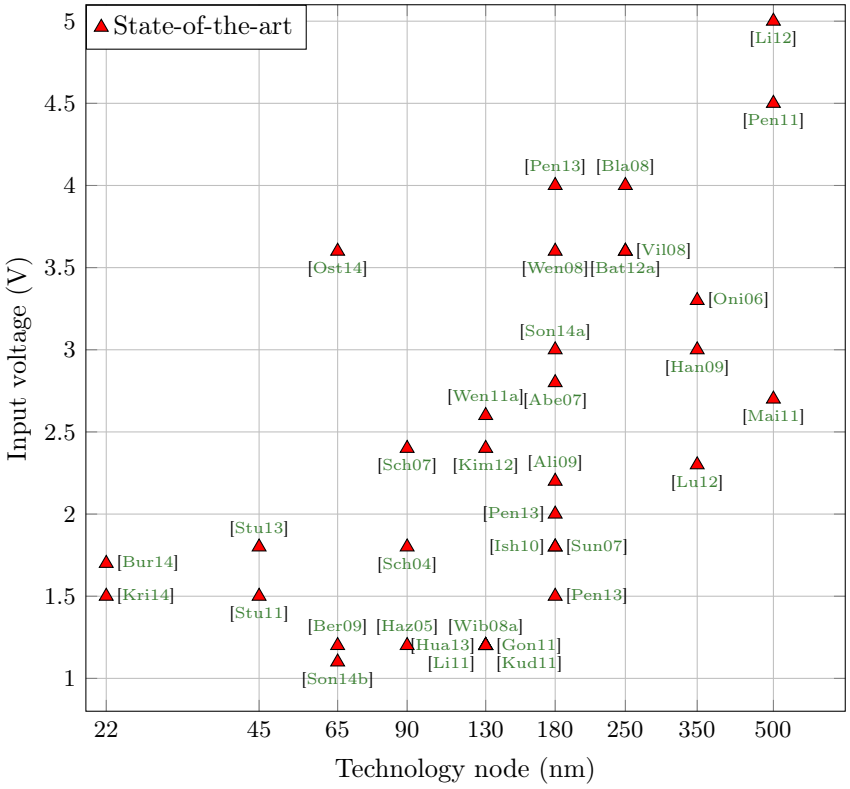


Figure 1.14 – Input voltage versus technology node.

1.3.1.4 Discussion on Figures of Merit

Part 1.3.1.3 has shown that efficiency, while being widely used and easy to understand, might not be the most suitable indicator for comparison of various converters. Efficiency is impacted by many parameters but the most problematic is the conversion ratio. Comparing the efficiency of two converters that don't have the same conversion ratio becomes tricky. It then becomes necessary to use an indicator that combines both the efficiency and the conversion ratio.

1.3.1.4.1 Efficiency Enhancement Factor (EEF) is proposed as a performance metric in [Wen08]. The idea behind this metric is to compare the

performance of the actual converter against an hypothetical linear converter operating in the same conditions – i.e. same input and output voltage, output current and conversion ratio. The conversion ratios of the switching converter and the linear converter are noted k_{SW} and k_{lin} respectively and they are equal. The efficiency of the switching converter is η_{SW}, for the linear converter it is η_{lin}, which is equal to k_{lin} assuming an ideal linear converter. EEF is defined as the input power difference of these two converters (ΔP_{IN}), divided by the input power of the hypothetical linear converter (P_{IN_lin}). The equation is:

$$EEF = \frac{\Delta P_{IN}}{P_{IN\_lin}} = \frac{P_{IN\_lin} - P_{IN\_SW}}{P_{IN\_lin}} = 1 - \frac{\frac{P_{OUT\_SW}}{\eta_{SW}}}{\frac{P_{OUT\_lin}}{\eta_{lin}}}, \tag{1.1}$$

and as $\eta_{lin} = k_{lin} = k_{SW}$ and $P_{OUT\_lin} = P_{OUT\_SW}$, we get

$$EEF = 1 - \frac{k_{SW}}{\eta_{SW}}. \tag{1.2}$$

EEF value is always lower than 1 and is not limited by a minimal low value (the EEF tends to $-\infty$ when the DC-DC converter efficiency tends to 0). A positive EEF means that the switching converter is more efficient than its linear counterpart, and a negative EEF means that it's not.

However, this Figure of Merit (FoM) is limited as it tends to favor the converter with a small conversion ratio. When looking at Equation (1.2), we see that the maximum achievable value depends on the conversion ratio. For instance a converter with a conversion ratio of 0.8 can not have an EEF greater than 0.2. EEF is calculated for efficiency results presented in [Che14] in Table 1.3. For the same converter, EEF can vary quite a lot, depending on which point is studied. Furthermore evaluating the gain of using the studied converter using only the EEF is not straightforward.

1.3.1.4.2 Losses Reduction Factor (LRF) is proposed here to address the shortcomings of the EEF. It is defined as the ratio of the losses of the hypothetical linear converter (as defined in Paragraph 1.3.1.4.1) and the losses

of the actual converter. The LRF calculation details are presented in Equation (1.4).

$$LRF = \frac{P_{IN,lin} - P_{OUT}}{P_{IN,SW} - P_{OUT}} = \frac{\frac{P_{OUT}}{\eta_{lin}} - P_{OUT}}{\frac{P_{OUT}}{\eta_{SW}} - P_{OUT}} = \frac{\frac{1}{\eta_{lin}} - 1}{\frac{1}{\eta_{SW}} - 1} = \frac{\frac{1-\eta_{lin}}{\eta_{lin}}}{\frac{1-\eta_{SW}}{\eta_{SW}}} = \frac{\eta_{SW}}{\eta_{lin}} \cdot \frac{1-\eta_{lin}}{1-\eta_{SW}} \tag{1.3}$$

$$LRF = \frac{\eta_{SW}}{k_{lin}} \cdot \frac{1-k_{lin}}{1-\eta_{SW}} \tag{1.4}$$

LRF can go from 0 (not included) to $+\infty$, and is not limited by conversion ratio. It tends to 0 when the efficiency of the actual DC-DC converter is also close to 0. LRF greater than 1 means the switching converter is doing better than its linear equivalent. The LRF directly tells us by which factor the losses will be cut if the studied DC-DC converter is utilized instead of the linear one. As it is a factor, it needs to be seen in a logarithmic scale. LRF is calculated for efficiency results presented in [Che14] in Table 1.3. It still favors a bit the low conversion ratio points, but as this factor makes sense in a logarithmic scale, it is more fair than EEF for high conversion ratio converter. Nevertheless, it is still hard to compare various converters using LRF as it still favors converters with a small conversion ratio.

1.3.1.4.3 Predicted efficiency Comparing two converters already working in the same conditions would be easy. The idea is that given an operating point efficiency, it would be nice if it were possible to predict the efficiency at another operating point (for instance at another conversion ratio). In order to achieve this, it is necessary to have a look at the loss mechanisms in a DC-DC converter and see what a different conversion ratio would change. We assume that the conversion ratio is modified by varying only the output voltage, i.e. the duty-cycle of the converter. This means that all other relevant values (i.e. input voltage, switching frequency and load current) are considered constant.

In a switching DC-DC converter, there are switching losses and conduction losses. Switching losses depend on switching frequency and input voltage, and conduction losses depend on the Root Mean Square (RMS) current [Gil02]. The RMS value contains two contributors: the load current and the ripple current. In the previously described conditions, only the ripple current depends on the duty cycle. If we suppose that the ripple contribution is relatively small, we deduce that the losses are not going to vary a lot when changing the output voltage, i.e. the conversion ratio. It is then possible to calculate a "predicted" efficiency (η_{pr}) at any given output voltage if the efficiency at one operating point (η_{op}) is available. The "predicted" efficiency estimates the converter efficiency if it were operating at an interpolated output voltage ($V_{OUT,pr}$), delivering the associated output power ($P_{OUT,pr} = V_{OUT,pr} \times I_{OUT}$). η_{pr} is defined in Equation (1.5).

$$\eta_{pr} = \frac{P_{OUT,pr}}{P_{loss} + P_{OUT,pr}} \tag{1.5}$$

Then power and losses are defined as follow, using the reported operating conversion ratio (k_{op}) and the "predicted" output voltage ($V_{OUT,pr}$) and its associated "predicted" conversion ratio (k_{pr}), assuming a constant input voltage:

$$P_{OUT,pr} = \frac{P_{OUT,op}}{V_{OUT,op}} \cdot V_{OUT,pr} \tag{1.6}$$

$$P_{loss} = \frac{P_{OUT,op}}{\eta_{op}} - P_{OUT,op} \tag{1.7}$$

$$\frac{V_{OUT,pr}}{V_{OUT,op}} = \frac{k_{pr}}{k_{op}} \tag{1.8}$$

We can then calculate the value of η_{pr}:

$$\eta_{pr} = \frac{\frac{P_{OUT,op} \cdot V_{OUT,pr}}{V_{OUT,op}}}{\frac{P_{OUT,op}}{\eta_{op}} - P_{OUT,op} + \frac{P_{OUT,op} \cdot V_{OUT,pr}}{V_{OUT,op}}} \tag{1.9}$$

$$\eta_{pr} = \frac{\frac{V_{OUT,pr}}{V_{OUT,op}}}{\frac{1-\eta_{op}}{\eta_{op}} + \frac{V_{OUT,pr}}{V_{OUT,op}}} \tag{1.10}$$

$$\eta_{pr} = \frac{k_{pr}}{k_{op}} \cdot \frac{1}{\frac{1-\eta_{op}}{\eta_{op}} + \frac{k_{pr}}{k_{op}}} \tag{1.11}$$

$$\eta_{pr} = \frac{\eta_{op} \cdot k_{pr}}{k_{op} - \eta_{op}\,(k_{op} - k_{pr})} \tag{1.12}$$

Table 1.3 – EEF, LRF and predicted efficiency calculations on results published in [Che14].

V_{IN}	3.3 V	3.3 V	3.3 V
V_{OUT}	2.4 V	1.8 V	1.2 V
Conversion ratio (k_{op})	0.72727	0.54545	0.36364
Efficiency reported (η_{op})	91.8 %	88.6 %	84.3 %
EEF	0.2078	0.3844	0.5702
LRF	9.614	6.477	4.199
Predicted efficiency (η_{pr}) at 2.4 V output	91.8 %	91.20 %	91.48 %
Predicted efficiency (η_{pr}) at 1.8 V output	89.36 %	88.6 %	88.96 %
Predicted efficiency (η_{pr}) at 1.2 V output	84.84 %	83.82 %	84.3 %

Table 1.3 shows the predicted efficiency values calculated for each reported point. The calculation offers a rather good prediction (less than 1 % error).

Using a predicted efficiency will allow to compare converters together at the same conversion ratio, making it easier to get consistent comparisons.

1.3.1.5 Outstanding state-of-the-art performances

Based on landscapes presented in Part 1.3.1.3, we can see that some data points are standing out the major trends. It is interesting to investigate what made these converters stand out, so these data points are discussed in the following paragraphs.

When looking at the filter frequency, some converters are using very small output filters with respect to their switching frequency. For instance the converter in [Abe07] has a 20 MHz filter corner frequency for a 45 MHz switching frequency. This is because it uses an on-chip inductor (with low inductance density) and hysteretic control to keep ripple relatively low. However achieved efficiency is not very high, only 64 % when converting 2.8 V to 1.8 V. This relatively low efficiency can be explained by the small inductor, making the current ripple high, that results in an important RMS current through the switches.

In terms of efficiency, the converter in [Bur14] shows very good performances. It operates at high frequency (140 MHz) with an significant step-down conversion ratio (0.62) and achieves around 90 % conversion efficiency. It is achieving high efficiency by taking benefit from the 22 nm FinFET CMOS technology performances. The power stage is designed with two Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in series, allowing to use very short length transistor, with thin oxide. In terms of assembly, it is highly integrated. Power inductors are air-core devices (no magnetic losses) embedded in package, and capacitors are on-chip MIM capacitors.

In terms of voltage rating, depicted in Figure 1.14, the converter presented in [Ost14] emerges. It withstands 3.6 V input voltage with a 65 nm bulk CMOS technology. In order to achieve this, it uses two MOSFETs in a cascode configuration as a single switch. The transistors are 2.5 V thick oxide MOSFETs.

The state-of-the-art addresses already some challenges but there are still improvements expected, for instance pushing further the trade-off between efficiency and switching frequency, and reducing the footprint of the passive components which is still a big part of these converters.

1.3.2 Components and technologies

This part presents a performance analysis of each constituent of a typical DC-DC converters, which are the passive components, the active components and the package/assembly. The passive components include the inductors and the capacitors, the active components are the power switches and control elements. The assembly part deals with what is utilized to connect the passive and the active components together, as well as connecting the converter to the rest of the world. This part present several considerations on components and technologies, and choices related to these will be presented in Part 1.4.2.

1.3.2.1 Passive components

Passive components can be either in package or integrated into a substrate. Many packages for passive components are available but they will not be discussed here. Only components in Surface Mounting Device (SMD) package types are considered for commercial devices.

1.3.2.1.1 Discrete inductors and capacitors are sold in SMD package of various sizes, depending on the component value that is inside. For the capacitor, the capacitance value and voltage rating influence the package size. For the inductor, it is the inductance value, its Equivalent Series Resistance (ESR) and if a magnetic material is utilized or not.

The Multi-Layer Ceramic Capacitor (MLCC) is a well known, mainstream component. More than 30 000 MLCCs are produced each second [Ho10]. Capacitors in the range of tens of nanofarads are found in 0402 (1 mm by 0.5 mm) SMD package size. Besides its relatively high capacitance density and low ESR (tens of milliohm), it suffers from a non-negligible Equivalent Series Inductance (ESL), which becomes problematic at high frequency. A typical ESL value is few hundreds of picohenries. Parasitic inductance of MLCC is mainly dictated by its package size [Cai97]. A high parasitic inductance implies a relatively low self-resonant frequency (at a given capacitance value). When looking for high frequency decoupling, this becomes a limiting factor. Figure 1.15 shows the typical impedance curve of a 10 nF MLCC in an 0402 SMD package. A circuit using this device will not benefit from effective decoupling above its resonant frequency (around 60 MHz).

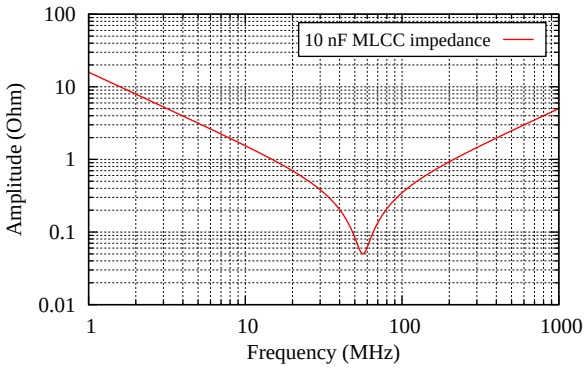


Figure 1.15 – Typical impedance characteristic of a 10 nF SMD MLCC.

Regarding the inductor, there are basically two kinds of devices: the magnetic core inductors and the air-core inductors. Magnetic inductors usually present a better DC performance than air-core devices (higher inductance and lower resistance). However the magnetic material doesn't behave very well at high frequency: AC losses due to the hysteretic losses are becoming prevalent meaning that the inductance value is dropping and equivalent resistance is increasing. Quite evidently, air-core devices don't suffer from magnetic losses, but the inductance density is very low. Both magnetic and air-core inductors are commercially available in SMD packages. The issue with these inductors is that they are not flat. They are basically a copper wire wrapped around a magnetic core for magnetic devices, or just wound as a solenoid for air-core inductors. The number of turns squared is proportional to the inductance, meaning that for each package size, there is a trade-off between inductance value (number of turns), resistance (wire length and diameter) and package size.

1.3.2.1.2 Integrated passive devices are alternatives to discrete passive components. They are manufactured using processes that aim to be co-integrated with active component processes.

There are various capacitor types in integrated technologies. The natural capacitor of a CMOS technology back-end (with a top and bottom metal plate using routing metal layers) is the Metal-Oxide-Metal (MOM) capacitor,

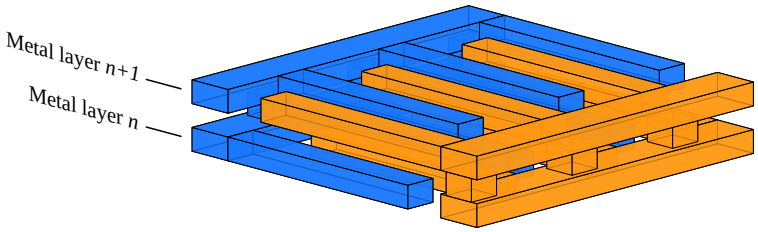


Figure 1.16 – MOM capacitor.

depicted in Figure 1.16 using two metal layers. This capacitor has quite low density but can handle relatively high voltage (depending on the spacing between the metal fingers). Its density is strongly dependent on the number of metal layers used and their thickness and spacing. This capacitor can also be distributed on-chip, reducing the parasitic inductance and resistance, making it suitable for very high frequency operation. One issue with MOM capacitors is that it uses the routing area, so it is impossible to route signal paths were there are MOM capacitors. Because of the low density and the increasing cost of advanced CMOS area, this kind of capacitors can become quite expensive.

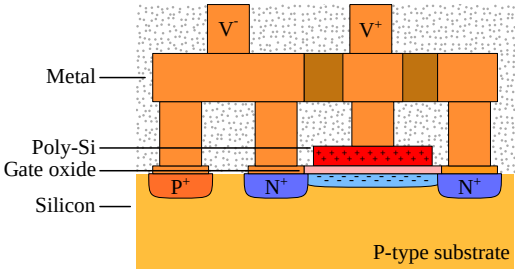


Figure 1.17 – MOS capacitor.

Another capacitor type intrinsically available in CMOS process is the Metal-Oxide-Semiconductor (MOS) capacitor, presented in Figure 1.17. The MOS capacitor basically uses the gate of a MOSFET as a capacitor. The gate is the positive capacitor electrode and the drain, source and bulk (all connected together) are the negative electrodes. In processes using high-K dielectric, density of MOS capacitors is higher than Metal-Oxide-Metal (MOM) capacitors. However voltage handling is the nominal technology voltage rat-

ing, except if thick oxide is available (the density is decreased as the voltage rating increases). One electrode is the silicon, meaning that there is a considerable bottom plate capacitance so this capacitor is not very suitable when a flying capacitor is required. A parasitic capacitor appears, source of losses. Furthermore, these capacitors are known to be non-linear with their applied voltage. Regarding the cost, it is similar to the MOM capacitor: it occupies space where transistors could have been designed, wasting costly area.

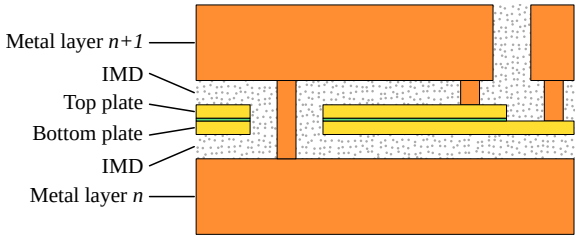


Figure 1.18 – MIM capacitor.

A third alternative for on-chip capacitors are Metal-Insulator-Metal (MIM) capacitors. They are shown in Figure 1.18. They are built with the same principle as MOM capacitors, except that they don't use routing metal layers. The difference is that they use intermediate metal layers which are in between two routing metal layers (generally between thick metal layers as the inter-metal dielectric is thicker there). It shows a better density than MOM capacitors as electrodes are less spaced. It also wastes less routing resources as only one routing layer is utilized. However MIM fabrication requires specific manufactured steps and these capacitors are not available by default in CMOS technologies.

The last capacitor technology discussed here is the deep-trench approach. Capacitors effective area is increased by etching the silicon with an important form-factor, and then a metal/insulator stack is deposited on this surface to create the electrodes as shown in Figure 1.19. These capacitors present the best density for integrated capacitors. They can be manufactured on a dedicated low-cost silicon chip and then assembled in-package with the converter [Lal13]. Fabricating deep-trench capacitors as a back end to a CMOS process is possible, as for instance described in [Cha15], but is very costly.

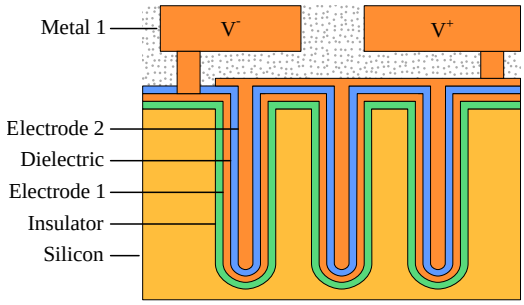


Figure 1.19 – Deep-trench capacitor.

Regarding inductors, it is also possible to go for integrated devices. Air-core inductors are the most natural inductors to be integrated. They are basically made using metal traces but they suffer from poor density, and a relatively high resistance value as the trace is long and thin.

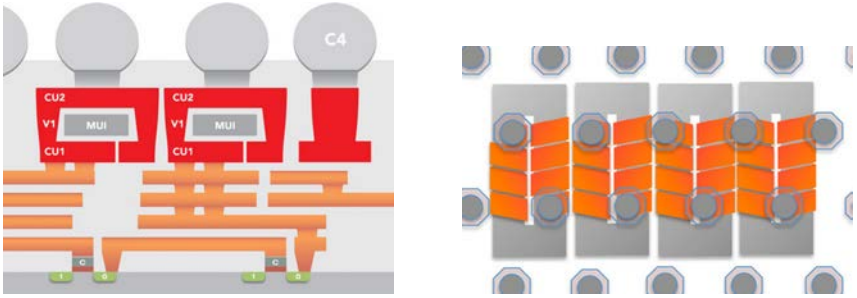


Figure 1.20 – Ferric process (from Ferric Semiconductor website[3]).

It is also possible to go for integrated magnetic core devices, but these are much less available than capacitor technologies. It is possible to use magnetic inductors by depositing magnetic material in CMOS back-end-of-line and creating a solenoid around it. This is what Ferric Semiconductor does [Stu14], proposing an option to the TSMC process. A cross section of the process is depicted in Figure 1.20.

The last discussed integrated inductors are the racetracks inductors. These inductors are also called "elongated spiral" inductors. A track of metal is

[3] http://www.ferricsemi.com/technology/

deposited on a magnetic material and then magnetic material is added in order to close the magnetic loop. Using this kind of integration allows for planar inductors, making an eventual 3D integration easier [Mat05].

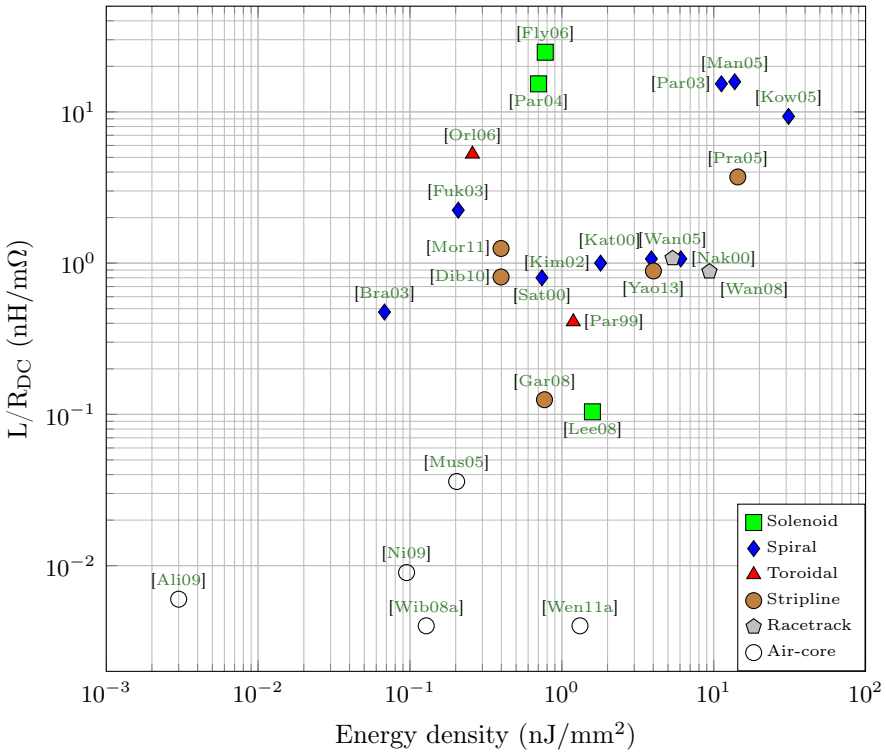


Figure 1.21 – Inductors DC figure of merit.

Figure 1.21 and Figure 1.22 are presenting the landscapes of integrated inductors. Figure 1.21 focuses on DC characteristics (energy density and inductance over resistance). For both metrics a higher value means a better performance. The air-core inductors present a low performance, especially when looking at inductance over resistance. However they present a very good characteristic in AC, as shown in Figure 1.22. Magnetic inductors are limited in frequency. Using magnetic material lamination might help to push the operating frequency of magnetic inductors. More details on integrated inductors can be found in [Mat12].

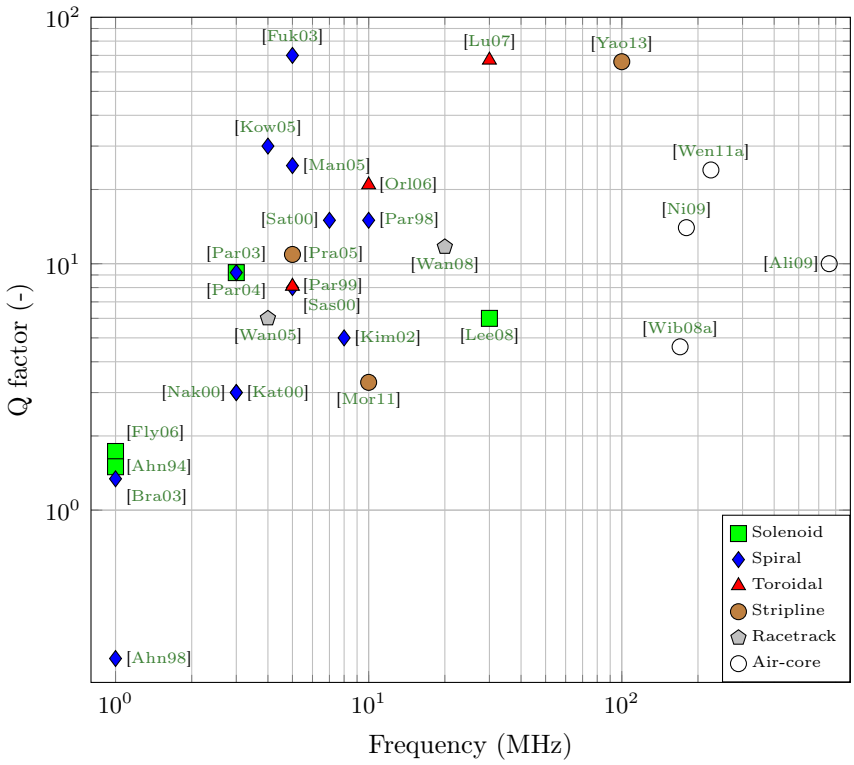


Figure 1.22 – Inductors AC figure of merit.

1.3.2.2 Active components

Many components can act as switches. In term of available technologies to manufacture these switches, the most classical is the CMOS technology using silicon material. Other material are available such as gallium-arsenide, gallium-nitride or silicon-carbide. These materials are showing good properties, allowing for high frequency, high current density and high temperature operation [Tou11]. However they lack the manufacturing facilities and the integration level that silicon already offers. The focus on this section is then only on silicon-based switches.

1.3.2.2.1 Lateral or vertical devices are the two major ways of manufacturing active silicon components. In vertical devices, one electrode of the

switch is at the bottom of the piece of silicon, the other on the top. The current is flowing vertically, making this type of component suitable for high voltage. However these components are not easily integrated with other ones, and are used as discrete transistors. In lateral devices, all connections are on top of the die, and current is flowing laterally. This allows for side by side integration, but power components can present a large area.

1.3.2.2.2 BJT, JFET and MOSFET are the three main types of transistor. These acronyms stand for Bipolar Junction Transistor (BJT), Junction Field-Effect Transistor (JFET) and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). The BJT is the first transistor ever to be made, at Bell Telephone Laboratories, in 1947. BJTs are mainly used for signal handling. For large integration their performance over frequency are higher than the ones of a MOSFET. BJTs are controlled in current, making them subject to non negligible driving losses. JFET and MOSFET behave similarly. The resistance of their channel is modulated by a voltage applied to the gate. For the JFET, the gate is a PN junction in reverse polarization. For the MOSFET, the gate is a capacitor. Both can be good switches, the difference is that the JFET is a normally-on component, and the MOSFET a normally-off component.

In term of component availability, the JFET is usually less present in CMOS processes as it is fabricated as a compatible device and is not a focus device of the technology. It doesn't benefit from scaling as well as the MOSFET, so its usage is mainly reserved for low noise analog circuit.

1.3.2.2.3 Laterally-Diffused MOSFET (LDMOSFET) operates at a more important voltage than a standard MOSFET because it has a laterally diffused drain region. This makes this device very good for high voltage operation, at the expense of an increased on-state resistance. These devices don't come as standard components in CMOS technologies. They are present in BiCMOS technologies, that benefited from extra time on technology development compared to standard CMOS technologies.

1.3.2.3 Packaging and assembly

Assembly and packaging are two crucial steps of manufacturing. In the case of a monolithic integration (all the active and passive components on the same piece of silicon) there is no assembly needed. This is still not the general case. It is necessary to assemble the active components to the passive ones (capacitors and inductors) in a way that the assembly doesn't ruin the performance. An ideal assembly should aim to add no parasitic inductance and capacitance.

There are several assembly techniques that can be used. The most familiar is on PCB, and the placement side-by side of all components, connecting them with the PCB copper traces. While being broadly used, this method suffers from poor interconnections. They are relatively long, so they are adding some inductance, highly unwanted for the decoupling capacitors. Doing the assembly this way also requires already packaged devices, increasing the parasitic elements and also making them larger.

An improvement of the PCB assembly is to embed some components inside the PCB, and put the others on top of them. This technology is commercially available, proposed for instance by AT&S [Pal05]. This offers shorter interconnection than in a simple PCB assembly, and it obviously reduces the area of the full assembly.

Active and passive devices can also be assembled by means of an interposer. Basically an interposer is like a piece of PCB but with much shorter and smaller interconnection capabilities. Furthermore an interposer can also embed some components, for instance capacitors. This makes it very interesting as interconnections are greatly shortened [Lal13].

In terms of packaging, the usual approach is to put the assembly in a discrete package, and then solder it on a PCB – except for the case where the assembly is directly done on PCB. The connection from the assembly to the package is classically done using wire-bonding.

Another possibility is the flip-chipping approach. The IC (or assembly) is flipped and connected to the PCB after balls are deposited. This improves interconnection by reducing the parasitic inductance and resistance. It is possible to go package-less, having the chip (or assembly) directly soldered on the PCB using wire-bonding or flip-chip approach. This approach is promising for high frequency converters.

1.4 Conclusion and design specifications

This section details the specifications of the design target in their context. Based on the specifications and the previously developed considerations it then concludes on pre-design choices. This includes the technologies chosen for design, and some restrictions of the design space.

1.4.1 Specifications of the design target

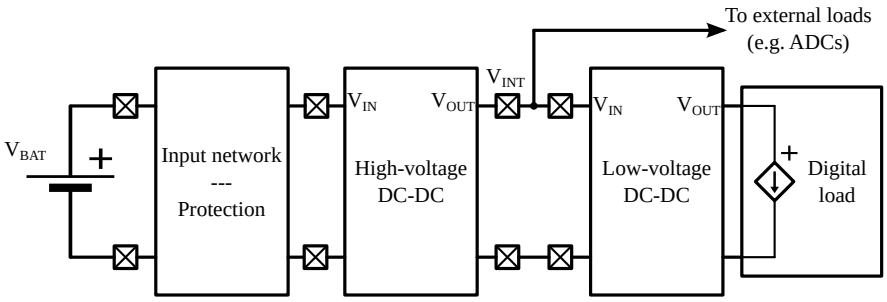


Figure 1.23 – Full system architecture.

The full system architecture is depicted in Figure 1.23. This is a classical automotive system, starting with the battery, and an input network ensuring some protection. The DC-DC conversion from the battery to the digital load is made in two steps. The first DC-DC converter is high voltage. It is designed for an input voltage varying from approximately 6 V to 16 V, and up to 60 V in the case of a load dump. The intermediate voltage (V_{INT}) is then a constant voltage fed to the input voltage of the low voltage converter, and it is also used for other peripherals (such as ADCs). The low voltage converter then generates the output voltage to the digital load, modeled as a current load.

The focus of this work is on the low voltage DC-DC converter. The objective is to integrate it with the digital load, either on chip or in package. The knowledge of the full system is very helpful when designing such a converter. In this case, we know that the input voltage of the converter is not going to vary much during operation as it is already the output of a first converter. This intermediate voltage is defined at 3.3 V. This voltage is not optimized, strictly speaking, as this work focuses only on the low voltage converter. The

proper value of the intermediate voltage would come from a system level analysis (Figure 1.23). A recent study seems to propose a similar value [Aul15].

Table 1.4 – Specifications of the target converter.

Name	Min	Typ.	Max	Unit
V_{IN}	3.0	3.3	3.6	V
V_{OUT}	-	1.2	-	V
I_{LOAD}	50	280	500	mA
I_{SLEEP}	-	15	-	mA
$I_{STANDBY}$	-	150	-	µA
I_{JUMP}	-	50	-	mA
T_{JUMP}	-	2	-	ns
Static voltage accuracy	−2.5	-	+2.5	%
Dynamic voltage accuracy	−6	-	+6	%
Efficiency at $I_{LOAD,TYP}$	90	-	-	%
Efficiency at $I_{LOAD,MIN}$	80	-	-	%
Efficiency at I_{SLEEP}	70	-	-	%
F_{SW}	100	-	-	MHz
Ambient temperature	−40	55	125	°C
Package height	-	1.2	4	mm
Total area	-	-	10	mm^2
Technology platform	40 nm bulk CMOS			

The major specifications of the low voltage converter are summarized in Table 1.4. Passive components values are knowingly omitted as they are subsequent to the first design choices, presented in Section 2.4. The major concern is on the efficiency in a first step. As seen in Part 1.3.1.3, it is very difficult to achieve high efficiency at high frequency and with a significant step-down conversion ratio (here V_{OUT}/V_{IN} is equal to 0.36). In addition to the efficiency challenge, the goal is also to obtain a converter with a volume as small

as possible. Regarding the selected technology (40 nm CMOS), as the ultimate goal is the integration with the digital load, it is mandatory to use the same CMOS technology for both the converter and the digital load. This limits the available devices to those available in the chosen technology, reducing the optimization space. Dynamic requirements are not very challenging as no specific reference transient performances have been specified so far. The focus will be on good static accuracy, and low voltage overshoot or droop during load transient. Expected load jumps are not critical (25 A/µs).

1.4.2 Technology portfolio

In order to design the converter, some technologies have been chosen based on considerations developed in Part 1.3.2. Available switching devices are classical P-MOSFET and N-MOSFET as of 40 nm bulk CMOS process.

For the passive components, classical SMD MLCC are clearly not suitable for the design target. They suffer from too low Self-Resonant Frequency (SRF), making them impractical for very high frequency operation (+100 MHz from Table 1.4). Regarding integrated capacitor structures, the CMOS C40 technology doesn't include MIM capacitors. MOM and MOS capacitors are available but they are showing a far too low density (approximately 2 nF/mm^2 for both types). Using these capacitors would require too much area and would be very expensive in silicon area. Even assuming that MIM capacitors are available, their density (approximately 10 nF/mm^2 according to the ITRS 2012 report [ITR12]) is still not sufficient for the application (only 100 nF would fit on 10 mm^2, leaving no room for the inductor). Even the sum of all available on-chip capacitors would theoretically be far from being sufficient. Capacitor technology suitable for the application is then the trench capacitors. They are showing a good density (200 nF/mm^2) and can be optimized for high frequency operation. An heterogeneous approach is selected for the converter: CMOS C40 for active devices and separate deep-trench capacitors.

It naturally comes the necessity to use an interposer that connects the capacitors to the IC. For the sake of simplification this interposer should embed the capacitors and provide some metal routing for interconnection purposes. Fortunately the selected technology allows for micro-bumping and flip-chipping.

On the inductor side, a choice needs to be made between air-core or magnetic devices. When looking at the air-core DC performance, the best reported result in term of inductance over resistance is the one presented in [Mus05]: approximately 0.04 nH/mΩ. This implies that for a 30 nH inductor, the DC resistance would be 750 mΩ. At nominal load operating condition (280 mA, 1.2 V output voltage, 336 mW output power) DC inductor resistive losses would be equal to 58.8 mW. Efficiency considering only inductor losses would be equal to 85.1 %, which is already well below the targeted efficiency. For this reason, the chosen inductors family is the magnetic one, in order to get a low ESR value. The goal is then to push further the frequency limits of the magnetic components.

In terms of structure, the interest is on racetrack inductors, allowing for planar integration, and even a possible co-design on the capacitive interposer by depositing copper and magnetic material on top of it. Such a design could greatly reduce the total area of the full converter as active and passive areas are overlapping.

1.4.3 Technology suppliers

The suppliers of the CMOS technology are Global Foundries and Infineon. Global Foundries will manufacture the CMOS chip, and then dicing and microbumping are realized by Infineon. Trench capacitors on interposer will be provided by IPDiA. This company also does the flip-chip assembly of the IC on top of the interposer [Lal13]. Racetrack magnetic inductors will be designed by Tyndall. They are targeting high frequency operation using thin layer of magnetic material [Wan05].

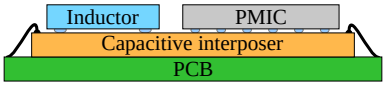


Figure 1.24 – Full system assembled and connected to PCB.

A representation of the assembly of the full system is depicted in Figure 1.24. The converter, or Power Module IC (PMIC), is soldered to the interposer as well as the inductors and the assembly will be wire-bonded on a PCB for input/output connections.

Chapter 2

Design methodology

Contents

This chapter presents the analyses carried out prior to the actual design of the converter. This includes a high-level study on the converter architecture, modeling of the losses of the active components and dimensioning of the output filter. Some considerations about control strategies are also presented. The analysis of the architecture is performed using analytical equations and high-level simulation. Switches' performances are evaluated through simulation and

then models are imported into architecture models. These analyses are then concluded by various design targets along with their respective objectives.

2.1 Architecture definition

This section details the high-level analysis of several DC-DC converter architectures. Considered architecture are the classical non-isolated synchronous buck converter, the two-phase buck converter, the two-phase buck converter with coupled inductors and the three-level converter. The methodology employed for the analysis is the following: waveforms and equations are determined assuming all components are ideal (no parasitic elements) and then parasitic components are introduced and losses are computed using previously established equations. This methodology is valid as long as the parasitic elements do not contribute a lot, i.e. the efficiency of the converter is relatively unaffected. In order to validate the analytical models, architectures are simulated and results are compared with the results of analytical equations.

2.1.1 Waveforms and equations

All architectures are evaluated assuming the following conditions: input current (I_{IN}) is constant due to large parasitic inductor (L_{PAR}), capacitors are sufficiently large to have a constant voltage across their terminals, switches are considered as ideal (no on-state resistance and switching losses), dead-time is reduced to 0 and the load is a constant current source.

In order to develop circuit equations, the Equivalent Series Inductance (ESL) of the capacitors is omitted. The inductors losses are modeled only using an Equivalent Series Resistance (ESR) which is constant with frequency.

The steady-state equations are derived assuming a constant input and output voltage and the impact of the parasitic resistors on the waveforms is neglected. The converter efficiency is assumed to tend to 100 %, giving the following relations (where α is the duty cycle):

$$V_{OUT} = \alpha \times V_{IN} \tag{2.1}$$

$$I_{IN} = \alpha \times I_{OUT} \tag{2.2}$$

2.1.1.1 One-phase buck converter

The architecture is depicted in Figure 2.1. The parasitic inductance L_{PAR} is supposed to be large enough to have the input current I_{IN} constant, i.e. with a negligible ripple value. The switches S_1 and S_2 are complementarily driven (i.e. 180° phase shift).

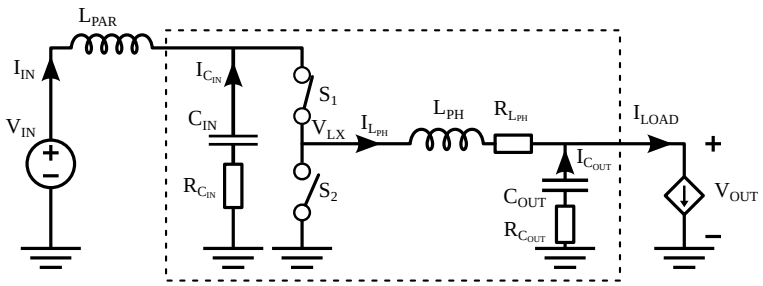


Figure 2.1 – 1-phase buck converter with main parasitic elements of passive components.

Voltage and current waveforms of a one-phase buck converter are presented for a duty cycle below 0.5 in Figure 2.2. The average current through the inductor is equal to the load current. For the input and the output capacitors the average current through them is null as steady-state operation is considered.

2.1.1.1.1 Inductor During the time between 0 and αT, the high-side switch is closed (on), and the low side switch is opened (off). The voltage across the inductor is then $V_{IN} - V_{OUT}$. Analytical equations and waveforms are presented for Continuous Conduction Mode (CCM). The current increase through the inductor is calculated with:

$$\begin{aligned} V_{IN} - V_{OUT} &= L_{PH} \times \frac{\mathrm{d}I_{L_{PH}}}{\mathrm{d}t} \\ V_{IN} - \alpha \times V_{IN} &= L_{PH} \times \frac{\Delta I^{+}_{L_{PH}}}{\Delta t} \\ \Delta I^{+}_{L_{PH}} &= \alpha\,(1-\alpha)\,\frac{V_{IN} \times T}{L_{PH}} \end{aligned} \tag{2.3}$$

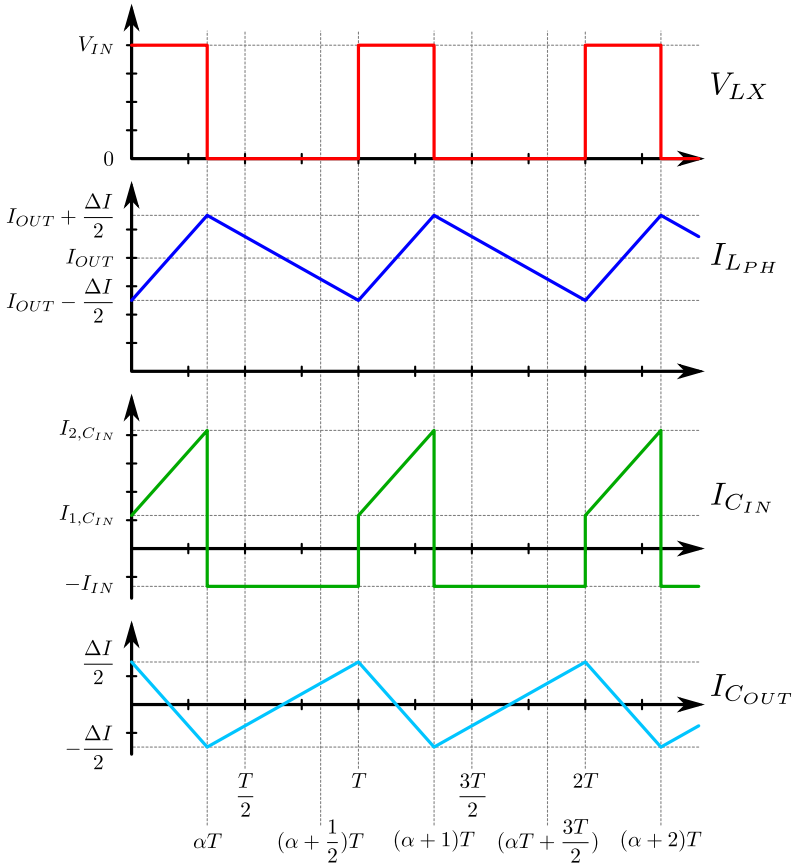


Figure 2.2 – Current and voltage waveforms for an ideal 1-phase buck converter in CCM.

Using the same method, the current decrease during low-side switch conduction is:

$$\begin{aligned} 0 - V_{OUT} &= L_{PH} \times \frac{\mathrm{d}I_{L_{PH}}}{\mathrm{d}t} \\ -\alpha \times V_{IN} &= L_{PH} \times \frac{\Delta I^{-}_{L_{PH}}}{\Delta t} \\ \Delta I^{-}_{L_{PH}} &= -\alpha\,(1-\alpha)\,\frac{V_{IN} \times T}{L_{PH}} \end{aligned} \tag{2.4}$$

As expected, $\Delta I^{+}_{L_{PH}} + \Delta I^{-}_{L_{PH}} = 0$.

The RMS current through the inductor can now be evaluated:

$$I^2_{RMS\_L_{PH}} = I^2_{OUT} + \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.5}$$

2.1.1.1.2 Output capacitor The current through the output capacitor for a one-phase buck converter is only the AC component of the inductor current.

$$I_{C_{OUT}} = I_{OUT} - I_{L_{PH}} \tag{2.6}$$

The RMS current through the output capacitor is then:

$$I^2_{RMS\_C_{OUT}} = \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.7}$$

2.1.1.1.3 Input capacitor The current through the input capacitor is equal to the input current during low-side switch conduction (S_2 closed). During high-side switch conduction (S_1 closed), the current through the input capacitor is the inductor current minus the input current. This gives the values of $I_{1,C_{IN}}$ and $I_{2,C_{IN}}$ (from Figure 2.2):

$$I_{1,C_{IN}} = I_{OUT} - \frac{\Delta I^2_{L_{PH}}}{2} - I_{IN} \tag{2.8}$$

$$I_{2,C_{IN}} = I_{OUT} + \frac{\Delta I^2_{L_{PH}}}{2} - I_{IN} \tag{2.9}$$

The RMS current through the input capacitor for a 1-phase buck is:

$$I^2_{RMS\_C_{IN}} = \alpha \left(I_{IN} - I_{OUT}\right)^2 + (1-\alpha)\, I^2_{IN} + \alpha \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.10}$$

Equation (2.10) can then be simplified using Equation (2.2). This leads to:

$$I^2_{RMS\_C_{IN}} = \alpha\,(1-\alpha)\, I^2_{OUT} + \alpha \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.11}$$

2.1.1.1.4 Losses Passive component losses in a 1-phase buck converter can be evaluated, taking into account the ESRs of input and output capacitors and the ESR of the inductor.

$$P_{PAS\_1ph} = R_{L_{PH}} I^2_{RMS\_L_{PH}} + R_{C_{OUT}} I^2_{RMS\_C_{OUT}} + R_{C_{IN}} I^2_{RMS\_C_{IN}} \quad (2.12)$$

Each term in Equation (2.12) can be calculated using Equation (2.5), Equation (2.7) and Equation (2.11):

$$R_{L_{PH}} I^2_{RMS\_L_{PH}} = R_{L_{PH}} \left(I^2_{OUT} + \frac{\Delta I^2_{L_{PH}}}{12} \right) \quad (2.13)$$

$$R_{C_{OUT}} I^2_{RMS\_C_{OUT}} = R_{C_{OUT}} \frac{\Delta I^2_{L_{PH}}}{12} \quad (2.14)$$

$$R_{C_{IN}} I^2_{RMS\_C_{IN}} = R_{C_{IN}} \left(\alpha \left(1-\alpha\right) I^2_{OUT} + \alpha \frac{\Delta I^2_{L_{PH}}}{12} \right) \quad (2.15)$$

$$\begin{aligned} P_{PAS\_1ph} = & \frac{\Delta I^2_{L_{PH}}}{12} \left(\alpha R_{C_{IN}} + R_{C_{OUT}} + R_{L_{PH}}\right) \\ & + I^2_{OUT} \left(\alpha \left(1-\alpha\right) R_{C_{IN}} + R_{L_{PH}}\right) \end{aligned} \quad (2.16)$$

Equation (2.16) shows that losses in a 1-phase buck converter depend on two major metrics: the phase current ripple and the output current. The phase current ripple is defined Equation (2.3), and depends on switching frequency, inductance value and input voltage. When considering only passive components' losses, a higher switching frequency helps reducing losses.

2.1.1.2 Two-phase converter

The architecture is depicted in Figure 2.3. This converter is basically a combination of two one-phase buck converters sharing the same input and output capacitors, and switching at the same frequency but in opposite phase (180° phase shift). Phase inductors are considered identical. Voltage and current waveforms are presented in Figure 2.4. Equations and waveforms are classically developed here for a duty cycle below 0.5 ($\alpha \leq 0.5$).

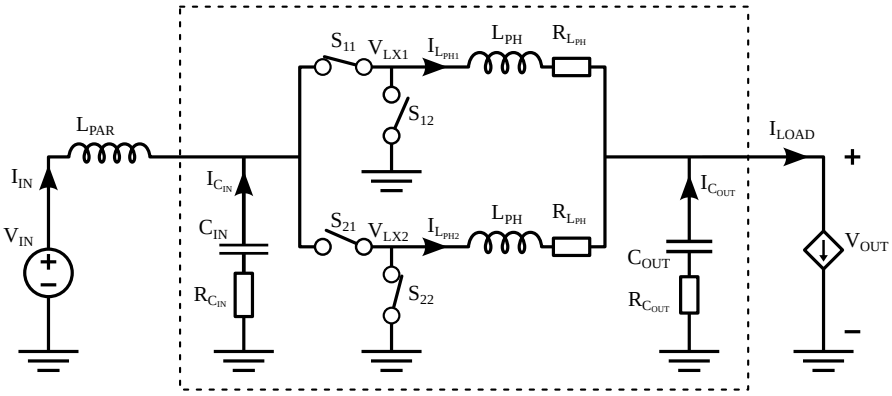


Figure 2.3 – Two-phase buck converter with main parasitic elements of passive components.

2.1.1.2.1 Inductor In a two-phase buck converter, the current phase ripple is the same as the one in the one-phase buck converter, defined by Equation (2.3). The average current is half of the load current as it is shared between the two phases. Thus the RMS current per phase can be expressed using:

$$I^2_{RMS\_L_{PH}} = \frac{I^2_{OUT}}{4} + \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.17}$$

2.1.1.2.2 Output capacitor The output capacitor is submitted to the sum of the two phase currents minus the load current. This means that the current through the output capacitor is the sum of the AC value of both phase currents. The maximum current value is reached when either one of $I_{L_{PH1}}$ or $I_{L_{PH2}}$ is at its peak value, and conversely, the current drops to a minimum when either $I_{L_{PH1}}$ or $I_{L_{PH2}}$ is at minimum value. The ripple current seen by the output inductor is then:

$$\Delta I_{C_{OUT}} = \frac{(1-2\alpha)}{(1-\alpha)} \Delta I_{L_{PH}} \tag{2.18}$$

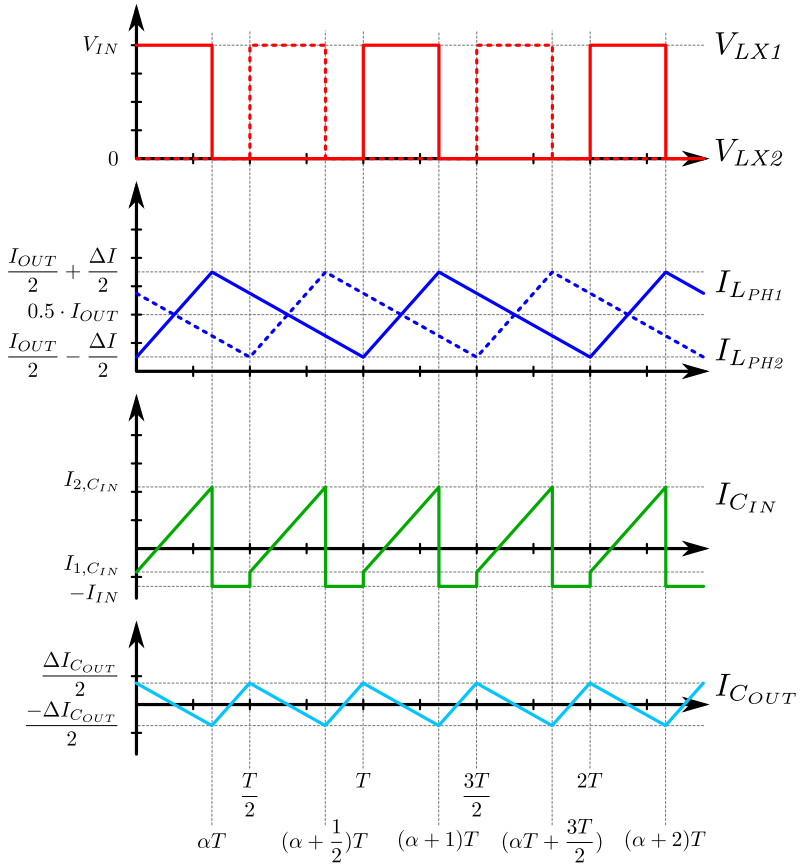


Figure 2.4 – Current and voltage waveforms for an ideal two-phase buck converter in CCM.

This leads to the RMS current:

$$I^2_{RMS\_C_{OUT}} = \frac{(1-2\alpha)^2}{(1-\alpha)^2}\frac{\Delta I^2_{L_{PH}}}{12} \tag{2.19}$$

Compared to a one phase buck converter (Equation (2.7)), this RMS current is always smaller. This implies that passives components' losses are smaller and required output capacitance value can be smaller in a two-phase configuration.

2.1.1.2.3 Input capacitor The current through the input capacitor is defined as a piecewise waveform for one switching period (for $\alpha \leq 0.5$).

$$I_{C_{IN}}(t) = \begin{cases} I_{L_{PH1}}(t) - I_{IN}, & \text{for } t \in [0, \alpha T] \\ -I_{IN}, & \text{for } t \in [\alpha T, \frac{T}{2}] \\ I_{L_{PH2}}(t) - I_{IN}, & \text{for } t \in [\frac{T}{2}, \frac{T}{2} + \alpha T] \\ -I_{IN}, & \text{for } t \in [\frac{T}{2} + \alpha T, T] \end{cases} \tag{2.20}$$

As $I_{L_{PH1}}(t) = I_{L_{PH1}}(t + {}^{T}/_{2})$, only definition between 0 and ${}^{T}/_{2}$ is sufficient for RMS current evaluation. The RMS current through the input capacitor is then:

$$I^2_{RMS\_C_{IN}} = 2\alpha \left(\alpha I_{OUT} - \frac{I_{OUT}}{2} \right)^2 + (1 - 2\alpha) I^2_{IN} + 2\alpha \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.21}$$

This simplifies into:

$$I^2_{RMS\_C_{IN}} = \alpha (1 - 2\alpha) \frac{I^2_{OUT}}{2} + 2\alpha \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.22}$$

2.1.1.2.4 Losses Similar to Equation (2.12), losses in a 2-phase buck converter are then:

$$\begin{aligned} P_{PAS\_2ph} = & \frac{\Delta I^2_{L_{PH}}}{12} \left(2\alpha R_{C_{IN}} + \frac{(1 - 2\alpha)^2}{(1 - \alpha)^2} R_{C_{OUT}} + 2R_{L_{PH}} \right) \\ & + I^2_{OUT} \left(\alpha (0.5 - \alpha) R_{C_{IN}} + 0.5 R_{L_{PH}} \right) \end{aligned} \tag{2.23}$$

Using Equation (2.16) and Equation (2.23) it is possible to calculate the gain in losses when going from a 1-phase to a 2-phase buck converter. It comes:

$$P_{gain} = P_{PAS\_1ph} - P_{PAS\_2ph} \tag{2.24}$$

$$\begin{aligned} P_{gain} = & I^2_{OUT} (0.5\alpha R_{C_{IN}} + 0.5 R_{L_{PH}}) \\ & + \frac{\Delta I^2_{L_{PH}}}{12} \left(-\alpha R_{C_{IN}} + \frac{\alpha (2 - 3\alpha)}{(1 - \alpha)^2} R_{C_{OUT}} - R_{L_{PH}} \right) \end{aligned} \tag{2.25}$$

Equation (2.25) shows that some losses' terms are decreasing while some others are increasing. However even with a negligible $R_{C_{OUT}}$, P_{gain} is positive until $\Delta I_{L_{PH}}$ reaches $\sqrt{6}\cdot I_{OUT}$, a condition that is never satisfied in continuous conduction mode (at the limit, $\Delta I_{L_{PH}}$ is equal to $2 \cdot I_{OUT}$).

2.1.1.3 Coupled two-phase converter

A two-phase converter with coupled inductors is a similar structure as an uncoupled two-phase converter (depicted in Figure 2.3), except that inductors are coupled with a coupling factor k. Phases are still at 180° phase shift. Figure 2.5 depicts the current and voltage waveforms for a coupled two-phase buck converter.

2.1.1.3.1 Inductors The currents through the coupled inductors are defined with the following system:

$$\begin{cases} V_{LX1} - V_{OUT} &= L_{PH1} \times \dfrac{\mathrm{d}I_{L_{PH1}}}{\mathrm{d}t} + k\sqrt{L_{PH1}L_{PH2}} \times \dfrac{\mathrm{d}I_{L_{PH2}}}{\mathrm{d}t} \\ V_{LX2} - V_{OUT} &= L_{PH2} \times \dfrac{\mathrm{d}I_{L_{PH2}}}{\mathrm{d}t} + k\sqrt{L_{PH1}L_{PH2}} \times \dfrac{\mathrm{d}I_{L_{PH1}}}{\mathrm{d}t} \end{cases} \tag{2.26}$$

Solving this system after linearization gives the current variation during the four different operating phases of a switching cycle ($0 \leq t \leq \alpha T$, $\alpha T \leq t \leq T/2$, $T/2 \leq t \leq (0.5+\alpha)T$ and $(0.5+\alpha)T \leq t \leq T$, assuming $\alpha \leq 0.5$ and $L_{PH1} = L_{PH2} = L_{PH}$). Thanks to the symmetrical architecture, calculation of current variation is then simplified.

- $0 \leq t \leq \alpha T$:

$$\begin{cases} \Delta I_{L_{PH1,t1}} &= \dfrac{\alpha\,(1-\alpha\,(1-k))}{1-k^2}\dfrac{V_{IN}\times T}{L_{PH}} \\ \Delta I_{L_{PH2,t1}} &= \dfrac{-\alpha\,(k+\alpha\,(1-k))}{1-k^2}\dfrac{V_{IN}\times T}{L_{PH}} \end{cases} \tag{2.27}$$

- $\alpha T \leq t \leq T/2$ and $(0.5+\alpha)T \leq t \leq T$:

$$\Delta I_{L_{PH1,t2-t4}} = \Delta I_{L_{PH2,t2-t4}} = \frac{-\alpha\,(0.5-\alpha)}{1+k}\frac{V_{IN}\times T}{L_{PH}} \tag{2.28}$$

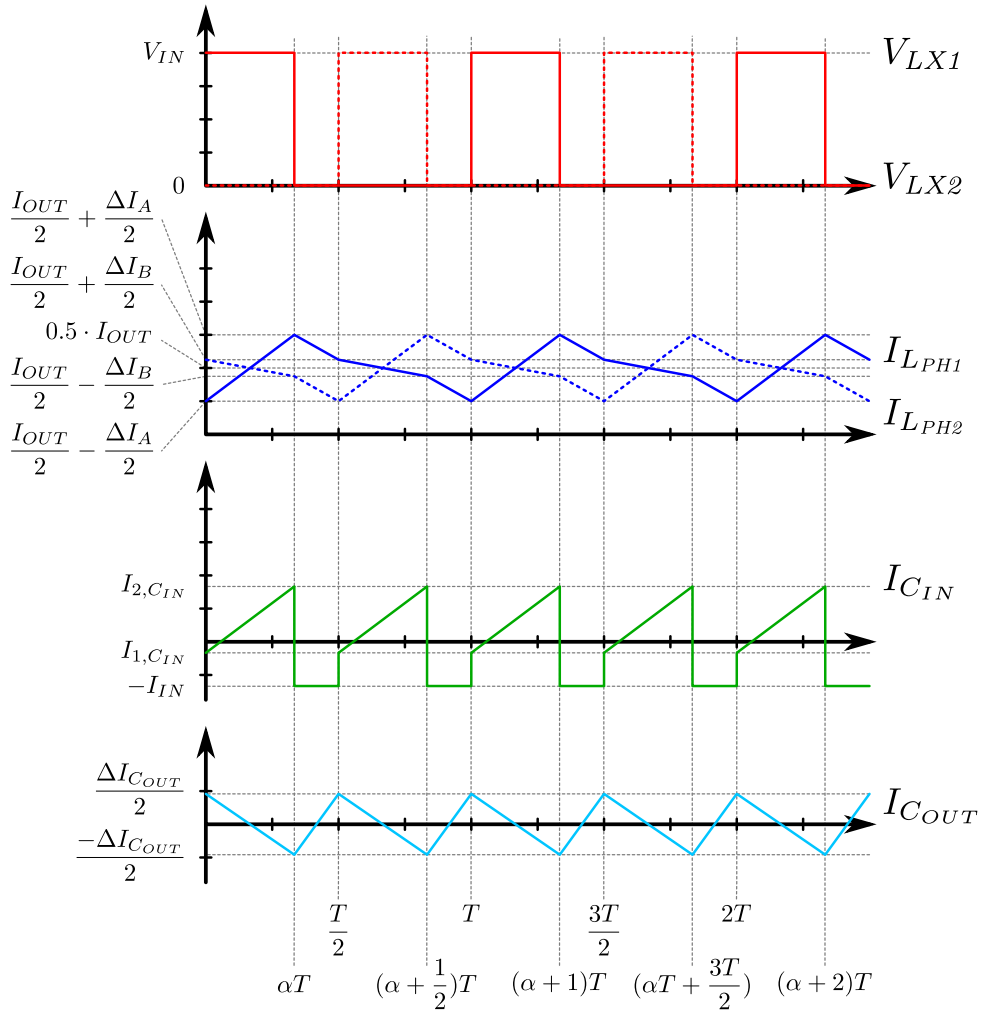


Figure 2.5 – Current and voltage waveforms of an ideal coupled two-phase buck converter in CCM.

- $T/2 \leq t \leq (0.5+\alpha)\,T$:

$$\begin{cases} \Delta I_{L_{PH1,t3}} & = \Delta I_{L_{PH2,t1}} \\ \Delta I_{L_{PH2,t3}} & = \Delta I_{L_{PH1,t1}} \end{cases} \tag{2.29}$$

We end up with a current waveform with three different slopes, as shown

in Figure 2.5. Notable current values are the followings (noted ΔI_A and ΔI_B):

$$\Delta I_A = \frac{\alpha\left(1-\alpha\left(1-k\right)\right)}{1-k^2}\frac{V_{IN}\times T}{L_{PH}} \tag{2.30}$$

$$\Delta I_B = \frac{-\alpha\left(k+\alpha\left(1-k\right)\right)}{1-k^2}\frac{V_{IN}\times T}{L_{PH}} \tag{2.31}$$

The optimum coupling factor that minimizes the total current ripple (ΔI_A) is:

$$k_{opt} = \frac{\sqrt{1-2\alpha}+\alpha-1}{\alpha} \tag{2.32}$$

The RMS current through the phase inductor is then:

$$\begin{aligned} I^2_{RMS\_L_{PHx}} = {} & \alpha\left(\frac{I^2_{OUT}}{4}+\frac{\Delta I^2_{L_{PH1,t1}}}{12}\right)+ \\ & (0.5-\alpha)\left(\left(\frac{\alpha V_{IN}T}{4\left(1-k\right)L_{PH}}+\frac{I_{OUT}}{2}\right)^2+\frac{\Delta I^2_{L_{PH1,t2}}}{12}\right) \\ & +\alpha\left(\frac{I^2_{OUT}}{4}+\frac{\Delta I^2_{L_{PH1,t3}}}{12}\right)+ \\ & (0.5-\alpha)\left(\left(\frac{-\alpha V_{IN}T}{4\left(1-k\right)L_{PH}}+\frac{I_{OUT}}{2}\right)^2+\frac{\Delta I^2_{L_{PH1,t4}}}{12}\right) \end{aligned} \tag{2.33}$$

Equation (2.33) simplifies to:

$$\begin{aligned} I^2_{RMS\_L_{PHx}} = {} & \frac{I^2_{OUT}}{4}+\alpha\frac{\Delta I^2_A}{12}+\alpha\frac{\Delta I^2_B}{12}+ \\ & (1-2\alpha)\left(\frac{\left(\Delta I_A-\Delta I_B\right)^2}{48}+\left(\frac{\alpha V_{IN}T}{4\left(1-k\right)L_{PH}}\right)^2\right) \end{aligned} \tag{2.34}$$

2.1.1.3.2 Output capacitor Output capacitor current ripple can be evaluated using phase current values when the slope is changing. We have:

$$\begin{aligned}\Delta I_{C_{OUT}} &= \Delta I_A - \Delta I_B \\ &= \frac{-\alpha\,(1-2\alpha)}{1+k}\frac{V_{IN}\times T}{L_{PH}}\end{aligned} \tag{2.35}$$

As output capacitor current is a triangular waveform, RMS current is evaluated with:

$$I^2_{RMS\_C_{OUT}} = \frac{\Delta I^2_{C_{OUT}}}{12} \tag{2.36}$$

2.1.1.3.3 Input capacitor Current through the input capacitor in a coupled two-phase buck is evaluated the same way as in an uncoupled two-phase buck converter.

$$I^2_{RMS\_C_{IN}} = 2\alpha\left(I_{IN} - \frac{I_{OUT}}{2}\right)^2 + (1-2\alpha)\,I^2_{IN} + 2\alpha\frac{\Delta I^2_A}{12} \tag{2.37}$$

2.1.1.3.4 Losses Passive components losses of a coupled two-phase coupled buck are calculated as

$$\begin{aligned}P_{PAS\_2ph-cpl} = {} & R_{C_{IN}} I^2_{RMS\_C_{IN}} + R_{C_{OUT}} I^2_{RMS\_C_{OUT}} \\ & + 2R_{L_{PH}} I^2_{RMS\_L_{PH}}\end{aligned} \tag{2.38}$$

When comparing losses for a converter with an optimum coupling factor (calculated using Equation (2.32)) against the losses of a non-coupled two-phase converter (Equation (2.23)), coupling is better. This is because at optimum coupling, current ripple is always smaller than in an uncoupled 2-phase converter, thus all RMS currents are smaller.

2.1.1.4 Three-level converter

Figure 2.6 presents the circuit of an ideal three-level converter. Switches S_1 and S_4 are complementary controlled, as well as S_2 and S_3. Capacitor C_{FLY} is charged at $V_{IN}/2$ in steady-state. For a duty cycle below 0.5, the switching sequence is as follow:

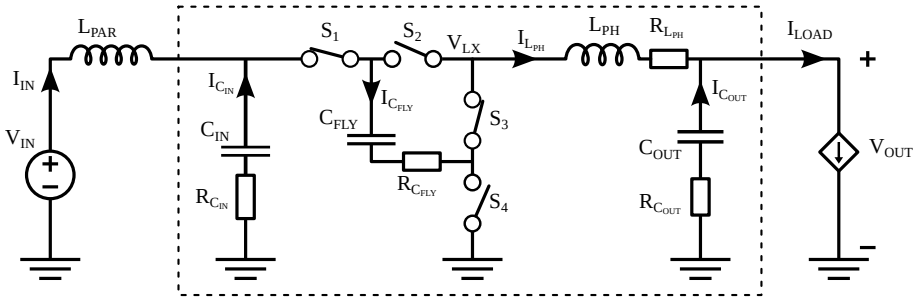


Figure 2.6 – Ideal three-level converter with main parasitic elements of passive components.

- From 0 to αT: S_1 and S_3 are closed.
- From αT to $T/2$: S_3 and S_4 are closed.
- From $T/2$ to $T/2 + \alpha T$: S_2 and S_4 are closed.
- From $T/2 + \alpha T$ to T: S_3 and S_4 are closed.

Current and voltage waveforms are pictured in Figure 2.7. As this converter is operating with one phase, inductor and output capacitor currents are evaluated with the same equations as for a single phase buck converter, Equation (2.5) and Equation (2.7) respectively. The only difference is the current ripple value.

2.1.1.4.1 Inductor In a three-level converter, the operating frequency of the inductor is twice the switching frequency, and the voltage swing at the input of the inductor is half the input voltage. This leads to an inductor current ripple equal to:

$$\Delta I_{L_{PH}} = \alpha\,(0.5 - \alpha)\,\frac{V_{IN} \times T}{L_{PH}}. \tag{2.39}$$

The inductor RMS current is then:

$$I^2_{RMS\_L_{PH}} = I^2_{OUT} + \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.40}$$

2.1.1.4.2 Output capacitor The output capacitor works in the same condition as the one in a one-phase buck converter, delivering current to compensate the current ripple of the inductor. The RMS current of the output capacitor is then:

$$I^2_{RMS\_C_{OUT}} = \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.41}$$

2.1.1.4.3 Flying capacitor The voltage across the flying capacitor is always half the input voltage. This capacitor delivers current to the inductor from 0 to αT and from $T/2$ to $T/2 + \alpha T$. This gives a RMS current value of:

$$I^2_{RMS\_C_{FLY}} = 2\alpha \left(I^2_{OUT} + \frac{\Delta I^2_{L_{PH}}}{12} \right) \tag{2.42}$$

2.1.1.4.4 Input capacitor The RMS current through the input capacitor is:

$$I^2_{RMS\_C_{IN}} = \alpha\,(1-\alpha)\, I^2_{OUT} + \alpha \frac{\Delta I^2_{L_{PH}}}{12} \tag{2.43}$$

Total losses of passive components in a three-level converter are then:

$$\begin{aligned} P_{PAS\_3lvl} = {} & R_{C_{IN}} I^2_{RMS\_C_{IN}} + R_{C_{OUT}} I^2_{RMS\_C_{OUT}} \\ & + R_{C_{FLY}} I^2_{RMS\_C_{FLY}} + R_{L_{PH}} I^2_{RMS\_L_{PH}} \end{aligned} \tag{2.44}$$

Except for the flying capacitor, all losses' contributors in Equation (2.44) are lower than the ones in a one-phase buck (Equation (2.16)) as the current ripple is reduced. The performance gain (or loss) of this converter will be strongly dependent on the ESR of the flying capacitor.

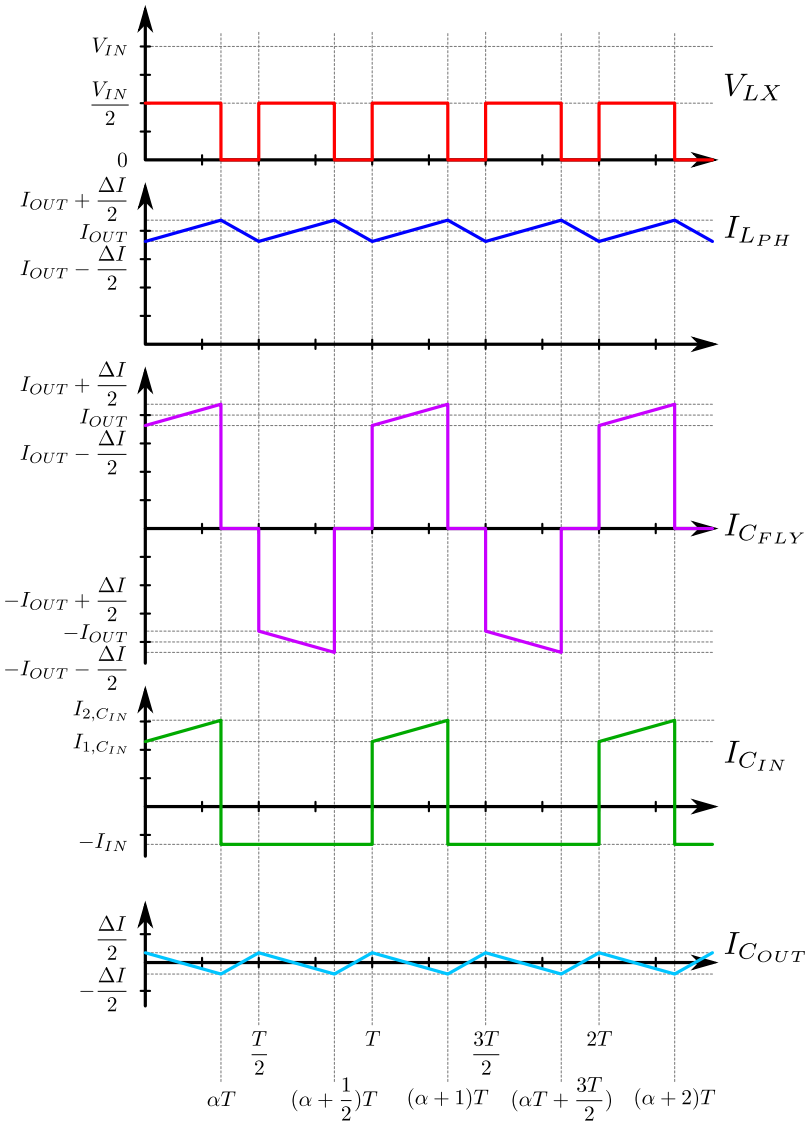


Figure 2.7 – Current and voltage waveforms for a three-level buck converter in CCM.

2.1.2 Losses breakdown and comparison

In order to evaluate architectures in terms of losses, equations developed in Part 2.1.1 are compared against each other in given operating conditions. They are also confronted to ideal circuit simulations using ideal switches for validation purposes.

2.1.2.1 Evaluation conditions and methodology

All circuits are evaluated in the same operating conditions, presented in Table 2.1. They were chosen to be consistent with the specifications (listed in page 42). Parasitic resistance values are arbitrarily chosen. As the goal is to compare the architectures, this choice is not critical.

Table 2.1 – Conditions for architecture evaluation.

Name	Value	Unit
V_{IN}	3.3	V
I_{OUT}	280	mA
T	5	ns
L_{PH}	30	nH
$R_{L_{PH},1\text{-phase}}$	150	mΩ
$R_{L_{PH},2\text{-phase}}$	300	mΩ
$R_{C_{IN}}$	250	mΩ
$R_{C_{OUT}}$	250	mΩ
$R_{C_{FLY}}$	150	mΩ

All converters are evaluated at the switching frequency of 200 MHz. Individual and total losses are compared for various duty cycles.

In order to fairly compare the one-phase with the two-phase converter, the parasitic resistance is doubled in the two-phase converter, making the equivalent current path (two phases in parallel) showing the same resistance as in a one-phase converter.

2.1.2.2 Primary assertion of model pertinence

All selected architectures (one-phase buck (Figure 2.1, two-phase buck (Figure 2.3), coupled two-phase buck and three-level buck (Figure 2.6)) have been simulated in the conditions listed in Table 2.1. Simulation has been performed using standard L, C, R, switches and source elements in a Spice simulator.

The relative differences in RMS current values given both by analytical equations and circuit simulations have been evaluated for various duty cycles.

Table 2.2 – Comparison of analytical equations and circuit simulations results based on RMS current values relative differences (in %).

	1-phase		2-phase		Coupled 2-ph.		3-level	
Duty cycle	0.25	0.45	0.25	0.45	0.25	0.45	0.25	0.45
$I_{RMS\_C_{IN}}$ (%)	−0.24	−0.45	−1.12	0.00	−0.11	+0.04	−0.08	0.00
$I_{RMS\_C_{OUT}}$ (%)	+1.47	+1.08	−5.61	−0.31	−0.04	−0.34	+3.54	+2.62
$I_{RMS\_L_{PH}}$ (%)	−0.11	0.00	−0.14	0.00	0.00	0.00	0.00	0.00
$I_{RMS\_C_{FLY}}$ (%)	-	-	-	-	-	-	−0.05	+0.04

Table 2.2 shows the relative deviation between analytical equation results and circuit simulation results. This relative error is very small (most of the time less than 1 %), except for the output capacitor. However as the output capacitor is the smallest contributor to losses, this is not critical in first approach. Equations can then be used to evaluate the losses of the selected architectures.

2.1.2.3 Breakdown of losses

Figure 2.8 presents the contributions to the losses of all components in each converter architecture. Red are the inductors losses, green the output capacitor losses, blue the input capacitor ones and purple the flying capacitor ones (only for three-level converter). For the coupled-inductor converter, coupling factor is supposed optimal (see Equation (2.32)) for every duty cycle.

Output capacitor losses are very small compared to other losses. Except for the one-phase buck, they are negligible. This means that the parasitic resistor of the output capacitor is not critical in terms of losses.

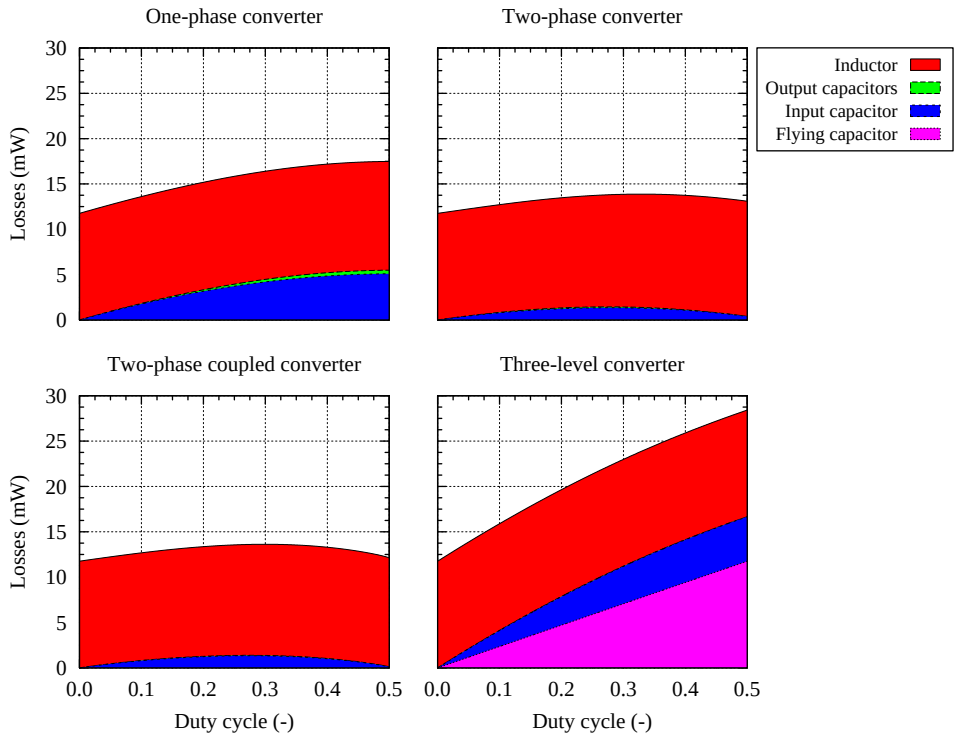


Figure 2.8 – Breakdown of losses in the evaluated architectures, for a duty cycle varying from 0 to 0.5.

The inductor losses are fairly constant whatever the architecture. They are also the dominant losses. This implies that the choice of the inductor plays a crucial role in the converter performance. A value of $5\,\mathrm{m\Omega/nH}$ has been chosen for single phase converters, and $10\,\mathrm{m\Omega/nH}$ for two-phase converters. Coupling reduces a bit the inductor losses by decreasing the current ripple, thus the RMS current. This is mainly noticeable when the duty cycle becomes close to 0.5. Input capacitor losses significantly decrease in two-phase converters. This is one of the major benefit of the multiphase approach.

The three-level converter presents significantly higher losses than the other architectures because of the flying capacitor. The main interest of the three-level converter is to reduce by a significant factor the current ripple through

the inductor compared to a one-phase buck converter. In order to benefit from the reduced current ripple, one could use a much smaller inductor, leading to a resistance also significantly reduced, diminishing inductor losses. However, the gain would still not counterbalance the important losses due to the flying capacitor.

The best candidate architecture in terms of efficiency is then the two-phase converter with coupled inductors. It gathers the advantages of the two-phase converter with a reduced phase current ripple.

2.1.2.4 Coupled two-phase converter

As the coupled two-phase converter is the structure of interest (justified by losses considerations) its behavior is further analyzed. The dimensioning and optimization of the coupled inductors with respect to specifications are detailed in Section 2.4.

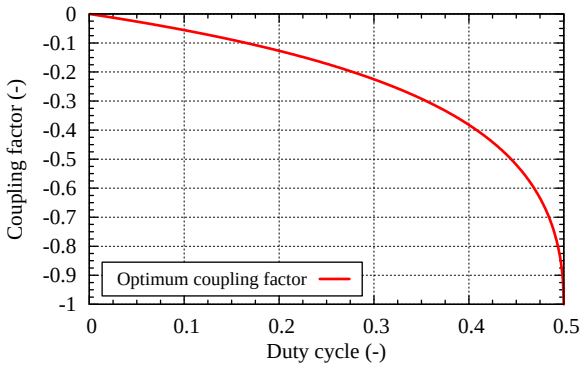


Figure 2.9 – Optimum coupling factor for a coupled two-phase buck, for a duty cycle varying from 0 to 0.5.

Figure 2.9 shows the evolution of the optimum coupling factor (Equation (2.32)) with the duty cycle. The factor is negative, meaning that the inductors are coupled in opposite polarities. It quickly drops to -1 when the duty cycle tends to 0.5. For a relatively low duty cycle, the optimum coupling factor is not very high.

Figure 2.10 shows the evolution of the current ripple when varying the coupling factor. We see that the current ripple decreases until it reaches the

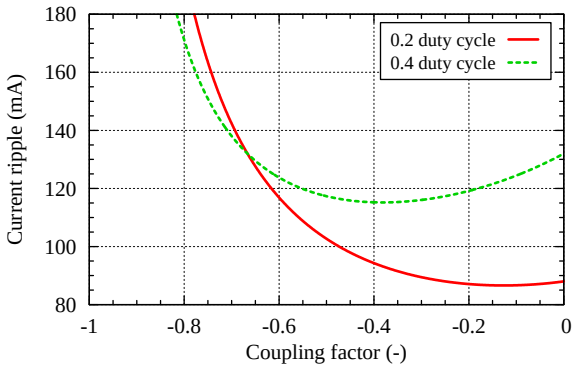


Figure 2.10 – Current ripple for various duty cycles, for a coupling factor varying from 0 to -1.

optimum coupling factor, and then it increases to a very high value – at the $k = -1$ limit, it tends to infinity. So having a coupling factor close to one is not desirable at all, even if it is the optimum coupling factor. For a duty cycle different than 0.5, it is highly unstable in terms of current ripple.

In a DC-DC converter, it is very impractical to have a varying coupling factor. The coupling factor is fixed when the output filter is designed. So having the optimum coupling factor for any duty cycle is highly improbable and impractical. It is necessary to see the evolution of the current ripple at a fixed coupling factor in order to confirm (or reject) the interest of coupling.

Figure 2.11 shows the current ripple value when varying the duty cycle, far various coupling factor. The first curve is the reference case when the coupling factor is null (equivalent to two uncoupled inductors). The second curve is the other extreme case, when the coupling factor is always optimum. The third curve shows the current ripple value when the coupling factor is fixed to -0.35. In this case, the ripple value slightly increases with respect to uncoupled inductors for a duty cycle varying from 0 to 0.25, and then becomes lower, tending to the value with optimum coupling. Ripple reduction for a duty cycle of 0.5 is not as important as with the optimum coupling factor, but still gives significantly better results than without coupling. The last curve is the current ripple value for a fixed coupling factor of -0.75. The ripple reaches higher value than in the case of uncoupled inductors, up to a duty cycle of

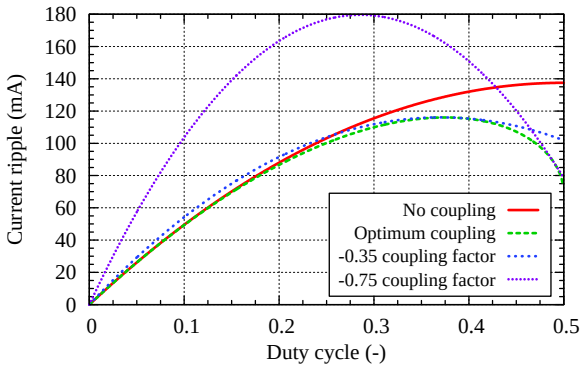


Figure 2.11 – Current ripple evolution for various coupling factors, and duty cycle varying from 0 to 0.5.

0.43, making the coupled inductors worse than their uncoupled counterpart most of the time.

In conclusion, coupling the inductors is beneficial for reducing the current ripple value, but coupling factor must be chosen wisely in order to avoid instability and considerably increase current ripple. Design of the coupled inductor structure is detailed in Part 2.4.2.2.

2.2 Control strategies

Control of various DC-DC converter topologies has been studied for a long time, and is relatively well documented [Eri01; Moh03]. Choosing and implementing the appropriate control strategy is not the core of the presented work. However some considerations about control have been developed and are presented here. A control strategy is then proposed but was not implemented.

2.2.1 Linear control strategies

The converter can be controlled in a linear fashion, by either controlling output voltage or output current.

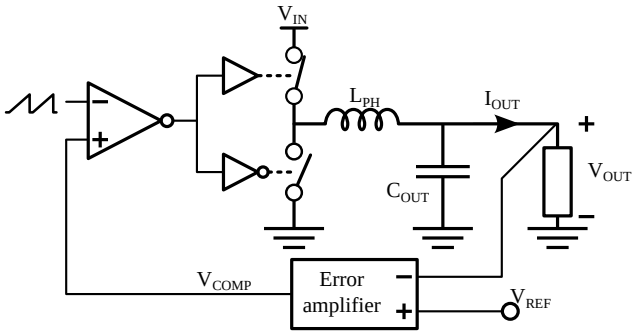


Figure 2.12 – Voltage-mode PWM control simplified schematic.

2.2.1.1 Voltage-mode control

Figure 2.12 depicts a voltage-mode controlled converter with Pulse Width Modulation (PWM) mode in CCM. It comprises the PWM generator, the power stage, the output filter (L_{PH} and C_{OUT}) and a linear compensation. The linear filter compares the output voltage to a reference voltage, and generates an error voltage that is then compared to a ramp waveform in order to build a PWM signal.

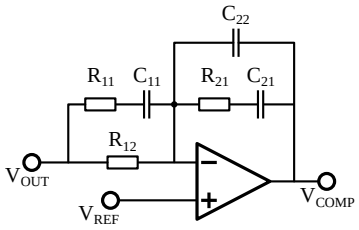


Figure 2.13 – Classical type III voltage error amplifier.

The linear filter classically used in the feedback is a type III voltage error amplifier, depicted in Figure 2.13. This circuit provides two zeros and three poles, including the operational amplifier main pole. The low frequency pole is used to control the static error of the converter. The other pole is used to maximize the attenuation of the switching ripple and high frequency noise. The two zeros are canceling the LC output filter double pole.

Using this kind of control and filter gives a generally stable system, but

suffers from approximation. First the switching of the power stage is intrinsically a non linear process. Stability is ensured if the converter open-loop bandwidth is well below the switching frequency (e.g. ten times lower). Also stability is valid for steady-state. Large scale instabilities can occur in some transient conditions, for instance the "period doubling" phenomena, also called subharmonic instabilities, described in [Pap04].

2.2.1.2 Current-mode control

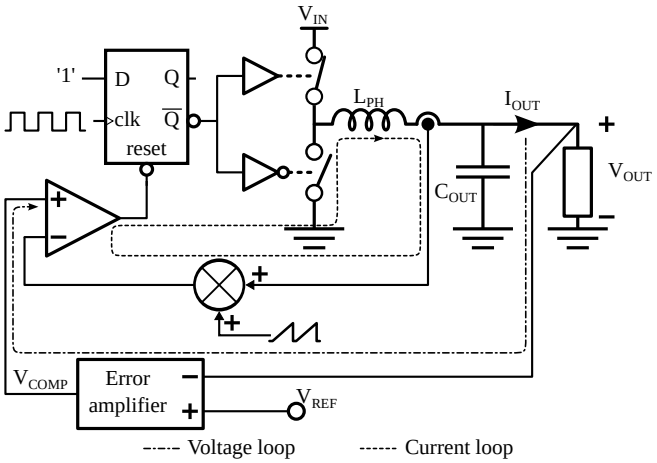


Figure 2.14 – Current-mode PWM control simplified schematic.

A current mode control converter is presented in Figure 2.14. The difference between the voltage mode control is that a current loop is added in order to regulate the inductor current. The current loop represented here is a "peak-current" type loop, meaning that the positive peak current is regulated. Other current loops exist, such as the "valley-current" loop (where the negative peak current is regulated) and the average current loop.

The general behaviors of current mode control strategies are presented in [She07]. As the inductor current is regulated, the current loop can be considered as a voltage-controlled current source. This makes the output filter a first order system with a single pole (formed by the output capacitor) that is easier to stabilize [For98]. A type II voltage error amplifier is then sufficient.

Regulating the inductor current makes the line transient performances better as the inductor current is directly impacted by the input voltage. Furthermore this kind of control and the only one pole rejects the resonant frequency of the LC output filter that lowers the performances of a voltage-mode PWM control. As a consequence a well designed current-mode controller demonstrates a wider regulation bandwidth and a lower output impedance than a voltage-mode control.

However sensing the current through inductor with a sufficient bandwidth is not an easy task especially at high switching frequency. A possible solution that doesn't decrease the efficiency is to sense the voltage drop across a switch [Che08]. This technique requires a high current sense gain and a bandwidth much higher than the switching frequency, which is difficult to obtain [Tak11]. An advanced solution was recently demonstrated [Ahs15].

2.2.2 Sliding-mode and hysteretic regulators

Linear control techniques are well-known but they are suffering from some weaknesses, e.g. limited regulation bandwidth, as previously described. This part presents an alternative to linear control methods.

2.2.2.1 Ripple-base sliding-mode regulator

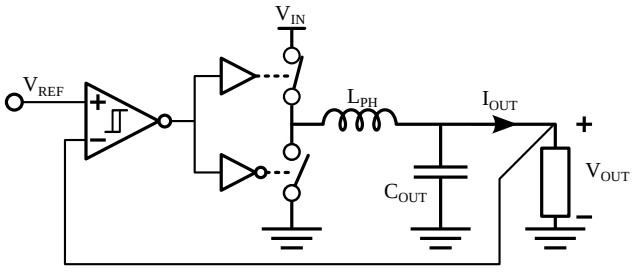


Figure 2.15 – Ripple-based control simplified schematic.

A converter with a simple ripple-based controller is presented in Figure 2.15. This kind of control is also called hysteretic control. The output voltage is directly sent to a comparator with an hysteresis. The other input of the comparator is the reference voltage. The output of the comparator

changes when the output voltage goes below (or above) the output voltage minus (or plus) half the hysteric cycle. This control method ensures that the output voltage is kept around the reference voltage, inside a given window, which is fixed by the hysteretic cycle.

The limitations of this control scheme is that the parasitic series resistor of the output capacitor needs to be sufficiently high in order to operate normally [Bao13]. Having a high ESR on the output capacitor is not something that is wanted as it would increase the losses and the static current ripple. Besides, the chosen capacitor technology (3D PICS capacitors) provides very low ESR values.

2.2.2.2 Current-mode sliding-mode control

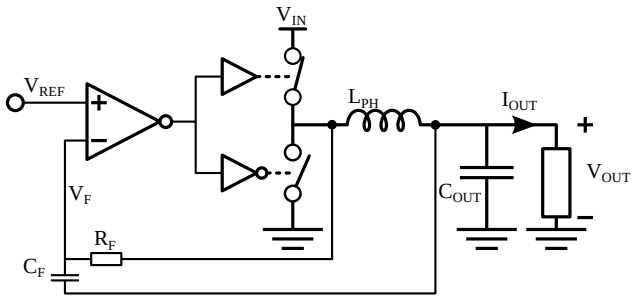


Figure 2.16 – Simplified schematic of current-mode sliding-mode control.

In order to get sliding mode control to work in the case of low output capacitor ESR value, it is possible to use the inductor current to get a significant ripple for control. The objective is to use a sliding function that mixes both the output voltage and inductor current. A way to achieve this is to use a current emulation filter, as shown in Figure 2.16. The R_F resistor and C_F capacitor are integrating the voltage across the inductor, giving voltage that is a scaled image of the inductor current. Several filters can be used to emulate the inductor current [Cas07].

As the output voltage is kept quasi-constant, the capacitor current is equivalent to the inductor current ripple. An equivalent behavior can be achieved by measuring (or emulating) the current through the output capacitor, as proposed in [Tan05; Vie10].

Ideally, an infinite switching frequency is required in order to minimize the error voltage. This chattering phenomena is extensively described in [Utk99]. This is not practically conceivable, as frequency is limited by delays in the feedback loop and switching speed. Furthermore a too high unpredictable frequency would increase the switching losses.

2.2.3 V^2, quasi-V^2 and V^2I_C control

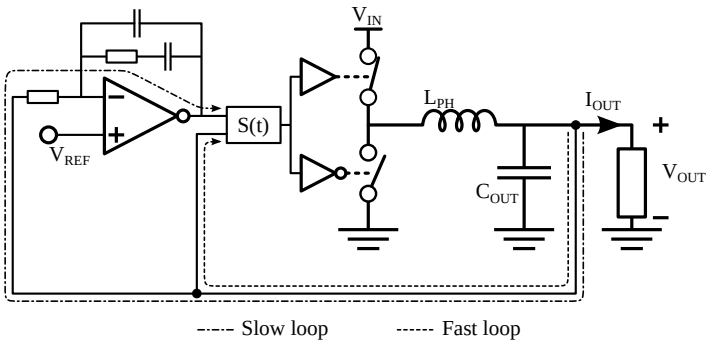
The idea behind the V^2, quasi-V^2 and V^2I_C controllers is to try to get the best of both the linear controllers and the sliding mode controllers. Compared to hysteretic controllers, a slow feedback loop is added in order to get a satisfactory static voltage accuracy while keeping the fast transient performances. All these strategies are extensively described in [Cor15].

The V^2 control strategy senses only the output voltage. It is then a two loops scheme, one fast and one slow. The fast loop behaves like a sliding mode control loop, and the slow loop like a linear voltage-mode control. Such a control loop is depicted in Figure 2.17a.

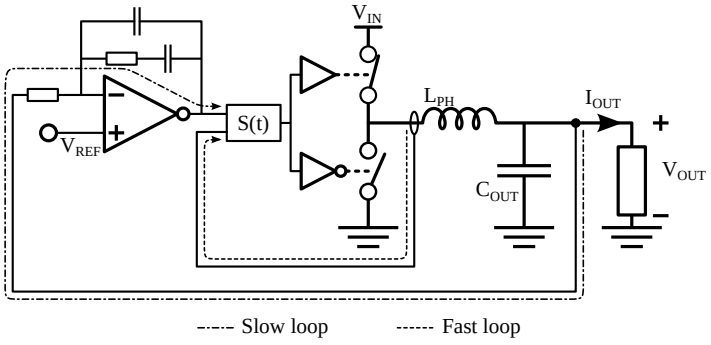
In converter where the output voltage ripple is kept very small (e.g. if the ESR of the output capacitor is negligible), the fast loop of a V^2 controller is very hard to design. In order to counteract this issue, a quasi-V^2 approach senses the inductor current and uses it in the fast loop. A converter with a quasi-V^2 control mode is depicted in Figure 2.17b.

Another way to have ripple information is to sense the output capacitor current. This is the V^2I_C approach, depicted in Figure 2.17c.

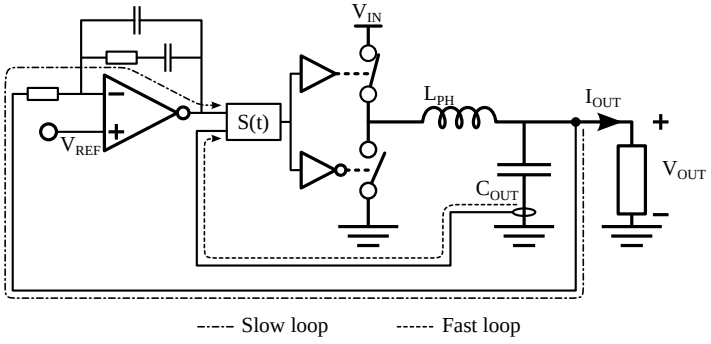
These two last controllers are equivalent as they are both using the output voltage in a slow and accurate loop, and the current in a fast loop. The difference is where the fast varying signal is sensed. From a control point of view, these types of loop use the output voltage and its derivative.



(a) V^2 control simplified schematic.



(b) Quasi-V^2 control simplified schematic.



(c) V^2I_C control simplified schematic.

Figure 2.17 – Simplified schematic of V^2, quasi-V^2 and V^2I_C controls.

2.2.4 Selection of a control method

In all converters that uses the current as a regulation input, the issue is to sense this current with a sufficient gain and bandwidth, along with a strong noise immunity, without lessening the efficiency. This issue becomes more prevalent if the switching frequency is very high, which is our case. So linear and sliding-mode current-mode controls are excluded in a first approach, as well as enhanced V_2 and the V^2I_C control modes.

As the objective is to target a small output current ripple and a high efficiency, solutions that require a high ESR of the output capacitor are not practicable. Thus sliding-mode voltage-mode and V^2 control mode are also to be discarded. The targeted application is very sensitive to output voltage quality, in amplitude and spectrum.

A linear voltage control loop seems to be one good candidate. It provides a very good static accuracy. Its inferiority in transient performance is counterbalanced by the very high switching frequency, allowing for a relatively high feedback loop bandwidth. Demonstration of a voltage-mode PWM/PFM control has been reported for switching frequency above 100 MHz [Bat12b]. Linear voltage-mode control is then the selected control method, but no implementation is proposed in the present work. It was skipped in this work as the issue is then less a challenge than an engineering effort.

2.3 Modeling of power switches

The analysis and modeling of the active components is carried out in this section. The goal of this analysis is to compare various MOSFETs in terms of energy efficiency in a switched-mode power supply application. The objective is to have a simple model, capable of predicting power losses. After the model is built, it is used to compare and select the proper device for our design target.

2.3.1 MOSFET model

2.3.1.1 Model definition

In order to evaluate switching and conduction losses, the model is built using capacitors and resistors. The selected SPICE simulator does not accommodate

easily HDL-based models what could have been also a reasonable approach.

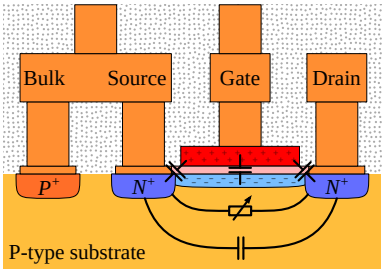


Figure 2.18 – Cross-section view of an N-MOSFET with parasitic elements.

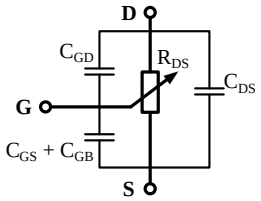


Figure 2.19 – Schematic model of an N-MOSFET with parasitic elements.

Figure 2.18 shows a cross-section of an N-type MOSFET with parasitic capacitors. The equivalent circuit of this MOSFET is presented in Figure 2.19. Modeling is rather simple based on four non-linear capacitors (with two of them in parallel) and one variable impedance. As the MOSFET is utilized as a switch, it is used in its linear region ($V_{DS} < V_{GS} - V_{TH}$), so the resistor is considered as a function of V_{GS} only.

Despite being already simplified compared to some other models which detail the switching operation in several steps [Ora15], a model that could be even more condensed would be better and could better act as a comparison criteria. In order to simplify the model, only one capacitance connected to the gate is considered. This capacitance is the sum of all three gate capacitances (gate-to-source, gate-to-bulk and gate-to-drain). This capacitance is driven by the control signal. This allows for separating the losses of the drivers from the losses of the power path. This macro-switch model is presented in Figure 2.20.

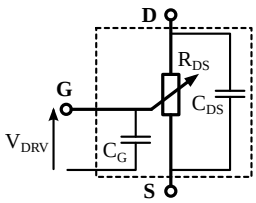


Figure 2.20 – Model considered for a N-MOSFET.

The controlled-impedance is driven by a voltage source, that charges and discharges the input capacitance C_G. The driving voltage modulates the R_{DS} resistor. The drain-to-source capacitor is either charged by the input source voltage (when the switch is opened, i.e. high R_{DS}) or discharged through the switch (when the switch is closed, i.e. low R_{DS}).

2.3.1.2 Losses

With the simplified model, it becomes relatively simple to evaluate the losses of a switch. From the driving signal perspective, the switch is only a capacitor. The energy stored in a capacitor is equal to:

$$E_C = \frac{1}{2}CV^2 \tag{2.45}$$

Since the charging efficiency of a capacitor by a constant voltage source through a resistive path is equal to 0.5 (as shown e.g. in [Wen11b]), the energy supplied from the driver for a full charge/discharge cycle (assuming no charge recycling mechanism) is equal to:

$$E_{DRV} = C_G V_{DRV}^2 \tag{2.46}$$

In order to simplify the notation and be comparable with other figures of merit, it is convenient to let the gate charge appear in the formula (using $Q_G = C_G V_G$). As the switch is driven at a given operating frequency (F_{SW}), power losses in the driver side are then formulated as:

$$P_{DRV} = Q_G V_{DRV} F_{SW} \tag{2.47}$$

The other contribution to the switching losses are the losses due the drain-to-source capacitance. During a switching cycle, this capacitor is charged at the full converter input voltage, and then fully discharged through the closed switch. If we then again assume no charge recycling mechanism (i.e. the capacitor is fully discharged through R_{DS}) the power losses due to drain-to-source capacitance are:

$$P_{SW,DS} = C_{DS} V_{IN}^2 F_{SW} \tag{2.48}$$

We can then compute the conduction losses of the switch, which are simply the resistive losses through the drain-to-source resistor.

$$P_{COND} = R_{DS} I_{DS,RMS}^2 \tag{2.49}$$

The RMS drain-to-source current is computed using equations and waveforms presented in Part 2.1.1.

The developed model here allows for a simple loss evaluation. However the considered capacitance are not constant. The gate capacitance is dependent on the gate voltage, and the drain-to-source capacitance is dependent on the drain-to-source voltage and the gate voltage. The gate voltage dependence on the drain-to-source capacitance can be neglected since this capacitance is only charged when the gate voltage is equal to 0 V.

When combining all the calculations and considerations developed above, we end up with a global formula for calculating the power losses of a switch:

$$\begin{aligned} P_{SW}(V_{DRV}, V_{IN}) = {} & R_{DS}(V_{DRV}) I_{DS,RMS}^2 \\ & + F_{SW} \left(C_{DS}(V_{IN}) V_{IN}^2 + Q_G(V_{DRV}) V_{DRV} \right) \end{aligned} \tag{2.50}$$

In order to be able to evaluate this function, the access to $R_{DS}(V_{DRV})$, $Q_G(V_{DRV})$ and $C_{DS}(V_{IN})$ is necessary.

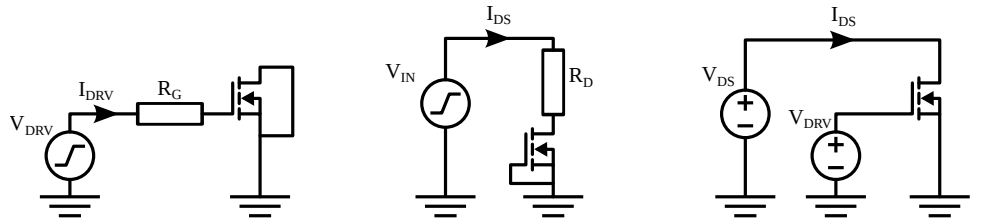
2.3.2 Technology evaluation

The selected technology has been evaluated using the switch model developed in Part 2.3.1. The standard digital 40 nm CMOS technology library gathers several MOSFET structures. These structures are optimized for various types of application, for instance for input/output, or for memory access, or even for high voltage handling. For each one of these devices, the drain-to-source resistance, the drain-to-source capacitance and the gate capacitance have been extracted, and devices have been compared. In order to calculate the RMS current through each transistor, a duty cycle of 0.36 (equal to $^{1.2}/_{3.3}$) is utilized.

2.3.2.1 Extraction of model parameters

The $R_{DS}(V_{DRV})$, $Q_G(V_{DRV})$ and $C_{DS}(V_{IN})$ have been gathered by the means of simulation for each device using the design kit in Cadence Virtuoso. Each

transistor put in simulation is a 10 µm large device with its minimal length. Simulations are very simple with a very short runtime, allowing for quick characterization. Figure 2.21 shows the three basic circuits simulated in order to get the required parameters for performance evaluation.



(a) Circuit for gate capacitance characterization.

(b) Circuit for drain-to-source capacitance characterization.

(c) Circuit for drain-to-source resistance characterization.

Figure 2.21 – Simulation circuits for MOSFET characterization.

For capacitance/charge extraction a pulse voltage source is used in a transient simulation (circuits in Figure 2.21a and Figure 2.21b) . Current through the resistor is measured and integrated in order to get the charge value, for a list of driving voltage values.

In order to get the value of the drain-to-source resistance two voltage sources are used in a DC simulation (circuit in Figure 2.21c). The drain-to-source voltage is set to a low value (50 mV) and current is measured for various driving voltage. By doing this it is possible to get the evolution of the drain-to-source resistance with the driving voltage.

2.3.2.2 MOSFET comparison

Several MOSFET types have been characterized. For each type, the N-channel and P-channel have been characterized. Three types of MOSFETs are available: the 5 V MOSFET with thick oxide, the 3.3 V MOSFET with medium oxide thickness and the regular 1.2 V with a thin gate oxide. The two MOSFETs with higher voltage handling are dedicated to input/output functions, as well as power handling. The low voltage MOSFET is the core device used for

digital/analog circuits. Clearly the 1.2 V devices can not fulfill the specifications (3.3 V input voltage), but they are still evaluated as technology reference point. All values are presented per µm of channel width.

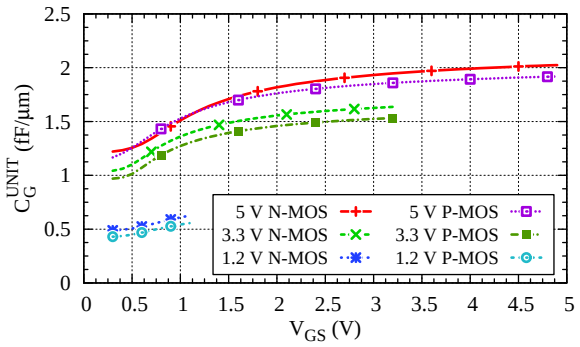


Figure 2.22 – Evaluation of the gate capacitance of the P-type and N-type MOSFETs in 40 nm CMOS library.

Figure 2.22 shows the gate capacitance per µm width values of each MOSFET when varying the gate voltage. Capacitances of N-MOSFET and P-MOSFET are almost the same, the capacitance being slightly larger for N-type devices. Because of their larger minimum length and thicker gate oxide, 5 V and 3.3 V have a larger gate capacitance.

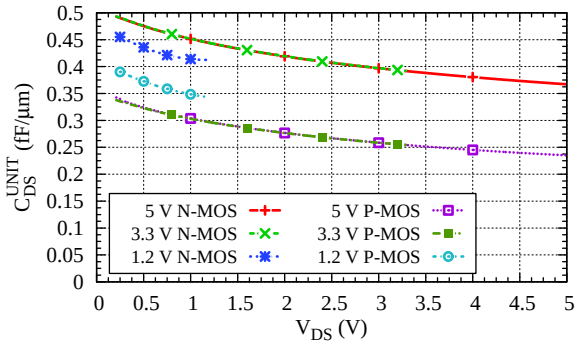


Figure 2.23 – Evaluation of the drain-to-source capacitance of the P-type and N-type MOSFETs in 40 nm CMOS library.

The drain-to-source capacitance (per µm width) characterization of each MOSFET is presented in Figure 2.23. It shows same values for 5 V and 3.3 V devices. The N-channel 1.2 V has a smaller capacitance value than the two other N-channel transistors. For the P-channel, it is the opposite: the 1.2 V device has a larger value than the 5 V and 3.3 V devices. As this capacitance is relatively small and doesn't change a lot across all the considered devices, it won't be the one that will determine the choice of the device for the design.

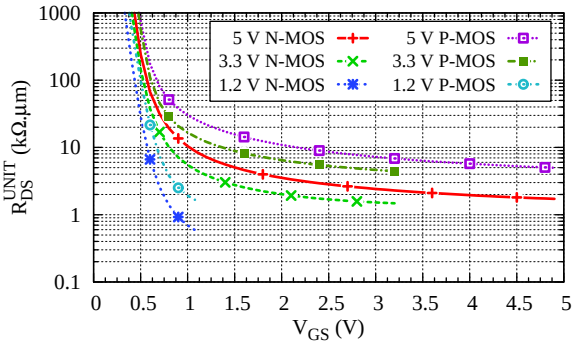


Figure 2.24 – Evaluation of the drain-to-source resistance of the P-type and N-type MOSFETs in 40 nm CMOS library.

The drain-to-source resistance evolution (referred to its width in µm) with the gate-to-source voltage is presented in Figure 2.24. We see that the factor between the N-MOSFET and the P-MOSFET is approximately three for every type of transistors. This factor is classically seen between N-MOSFET and P-MOSFET due to the mobility difference between electrons (in N-MOSFET) and holes (in P-MOSFET). Quite predictably, the MOSFET with less resistance value goes with the voltage capabilities of the transistors: the higher the voltagerating, the larger the resistance.

Based on these three characterizations and the losses model presented in Part 2.3.1, it is possible to select the device that will give the best efficiency in the converter. As the drain-to-source capacitance is not determinant because of its relative low and invariant value, the focus is on the the gate charge and channel resistance.

The characteristic of each MOSFET is plotted in the $Q_G V_{GS} - R_{DS}$ plane

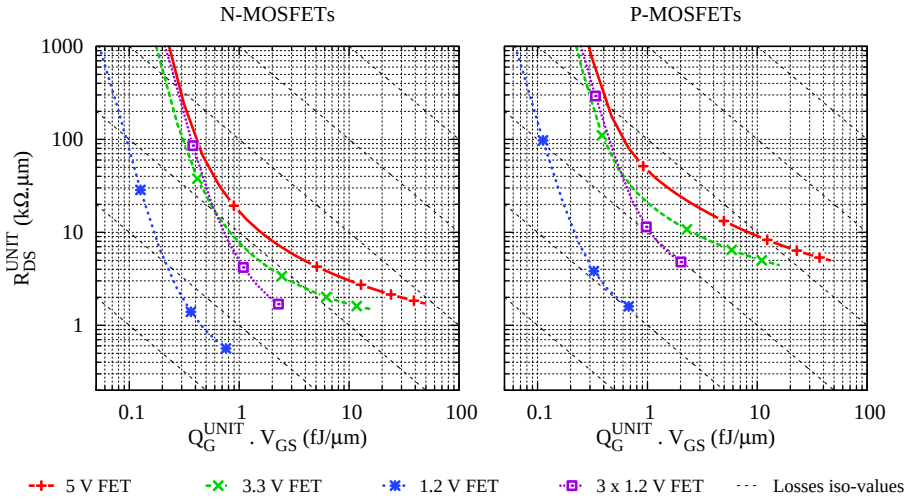


Figure 2.25 – Performance plane of the considered N-type and P-type MOSFETs.

in Figure 2.25. Based only on data in the plane (i.e. neglecting the C_{DS} contribution) and assuming a MOSFET width of W_{MOSFET} (in µm), losses are equal to:

$$P_{MOSFET} = I_{DS,RMS}^2 \frac{R_{DS}^{UNIT}}{W_{MOSFET}} + F_{SW} Q_G^{UNIT} V_G W_{MOSFET} \tag{2.51}$$

By differentiating this expression, it is possible to compute the optimum MOSFET width for a given current and frequency. The optimum width is:

$$W_{OPT} = I_{DS,RMS} \sqrt{\frac{R_{DS}^{UNIT}}{F_{SW} Q_G^{UNIT} V_G}} \tag{2.52}$$

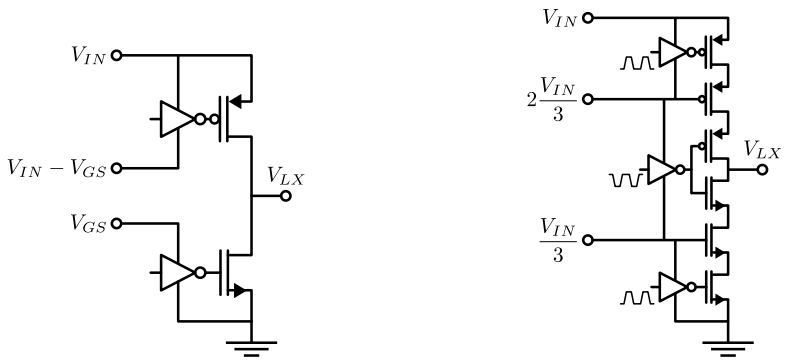
So for any operating point, if we assume that we are at optimum width, the minimum losses achievable are:

$$P_{OPT} = I_{DS,RMS} \sqrt{F_{SW} Q_G^{UNIT} V_G R_{DS}^{UNIT}} \tag{2.53}$$

We can deduce from Equation (2.53) that losses are constant if the product $Q_G V_G \cdot R_{DS}$ is constant. These iso-values of losses are plotted in Figure 2.25. The best MOSFET would sit in the lower left corner.

The best available MOSFET is the low voltage one. However, it can not be used alone as it can not withstand the converter input voltage. The 3.3 V MOSFET seems then to be the best candidate for our specifications. Using graph from Figure 2.25 also shows what is the optimum working point of the transistor. For the 3.3 V devices, in order to get best efficiency, the voltage applied should not be too high.

In addition to the characterization of each MOSFET, an hypothetical MOSFET is also included. This hypothetical device is built using the 1.2 V type that is three times more lossy compared to a single one, both in terms of gate capacitance and drain-to-source resistance. This is the series configuration of three low-voltage MOSFET. From the graph, we can expect that three low voltage devices in series will give a better efficiency than a single 3.3 V MOSFET. Also, putting these devices in series can make a "macro-switch" that can withstand up to 3.6 V.



(a) Power stage of a synchronous buck using 3.3 V MOSFET.

(b) Power stage of a synchronous buck using three 1.2 V MOSFET in series.

Figure 2.26 – Considered power stages.

Figure 2.26 depicts the two considered power stages. The one in Figure 2.26a is built using 3.3 V P- and N-MOSFETs. In Figure 2.26b the power stage is built with three low voltage MOSFETs in series. This power stage is referred to as the three-MOSFET cascode power stage. A brief analysis based on simulation results of this structure is proposed in [Kur05]. Both figures are simplified schematics, design details of each structure are presented

in Chapter 3.

2.3.3 Expected efficiency

Based on MOSFETs models and the technology evaluation, it is possible to evaluate the losses of the power stage. This is performed for both 1-phase and 2-phase configurations, and standard and cascode power stages. In each case, the optimum width is calculated using Equation (2.52), at the nominal output current (280 mA). Losses are calculated using Equation (2.53). As this equation doesn't include the losses due to the drain-to-source capacitance, they are added using Equation (2.48), with:

$$C_{DS} = C_{DS}^{UNIT} \times W_{OPT} \tag{2.54}$$

A gate-to-source voltage of 2 V is assumed for both P- and N-MOSFETs in standard power stage, and a gate-to-source voltage of 1.1 V for the cascode power stages. High side and low-side MOSFET currents are evaluated using waveforms from Part 2.1.1:

$$I_{RMS}^{HS} = \sqrt{\alpha I_{PH}^2 + \alpha \frac{\Delta I_{PH}^2}{12}} \tag{2.55}$$

$$I_{RMS}^{LS} = \sqrt{(1-\alpha)\, I_{PH}^2 + (1-\alpha)\, \frac{\Delta I_{PH}^2}{12}} \tag{2.56}$$

In order to simplify the calculations, and as the current ripple through the inductor is not known, it is supposed to have a negligible contribution to the RMS current. As the ripple contribution to the RMS current is less than 4 % when ripple value is equal to the average current, this hypothesis is not unreasonable. Results are summarized in Table 2.3 for a switching frequency of 200 MHz. For the two-phase configuration, results are given for one phase assuming the current is shared evenly between the two phases.

We see that the optimum width in a two-phase configuration is exactly half the optimum width for the one-phase configuration, meaning the total width of all MOSFETs is conserved. Regarding the losses, they are also divided by

Table 2.3 – Losses evaluation of standard and cascode power stage, using active technology model.

		One-phase		Two-phase	
		Standard	Cascode	Standard	Cascode
$W_{HS,OPT}$	(mm)	12.51	18.30	6.25	9.15
$P_{HS,R_{DS}}$	(mW)	14.60	7.40	7.30	3.70
$P_{HS,C_{GS}}$	(mW)	14.60	7.40	7.30	3.70
$P_{HS,C_{DS}}$	(mW)	6.92	4.59	3.46	2.29
$P_{HS,TOT}$	(mW)	36.12	19.39	18.06	9.70
$W_{LS,OPT}$	(mm)	9.02	13.64	4.51	6.82
$P_{LS,R_{DS}}$	(mW)	11.23	6.21	5.61	3.11
$P_{LS,C_{GS}}$	(mW)	11.23	6.21	5.61	3.11
$P_{LS,C_{DS}}$	(mW)	7.69	4.09	3.85	2.04
$P_{LS,TOT}$	(mW)	30.14	16.51	15.07	8.26

two when comparing one-phase and two-phase configurations. As in the two-phase configuration only half the converter is considered, total losses are the same for both configurations. This implies that for a given technology, using several phases doesn't impact the efficiency of the switches. Furthermore, the achievable converter efficiency when considering only active components doesn't depend on the current (at given input and output voltages). In our case, expected efficiency (computed using losses from Table 2.3 at nominal power point) when using a standard power stage is expected to be 83.5 % (for both single and double phase structures) and 90.3 % for the converter with a cascode power stage. So even with the cascode power stage, almost all the losses budget (with respect to the 90 % efficiency target) is consumed by the active components.

As the cascode power stage displays the best performance, it is the selected structure for our design objective. Its full optimization and design is detailed in Section 3.2.

2.4 Output filter and decoupling capacitors

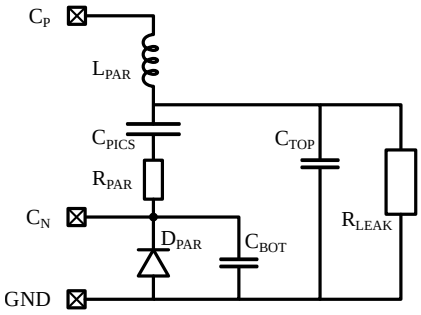
This section presents the models used for the passive components and the dimensioning for the design target. It includes models of the capacitors, inductors and coupled inductors. After describing the models and their limitations, the sizing of the output filter and the decoupling capacitors is detailed. As the dimensioning of the passive components is evaluated prior to active components, it is based on pre-design considerations. Co-optimization could further improve the converter performance, but it was not performed in this work.

2.4.1 Circuit models

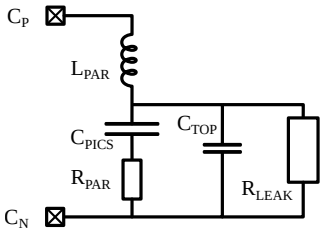
This part presents the circuit models that are used for optimizing the passive components. As the technologies are under development, models are subject to changes during design phase. Because of this, models for the passive components are simplified in order to be less dependent on technological parameter tuning, and ease optimization in some way. Reader must consider that the final technologies (CMOS, inductance, capacitors) are here the ones obtained with the demonstrator in Chapter 4. Comparison between simulations and measurements will be carried out and feedback on device sizing will be given in Chapter 4.

2.4.1.1 Capacitor model

The capacitor technology is the 3D-PICS technology from IPDiA [Lal13]. It can be modeled as a sub-circuit as depicted in Figure 2.27a. C_P and C_N are the positive and negative electrodes of the capacitor, and GND terminal is the silicon substrate. C_{PICS} designates the main capacitor. The access inductance is modeled by the localized parameter L_{PAR}, and the parasitic series resistance is R_{PAR}. A parasitic diode D_{PAR} is present between the C_N and GND terminal. C_{TOP} and C_{BOT} are the parasitic capacitances between capacitor electrodes (top and bottom) and the substrate. The diode and the top and bottom capacitance have an impact if the capacitor is used as a flying capacitor, e.g. in a switched-capacitor application. In switched-capacitor Switched-Mode Power Supply (SMPS) design, the parasitic capacitors appear as an effective coefficient that modulates the electrical value of the physical



(a) Full model schematic of a PICS trench capacitor.



(b) Simplified model schematic of a PICS trench capacitor.

Figure 2.27 – Model of a PICS trench capacitor.

flying capacitor [Sou15]. The capacitor current leakage is modeled by a resistor (R_{LEAK}) in parallel with the structure.

Since these capacitors are going to be used for decoupling and filtering with respect to the ground, the negative terminal (C_N) and the ground terminal are connected together. So the parasitic diode and parasitic bottom terminal capacitance are shorted thus the parasitic effects of the bottom capacitor are not particularly an issue. The equivalent capacitor is then the one presented in Figure 2.27b. The only parasitic components left are the parasitic access inductance, the equivalent series resistance and the leakage resistance. The capacitance of the top plate is not an issue as it is in parallel with the structure, thus it is beneficial for decoupling.

The main capacitor (C_{PICS}) has a density of approximately $200\,nF/mm^2$ for a voltage rating of 5 V. The top plate capacitance density is approximately $80\,pF/mm^2$. This represents a density of 0.04 % of the main capacitance density. This implies that for dimensioning, it is not relevant to consider this parasitic capacitance.

Leakage impact is only on the losses. As the voltage across the capacitor is almost constant, the leakage current is a DC current, that has no impact on the AC performances of the capacitor. Leakage resistance is at least in the order of the tens of MΩ, meaning that losses are below the µW, assuming 3.3 V at the capacitor terminals. So impact on total losses and efficiency is

negligible considering an output power of hundreds of mW. This resistance can be neglected also in dimensioning. The model of the capacitor is then an RLC series circuit (i.e. circuit in Figure 2.27b with an infinite R_{LEAK} value and null C_{TOP} value).

2.4.1.2 Inductor model

Modeling of magnetic inductors at relatively low frequency is rather well-known [Hil14]. However these models become limited when the operating frequency goes high. The modeling and optimization of the inductors considered in this work are presented in [And13]. The considered structure is depicted in Figure 2.28. Details on the technology of the considered inductors is presented in [Wan07].

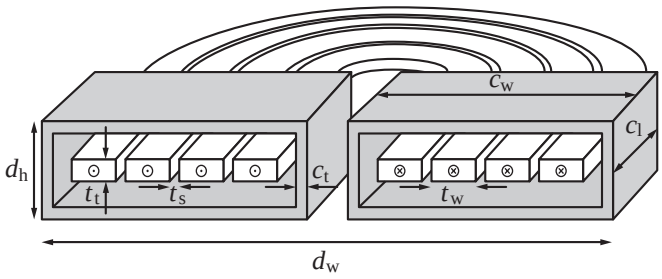


Figure 2.28 – Cross-section of the structure of inductors of interest with relevant geometrical parameters [And13].

One of the issues in magnetic inductors at high frequency is the skin effect of the magnetic material. In order to cope with this, the thickness of the magnetic material needs to be reduced, meaning that more isolated magnetic layers are needed in order to keep a constant inductance value. This makes the manufacturing of these inductors more complex and costly.

The modeling of magnetic material at high frequency is very complex and is not a primary goal of this thesis. The current through the inductor is mostly a DC current, so a very simple inductor model has been used for dimensioning. Inductor model is a simple RL series circuit, depicted in Figure 2.29. Figure 2.29a is for a single inductor, and Figure 2.29b is for two

(a) Model considered for inductor.

(b) Model considered for coupled inductors.

Figure 2.29 – Models considered for single and coupled inductors.

coupled inductors. The parasitic resistance R_{PARx} is supposed to be proportional to inductance value. This parasitic resistance combines the effect of copper trace resistance and magnetic material effects translated into effective resistance. For the coupled inductors, two identical inductors are considered with a coupling factor. Inductor behavior is verified in Chapter 4, as well as the identification of R_{PAR}.

2.4.2 Dimensioning

Based on the models presented previously, the passive components have been dimensioned and optimized for the targeted converter. Closed-loop converter design could not be done due to restrictions on silicon availability. As only open-loop converter is considered, the dimensioning is only partial, based mostly on steady-state considerations. A dimensioning with full close-loop considerations might result in a different output filter (inductor and capacitor) than the selected one.

2.4.2.1 Output filter for one-phase converter

As transient performances are not the key issue in this thesis, output filter sizing is not severely constrained by dynamic requirements. Steady-state voltage and current ripples are the key elements for sizing the output filter. As we rely on dense deep-trench capacitor technology, inductor is the limiting factor.

Inductor current ripple is very important as it defines the limit between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The limit is attained when the current ripple (peak-to-peak) reaches

twice the average current. Our target is to operate most of the time in CCM, meaning that the CCM/DCM limit should be around the minimum load current, which is around 50 mA. This allows for a current ripple of approximately 100 mA, equivalent to an inductance value of 40 nH at 200 MHz switching frequency (80 nH at 100 MHz).

However having a too big inductors displays also some drawbacks. Parasitic resistor of the inductor is roughly proportional to the inductance value. The value given by the inductance manufacturer is that it is approximately 5 mΩ/nH. This means that a high inductance value will make the inductor lossy, which is unwanted. As the active part consumes already a lot of the losses budget, it is necessary to restrain the losses of the inductor, thus limit the inductance value.

Based on all the previously developed consideration, an inductance value of 30 nH has been chosen for 200 MHz switching frequency (and 60 nH for 100 MHz switching frequency). Converter will not operate in CCM at 50 mA load current: but efficiency at nominal current load (280 mA) is favored over minimum load current.

Regarding the output capacitor, the value has been chosen to 15 nF. Using a 15 nF capacitor can meet output voltage accuracy requirements at both 100 MHz and 200 MHz. Having one capacitor for both frequencies makes manufacturing faster and easier.

As the maximum switching frequency considered is 200 MHz, the SRF of the output capacitor should be higher than this value. Thus for a 15 nF capacitor, its ESL should be below 40 pH. This low ESL value is achievable using IPDiA PICS technology, but requires a careful design optimization.

Chosen passive components values have been validated using SPICE simulation. Simulation results are presented in Figure 2.30. Switching frequency is 200 MHz as this is the worst case for passive components. Parasitic inductance of the capacitor is set to 10 pH and parasitic resistance to 150 mΩ, based on data from the capacitor technology supplier. Main input decoupling capacitor (the V_{DD} net) is 30 nF, decoupling capacitors for references ($V_{DD\text{-}HS}$, $V_{SS\text{-}HS}$ and $V_{DD\text{-}LS}$ nets) are 10 nF and output capacitor is 15 nF. Inductance is 30 nH, with a parasitic resistance of 150 mΩ. Simulation was carried using switches based on characterization from Part 2.3.2 on a typical synchronous

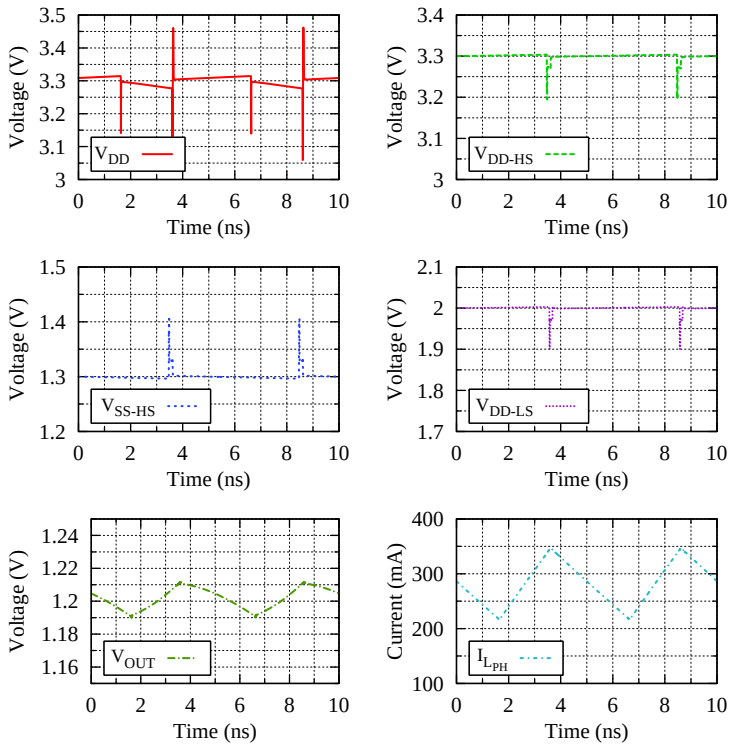


Figure 2.30 – Transient simulation waveforms of input voltages, output voltage and inductor current.

buck converter. We see from the simulation results that the selected passive components values are sufficient to ensure proper input and output decoupling. Spikes seen on voltage waveforms are due to parasitic inductance of the capacitors. Their amplitude and duration are limited so no impact on the converter behavior is observed.

2.4.2.2 Output filter for two-phase coupled converter

In Section 2.1 it has been shown that coupling inductors in two-phase converter helps reducing the current ripple. This can help achieving higher efficiency by several means. The direct one is that reducing the current ripple logically reduces the RMS current, both through the inductor, the high-side and low-side

switches and the input and output capacitors. Since the ripple contribution to the losses is relatively low, the gain exists but is not very significant only considering this. Smaller ripple current value helps reducing the inductance values, leading to a smaller parasitic resistance, thus smaller inductor ohmic losses. The last possible action is to reduce the switching frequency, allowing for smaller losses in the active parts. As Section 2.3 has shown that active components are critical losses contributors, this is the strategy that has been chosen.

The optimization of the coupled inductors is carried out assuming 100 MHz switching frequency. The phase inductance value chosen in this case is 45 nH. It has been chosen to be in between the two uncoupled configurations (30 nH for 200 MHz and 60 nH for 100 MHz).

In order to assess the gain in losses from coupling the inductors, several cases have been considered in simulation. The first one is a reference case, without any coupling. Then inductors are coupled and coupling factor is optimized to get minimum current ripple. The last case introduces an output inductor to the coupled inductor structure. The latter circuit is depicted in Figure 2.31. The motivation is to hold down the sum of the coupled inductors currents. From a practical point of view, a parasitic access inductance will always exist.

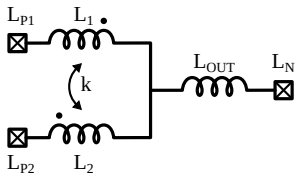


Figure 2.31 – Coupled inductors with an additional output inductor structure.

A constraint on total inductance value is put on all three structure in order to have a fair comparison. This value is set to 90 nH. Filter optimization has been carried out by emulating power stages using pulse voltage sources, an output capacitor of 15 nF in the nominal conditions (3.3 V to 1.2 V, 280 mA load current). Impact of parasitic resistor is neglected. Optimization results are summarized in Table 2.4.

Table 2.4 – Optimization results of coupled inductors structures.

	L_{PH}	L_{OUT}	k	$\Delta I_{L_{PH}}$	Ripple decrease
Case #1	45 nH	-	0	168 mA	-
Case #2	45 nH	-	0.32	152 mA	9.5 %
Case #3	35 nH	20 nH	1	125 mA	25.6 %

Case #1 is the reference case. No coupling is assumed and each phase has 45 nH inductance. Inductor current ripple is then 168 mA.

The case #2 introduces coupling between the two phases without significant L_{OUT} value. Optimum coupling factor given by simulation is 0.32, which is consistent with the value given by Equation (2.32), equal to 0.316. The inductor current ripple is then equal to 152 mA, reducing it by almost 10 % compared to the uncoupled case #1.

The last case #3 uses a physical output inductor in addition to the two phase inductors. The minimum current ripple value is achieved when inductance is shared as follow: 35 nH for each phase, with a coupling factor of 1, and 20 nH for the output inductance. Phase inductor current ripple is then 125 mA. This is a 25.6 % improvement compared to the reference case. We end up with the same ripple value we have with a 60 nH phase inductor at 100 MHz.

The use of an output inductor seems then to be a good strategy to get the most of a total given inductance value. However it requires very tightly coupled inductor to be efficient. A sensitivity analysis on the coupling factor has been performed in order to evaluate if the gain in current ripple value is still significant when some leakage inductance is accounted for (i.e. the coupling factor decreases). A simulation using a coupling factor of 0.8 instead of 1 shows an increase in the phase inductor current ripple of 3.7 mA. This is a relatively small degradation, meaning that the performance of this inductor structure is reasonably robust with respect to the coupling factor. This relaxes the fabrication of inductors.

Regarding the output capacitor, the same 16 nF capacitor than the one for the 200 MHz converter is used. It makes sense to use a capacitor with a SRF higher than 200 MHz even if the switching frequency is 100 MHz as in a

two-phase converter the frequency seen by the capacitor is twice the switching frequency.

2.4.2.3 Input voltage decoupling capacitors

The same input decoupling capacitors are used for all configurations. So they are dimensioned considering the worst case, which is the single phase configuration. These capacitors include the main input decoupling capacitor, and three decoupling capacitors used for the power supply of the drivers.

The main input decoupling capacitor is there to maintain a constant voltage at the input of the converter and deliver the pulsing current. The current that comes from the input voltage source is supposed to be constant due to an important parasitic inductance. A sufficiently high capacitance value is required to achieve this behavior. However a too high value would lead to a capacitor with a low SRF, making it impracticable for high frequency operation. A value of 30 nF is selected, meaning that the ESL must be below 20 pH for proper operation. The value of 30 nF limits the voltage drop below 100 mV when supplying the nominal load current (280 mA) for 10 ns, which allows for a proper behavior of the converter. In terms of ESR, the smallest value possible is the better in term of power efficiency, especially as this capacitor is a non-negligible contributor to the losses. A value below the hundred of mΩ is preferable. It is still less critical than the ESL constraint: a lossy capacitor is still better than a non-functional one.

Regarding the three capacitors for decoupling power supplies of the driver, the same constraints applies in terms of functionality and frequency operation. However current drawn from these is much less than the current drawn from the main decoupling capacitor as they do not supply the main power, so their values doesn't need to be as important. A value of 10 nF is chosen. A smaller capacitance value lessen a bit the ESL constraint, which makes the capacitor design easier for high frequency operation.

2.5 Conclusion and design objectives

Various architectures have been analyzed and compared toward the objective of maximizing the efficiency. Considerations on control were presented and

a control scheme selected, but no further investigations on this side are proposed in the presented work. A model of the technology was proposed and utilized to evaluate the selected one, and this analysis led to the idea of a three-MOSFETss cascode power stage. Output filter was then dimensioned based on classical considerations and validated using SPICE simulations. This section presents then the parts that are designed, along with the objectives associated with them. The choices have been guided by the several considerations developed in the previous sections.

2.5.1 Active parts

It has been chosen to focus on the power stage and the associated driving circuits. The analysis of the technology has shown that a power stage using three low-voltage MOSFETs in series instead of one high voltage device should provide a higher efficiency. In order to validate this, both structures are designed.

The architecture analysis also demonstrated the interest of the two phase approach. In order to validate this result, it is necessary to have several power cells, one optimized for a one-phase configuration and one for the two phase configuration, i.e. one for nominal load current and one for half the nominal current respectively.

As the two-phase structure is also expected to use coupled inductors and operate at lower frequency than the single phase configuration, they are designed for 100 MHz switching frequency (and 200 MHz for the single phase configurations).

Because of the limited silicon area available, it has been decided to have two similar silicon dice. The first contains all the circuits with a standard power stage, and the second one the circuits with the cascode power stage. Due to Inputs/Outputs (I/O) number limitation, it is decided to design only one phase of the two-phase converter. The two phase configuration is planned to be obtain using two dice, allowing for modular testing but probably higher parasitic values.

Here are the circuits that are designed:

- Power stage and driving circuit for a standard power stage using 3.3 V MOSFETs, optimized for 280 mA and 200 MHz switching frequency,

- Power stage and driving circuit for a standard power stage using 3.3 V MOSFETs, optimized for 140 mA and 100 MHz switching frequency,
- Power stage and driving circuit for a cascode power stage using 1.2 V MOSFETs, optimized for 280 mA and 200 MHz switching frequency,
- Power stage and driving circuit for a cascode power stage using 1.2 V MOSFETs, optimized for 140 mA and 100 MHz switching frequency.

2.5.2 Passive components

Capacitors are embedded on a passive interposer. Due to manufacturing constraints, one version only of the interposer has been available. This means that it should be pad compatible with all designed silicon chips. Furthermore, it must have enough decoupling capacitors to fit both converter structures. In addition to the capacitors, a landing pattern for the chip is required. A landing pattern for a commercial inductor is also added, in order to be able to test the assembly and compare the performance of the commercial inductor and the racetrack planar inductors. Here is the list of the elements specified for the interposer:

- One 4×4 pad matrix for IC connection,
- One 30 nF capacitor for main input decoupling,
- Three 10 nF capacitor for voltage references/driver supplies input decoupling,
- One 15 nF capacitor for output decoupling,
- One 0402 SMD landing pattern for output inductor.

Regarding the inductors, they have been specified based on dimensioning considerations developed previously. They are the followings:

- One 30 nH inductor for 200 MHz, single phase operation,
- Two 45 nH coupled inductors (0.35 coupling factor) for 100 MHz, two-phase operation,

- Two 35 nH coupled inductors (maximum possible coupling factor) for 100 MHz, two-phase operation,
- One 20 nH inductor for 100 MHz, two-phase operation (output inductor of tightly coupled structure).

All these parts are designed in parallel then fabricated with the dedicated technologies, and then assembled. This allows for individual testing and validation before the assembly, securing each design step.

Chapter 3

IC Design

Contents

This chapter details the design and optimization of the converters selected in the preceding chapter. The design steps are presented in a top-down approach, starting with a global system view, then detailing the sub-parts. The focus here is put on active parts of the converter. Capacitors design and magnetic inductors design are briefly presented in Section 4.2 and Section 4.3. Following the block design review, considerations on the layout are presented.

In the end, considerations on I/O pads and chip-level layout concerns are discussed.

3.1 Global system view

Even though four converters selected for fabrication, they all have the same global structure. The two major differences between them are the switching frequency (100 MHz and 200 MHz) and the type of power stage utilized (standard and cascode power stage).

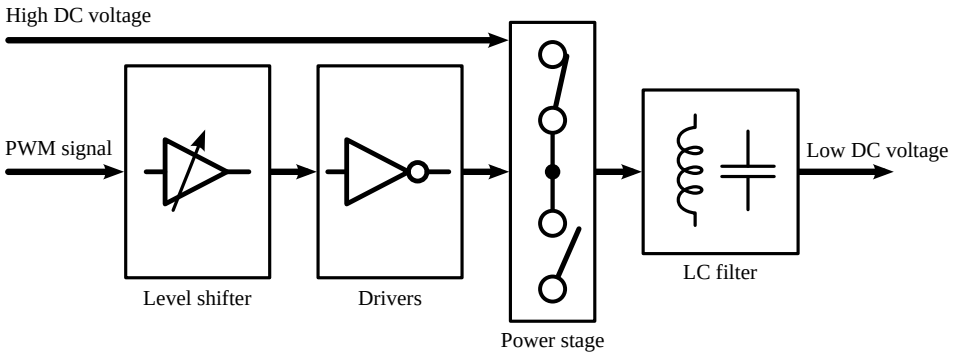


Figure 3.1 – Global system with building blocks.

Limitations in access to silicon forbids to reach a full converter system. The power stage is the focus here. A global view of the system is presented in Figure 3.1. It is built using four main parts: a level-shifter, the drivers, a power stage and the LC output filter. The level-shifter is here to adapt the voltage levels between the PWM input and the power stage. The drivers strengthen the driving signals before feeding it to the power stage. At the end the LC filter smooths the output voltage. The design of the LC filter is not presented here as it was carried out by industrial partners.

All these elements are different if the cascode power stage is considered or if the standard power stage is considered. The frequency optimization (100 MHz and 200 MHz) impacts the power stage and the drivers. A level-shifter operating at 200 MHz can easily operate at 100 MHz, making a dedicated design unnecessary.

The previously listed building blocks of the converter are detailed in the following section, starting from the output of the converter. These blocks are presented for the both standard and cascode converters.

3.2 Design details

3.2.1 Power stage

The main role of the power stage is to transfer the right amount of power from the main input to the output filter. Once the type of power stage is selected, the role of the optimization is to define the width of the power MOSFETs. In addition to the analytical optimization presented in Section 2.3, power stages have been optimized using the *Global Optimization* tool available in the Cadence design environment.

In a first approach, the drivers of the power stage have been modeled using an ideal driver structure, as depicted in Figure 3.2. This driver is constituted of two voltage-controlled current sources, with a feedback. Assuming a capacitive load (which is the case when driving the gate of a MOSFET) the output voltage V_{OUT} will tend to the input voltage V_{IN}. This driver uses two parameters: the saturation current to mimic the MOSFET saturation current and a transconductance value. It allows for evaluating the gate switching losses of the power stage. In all the considered cases, the saturation current has been set to 300 mA and the transconductance value to 1 S. These values have been chosen sufficiently high for small turn-on and turn-off times, but still realistic given the technology. They have however not been finely tuned as they do not impact much the gate losses.

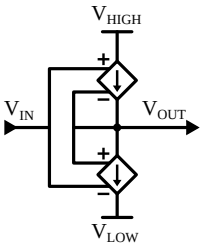


Figure 3.2 – Structure utilized for driver simulation.

3.2.1.1 Standard power stage

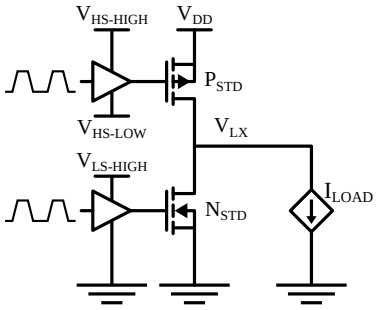


Figure 3.3 – Circuit for standard power stage optimization.

The standard power stage is built using two MOSFETs, one P-MOSFET for the high-side and one N-MOSFET for the low-side. The MOSFETs are 3.3 V standard devices using medium thickness oxide. The minimum MOSFET length is 400 nm. The circuit for optimization purposes is depicted in Figure 3.3. In addition to the power stage, it includes two drivers (the ones presented in Figure 3.2) four ideal DC voltage sources (one for the main input (V_{DD}), one for high-side high level ($V_{HS\text{-}HIGH}$), one for high-side low level ($V_{HS\text{-}LOW}$) and one for low-side high level ($V_{LS\text{-}HIGH}$)) two separate driving signals and a constant current load (emulating inductor current). Output inductance has been replaced by a current source as it allows to avoid the start-up transient burden, reducing the simulation time very effectively, which is critical in a global optimization due to the necessity to run a lot of simulation.

The values of V_{DD} and $V_{HS\text{-}HIGH}$ are fixed to 3.3 V. The load current, I_{LOAD}, is set to 280 mA for the one-phase configuration and 140 mA for the two-phase configuration. The optimization can adjust the value of the swing of both high-side and low-side drivers (by changing the $V_{HS\text{-}LOW}$ and the $V_{LS\text{-}HIGH}$ values), the width of both power transistors (P_{STD} and N_{STD}), the rising and falling delays (dead-time) of the low-side MOSFET and the duty cycle of the driving signals (to adjust the output voltage to the right value).

Two targets are defined for the optimization. First, the output voltage needs to be 1.2 V. In our case, the output voltage is calculated using the

average value of the V_{LX} voltage. A strong constraint on this value is defined, ensuring that it is between 1.1995 V and 1.2005 V. These values were arbitrary chosen to ensure an output voltage sufficiently close to the desired one. The second target of the optimization is to minimize the power drawn from each power supply. If the first constraint is enforced, minimizing the input power implies that the losses are minimized – the output power being constant as the output voltage and current are fixed.

The optimization was run several times with different starting points in order to evaluate the consistency of the results. Results were quite close to each other each time. A slight variation has been observed on the gate voltage swing and MOSFET width values across the several optimization results. This variation had no impact on the efficiency figure, meaning that several quasi-optimized configurations exist.

Table 3.1 – Optimization results for 100 MHz and 200 MHz configurations.

Frequency (MHz)	100			200		
Load current (mA)	70	140	280	70	140	280
High-side gate swing (V)	1.9	1.85	1.95	2.05	1.85	2
High-side FET width (mm)	3.7	7.3	15.3	2.59	7.4	10.2
Low-side gate swing (V)	1.8	1.8	1.7	1.8	1.55	1.65
Low-side FET width (mm)	2.5	4.8	11.4	1.34	4.5	7.7
N-driver rising delay (ps)	180	185	185	120	170	160
P-driver falling delay (ps)	0	5	10	0	20	10
Power stage efficiency (%)	85.7	85.9	85.5	80.2	80.1	80.1

The optimization results are summarized in Table 3.1. The standard power stage has been optimized at 100 MHz and 200 MHz for three load currents: nominal load, half nominal load and one fourth of the nominal load. These cases would respectively be the one-phase, two-phase and four-phase architectures – a four-phase design is not planned in this work.

The optimum gate voltage swing is around 2 V for the P-MOSFET and 1.7 V for the N-MOSFET. MOSFET width is almost proportional to the load

current. Width of P-MOSFET is approximately 1.5 times larger than N-MOSFET while being almost 3 times more resistive. This dissimilarity is explained by the fact that the P-MOSFET conducts less time than the N-MOSFET (as the duty cycle is below 0.5) therefore RMS current is reduced, and so are losses. Power stage efficiency is constant across all load currents, and only varies with the switching frequency.

Based on the optimization results and on some practical considerations, design values have been chosen. The gate voltage swing has been fixed to the same value for both high side and low side switch in order to ensure a better matching of the two driver lines. This increases a bit the drivers' losses of the low-side MOSFET, but decreases also its conduction losses. Overall impact is a limited decrease of global efficiency (less than 0.2 %). Furthermore, width values have been rounded to be easily divisible in smaller identical part in order to ease the layout step. Delay values are taken into account in the design of the drivers. Chosen design values are summarized in Table 3.2.

Table 3.2 – Selected design values for standard power stage.

Frequency	(MHz)	100	200
Load current	(mA)	140	280
High-side gate swing	(V)	2	2
High-side FET width	(mm)	7.2	10.2
Low-side gate swing	(V)	2	2
Low-side FET width	(mm)	5.4	7.65

3.2.1.2 Cascode power stage

The same optimization flow as the one previously presented has been utilized for the cascode power stage. The circuit used for optimization is depicted in Figure 3.4. It is built using digital core devices of the technology (thin gate oxide and 40 nm minimum channel length) that are rated for 1.2 V. It includes four voltage sources (main DC input, 3.3 V, 2.2 V and 1.1 V sources for the drivers) and six ideal drivers. Transistors P_{P1}, P_{P2}, P_{P3} and N_{P1}, N_{P2}, N_{P3}

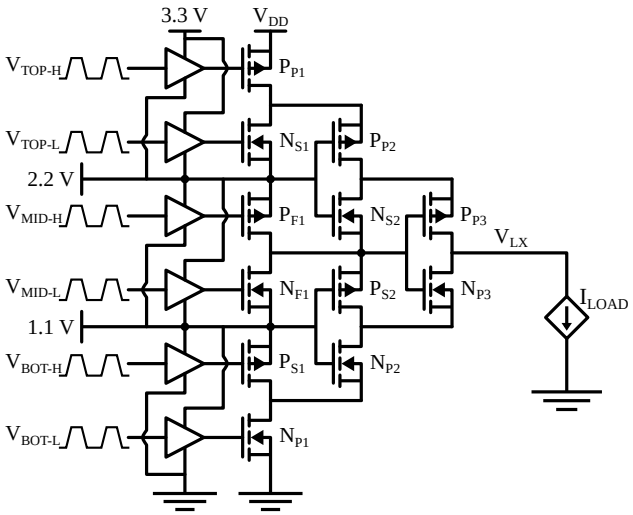
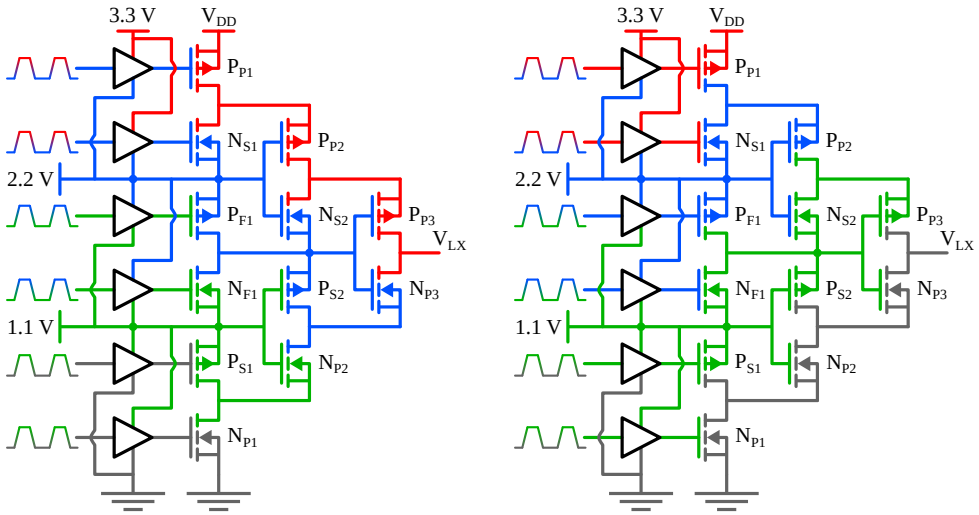


Figure 3.4 – Circuit for cascode power stage optimization.

are acting as high-side and low-side power switches respectively. The cascode structure allows for equal distribution of the voltage stress across the three power devices. Transistors N_{S1} and N_{S2} guarantee that the devices P_{P2} and P_{P3} are properly turned-off when the low side branch is turned-on, ensuring an equal voltage stress across the branch $P_{P1\text{-}P2\text{-}P3}$. Transistors P_{S1} and P_{S2} have an equivalent role for the $N_{P1\text{-}P2\text{-}P3}$ branch. Inverter P_{F1}-N_{F1} generates the proper voltage for driving the gate of P_{P3} and N_{P3}, so that their gate-to-source and gate-to-drain voltages never exceed 1.1 V. The two switching states of the power stage in CCM are depicted in Figure 3.5. In Figure 3.5a the high-side branch is turned-on, and the low-side branch is turned-on in Figure 3.5b. The selected cascode power stage structure does not allow for DCM operation as gates of P_{P3} and N_{P3} are connected together so they can't be "off" at the same time. Only CCM-operated power stage is then considered. As a DCM-capable power stage would be more complex, restriction to the CCM-operated one is made to secure the design and limit the complexity for the first design run.

Optimization targets are the same as in the case of the standard power stage: 1.2 V output voltage and minimum total input power – calculated as the average of the products of voltage and current of each source. Constraints have been set on the power MOSFETs: P_{P1}, P_{P2} and P_{P3} are identical, as well



(a) Cascode power stage in phase 1 of switching operation in CCM.

(b) Cascode power stage in phase 2 of switching operation in CCM.

Figure 3.5 – Cascode power stage in its two switching states.

as N_{P1}, N_{P2} and N_{P3}. N_{S1} and N_{S2} are also constrained to be identical, as well as P_{S1} and P_{S2}. The reference driving signal is $V_{TOP\text{-}H}$, and rising and falling edges of all other signals can vary independently. Due to the higher number of driving signals and MOSFETs to optimize, optimization of this structure required longer simulation time than for the standard power stage, implying that less optimization runs were possible.

Cadence optimization results on cascode power stage are summarized in Table 3.3 and Table 3.4 for 100 MHz and 200 MHz respectively. A major difference with the standard power stage is that optimum width of the power transistors increases but is not proportional to the load current. This observation could be explained by the fact that gate capacitance is impacted by drain-to-source current because of short-channel effects. However efficiency of the power stage is not impacted by the load current. Widths of $N_{S1\text{-}S2}$ and $P_{S1\text{-}S2}$ do not seem to be critical parameters. These MOSFETs need too be large enough to operate fast, but not to large as it would increase switching losses.

Table 3.3 – Optimization results for the 100 MHz configurations.

Frequency	(MHz)	100		
Load current	(mA)	70	140	280
$P_{P1\text{-}P2\text{-}P3}$ width	(mm)	9.6	12.4	21.2
$N_{P1\text{-}P2\text{-}P3}$ width	(mm)	3.4	5.4	10
$N_{S1\text{-}S2}$ width	(mm)	0.5	0.5	0.5
$P_{S1\text{-}S2}$ width	(mm)	2	2.5	3.1
P_{F1} width	(mm)	0.5	0.79	0.79
N_{F1} width	(mm)	0.32	0.5	1.2
$V_{TOP\text{-}H}$ rise/fall delay	(ps)	0/0	0/0	0/0
$V_{TOP\text{-}L}$ rise/fall delay	(ps)	235/-20	245/-15	225/-25
$V_{MID\text{-}H}$ rise/fall delay	(ps)	0/0	0/0	0/0
$V_{MID\text{-}L}$ rise/fall delay	(ps)	185/-55	120/-55	115/-50
$V_{BOT\text{-}H}$ rise/fall delay	(ps)	0/0	0/0	0/0
$V_{BOT\text{-}L}$ rise/fall delay	(ps)	420/-5	290/-5	265/-10
Power stage efficiency	(%)	91.7	92.0	91.7

Selected design values following the optimization of cascode power stage are presented in Table 3.5. Values have been rounded for easier implementation. $N_{S1\text{-}S2}$, $P_{S1\text{-}S2}$, P_{F1} and N_{F1} in the 100 MHz configuration are chosen to be the same as in the 200 MHz configuration. No significant impact on the power stage behavior and efficiency has been observed following this decision. Delay values are taken into account in the design of the drivers.

Table 3.4 – Optimization results for the 200 MHz configurations.

Frequency (MHz)	200		
Load current (mA)	70	140	280
$P_{P1\text{-}P2\text{-}P3}$ width (mm)	6.2	6.8	14.2
$N_{P1\text{-}P2\text{-}P3}$ width (mm)	2.1	3.6	6
$N_{S1\text{-}S2}$ width (mm)	0.5	0.5	0.5
$P_{S1\text{-}S2}$ width (mm)	1.3	1.8	3.6
P_{F1} width (mm)	0.36	0.7	0.7
N_{F1} width (mm)	0.26	0.36	0.96
$V_{TOP\text{-}H}$ rise/fall delay (ps)	0/0	0/0	0/0
$V_{TOP\text{-}L}$ rise/fall delay (ps)	160/-10	105/-10	125/-40
$V_{MID\text{-}H}$ rise/fall delay (ps)	0/0	0/0	0/0
$V_{MID\text{-}L}$ rise/fall delay (ps)	110/-25	60/-25	75/-45
$V_{BOT\text{-}H}$ rise/fall delay (ps)	0/0	0/0	0/0
$V_{BOT\text{-}L}$ rise/fall delay (ps)	200/-10	150/-10	170/-15
Power stage efficiency (%)	88.2	88.3	88.1

Table 3.5 – Selected design values for cascode power stages.

Frequency (MHz)	100	200
Load current (mA)	140	280
$P_{P1\text{-}P2\text{-}P3}$ width (mm)	12.6	14.88
$N_{P1\text{-}P2\text{-}P3}$ width (mm)	5.4	6.36
$N_{S1\text{-}S2}$ width (mm)	0.9	0.9
$P_{S1\text{-}S2}$ width (mm)	2.88	2.88
P_{F1} width (mm)	2.88	2.88
N_{F1} width (mm)	1	1

3.2.2 Drivers

Drivers of the power MOSFETs are playing a key role in the timing of the driving signals. Optimization results of the power stages previously presented have shown that some delays on rising and/or falling edges of several driving signals need to be controlled in order to get maximum efficiency. The absence of a proper delay could lead to short-circuit current spike in the power stage.

3.2.2.1 Delay control

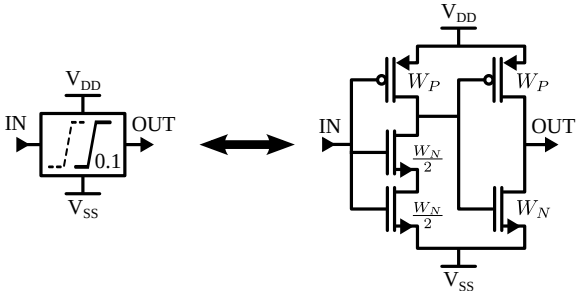


Figure 3.6 – 100 ps rising edge delay cell symbol (left) and schematic (right).

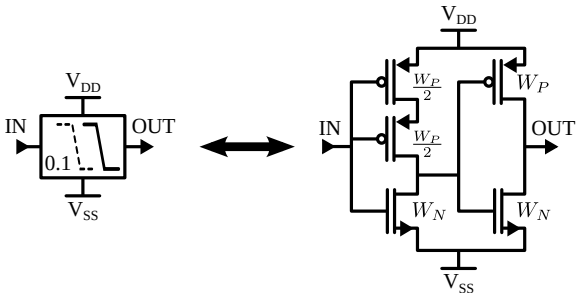


Figure 3.7 – 100 ps falling edge delay cell symbol (left) and schematic (right).

These delays are generated using asymmetric inverters. In order to ease design, similar delay cells have been designed for both standard and cascode power cell. The difference is in the chosen transistor type (3.3 V devices for standard power stage an 1.2 V devices for cascode power stage) and on the

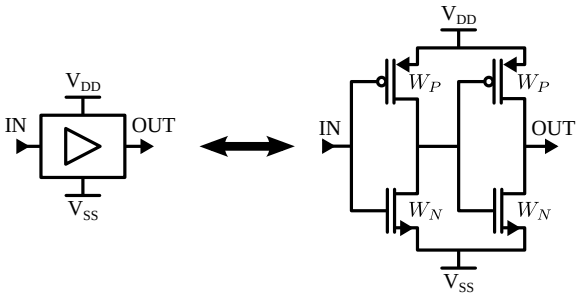


Figure 3.8 – No-delay cell symbol (left) and schematic (right).

W_P/W_N ratio. For the 3.3 V devices, this ratio is equal to 3, and for the 1.2 V devices it is equal to 2. Delay is applied on rising and/or falling edge by using an N-MOSFET or P-MOSFET that has a W/L ratio four times smaller than in a well balanced inverter.

Three primary cells have been designed in order to generate the proper delay values. The first one (depicted in Figure 3.6) generates a 100 ps delay on the rising edge of the signal. The second one (depicted in Figure 3.7) generates a 100 ps delay on the falling edge of the signal. The last one (depicted in Figure 3.8) generates no delay on both edges, but is necessary to compensate for the propagation time through the two previous cells – e.g. when having two driver lines and only one line requires a delay on a rising/falling edge. These three cells have an equal input capacitance and drive strength, making them interchangeable. These cells can also operate inside any voltage domain.

Two other cells have been built based on the former three cells. These cells are delaying either rising or falling edge of a signal relatively to an other one. They are depicted in Figure 3.9 and Figure 3.10.

In addition to these elementary delay cells, an input buffer for the driver line has been designed. This buffer is depicted in Figure 3.11. It is built using tapered, balanced inverters. The purpose of this is to provide easier and less variable and a more systematic design of the driver lines. Using this cell ensures that the input capacitance of the driver line is well controlled.

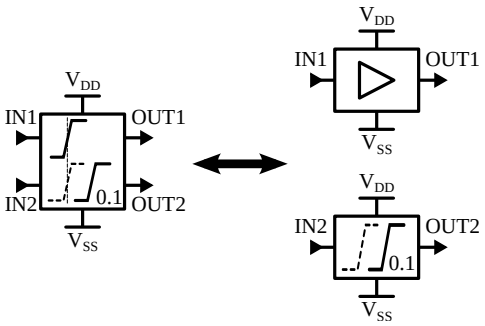


Figure 3.9 – Relative 100 ps rising edge delay cell symbol (left) and building blocks (right).

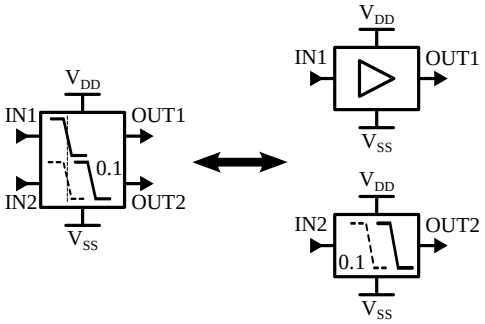


Figure 3.10 – Relative 100 ps falling edge delay cell symbol (left) and building blocks (right).

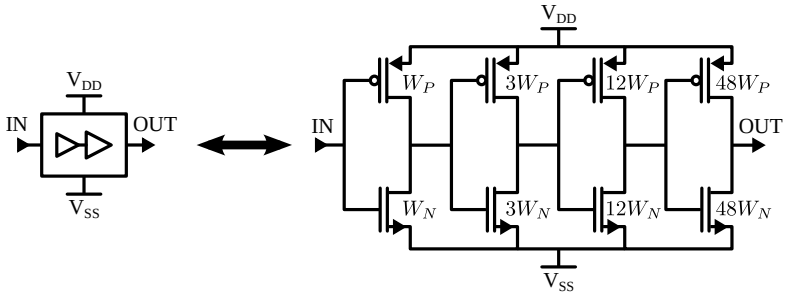


Figure 3.11 – Input buffer of a driver line.

3.2.2.2 Drivers of the standard power stage

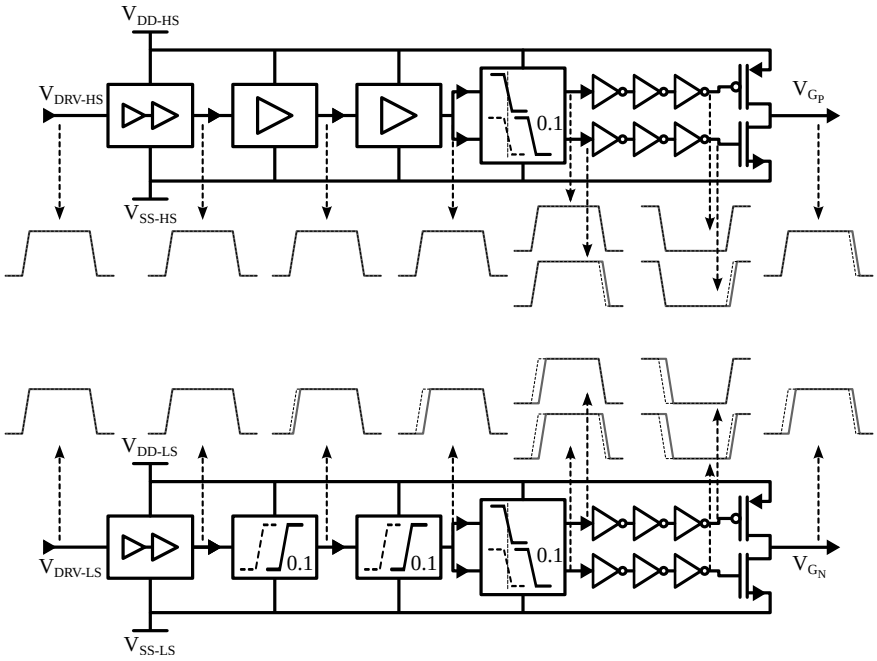


Figure 3.12 – Drivers of the standard power stages.

Full structure of the drivers for the standard power stage is depicted in Figure 3.12. The same structure is utilized for both the 100 MHz and the 200 MHz configurations. It has been chosen that the last drivers of the driver lines have separated inputs for their P-MOSFET and N-MOSFET in order to avoid any short-circuit current through these two large inverters. Delay is chosen according to optimization results presented in Table 3.1. N-driver rising delay is rounded to 200 ps and no delay is added for the P-driver falling edge.

The three inverters following the relative delay cells are balanced tapered buffers. They ensure that the drivers deliver a strong driving signals to the power MOSFETs. Their width increases regularly. A tapering factor of approximately 3.8 has been chosen. This value is an acceptable trade-off between propagation time and losses of the driver line [Hed94].

3.2.2.3 Drivers of the cascode power stage

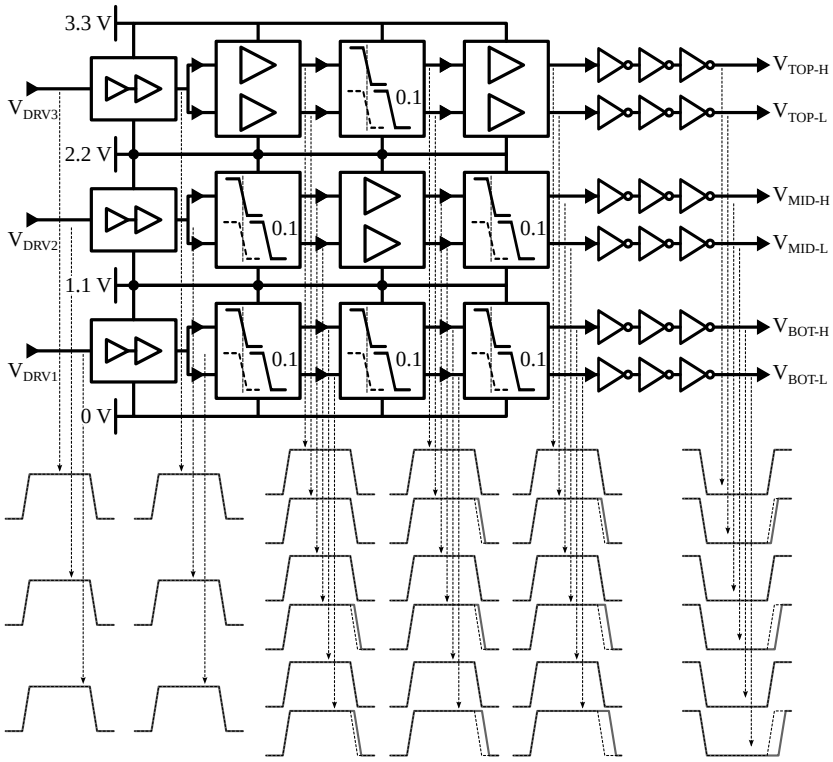


Figure 3.13 – Drivers of the 100 MHz cascode power stage.

The drivers of the cascode power stage are implemented similarly to the drivers of the standard power stage. The designed driver lines are presented in Figure 3.13 and Figure 3.14 for the 100 MHz and the 200 MHz configurations respectively. Delays are chosen based on results presented in Table 3.3 and Table 3.4. The 100 MHz requires more delay cells than the 200 MHz as the current is also lower, meaning that parasitic capacitances discharge requires more time.

The drivers are designed using three "stacked" power supplies. Using these supplies ensures that no inverter suffers more than 1.1 V, allowing to use core devices in the driver lines. As a result, all transistors utilized in the driver line for the cascode power stages are low-voltage devices (1.2 V). Using these

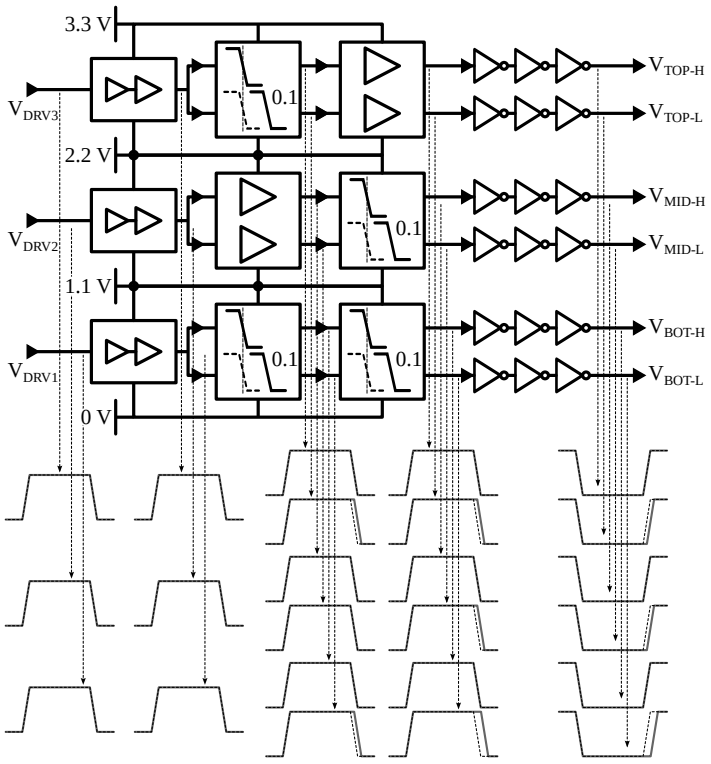


Figure 3.14 – Drivers of the 200 MHz cascode power stage.

devices makes the driver lines more efficient as these transistors have a smaller gate capacitance than the 3.3 V devices.

3.2.3 Level-shifter

The presented driver lines are working properly only if properly synchronized signals are present at their inputs. A level-shifter is then necessary to generate the required driving signals at the appropriate voltages and timing accuracy. Level-shifting circuits ad techniques are well used in digital circuits where several voltage domain are present [Hen07; Wan02; Cha84]. The level-shifter must operate at 200 MHz and be able to output a minimum pulse width of 1 ns. Furthermore the relative timing delay between the output signals needs to be negligible, i.e. no more than few tens of pico-seconds. In the end, the power

consumption of the level-shifter should also not impact the efficiency of the converter. In terms of implementation, only 3.3 V MOSFETs are considered as voltages inside the level-shifter are expected to be above 1.2 V.

Following these considerations, two structures for the level-shifter have been investigated. These structures are a latch-based circuit and a comparator based circuit.

3.2.3.1 Latch-based level-shifter

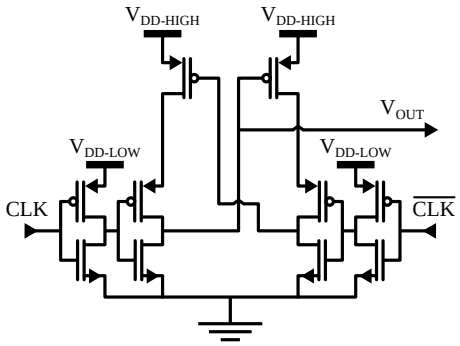


Figure 3.15 – Latch-based level-shifter schematic.

The latch-based circuit is depicted in Figure 3.15. It requires two complementary clock signals at the input. Amplitude of the inputs is between 0 V and $V_{DD\text{-}LOW}$. The amplitude of the output signal is between 0 V and $V_{DD\text{-}HIGH}$. A similar structure can be used to change the lower voltage level.

One of the advantages of this structure is that there is no DC power consumption. It can also propagate fairly small pulses. However speed (i.e. propagation time and resulting rising and falling times) is very dependent on the voltage and size of the devices. For instance using 3.3 V devices to generate a signal with an amplitude of 1.1 V (in the case of the cascode power stage) makes this circuit not very fast. Furthermore using this structure to generate all required driving signals would require several blocks, operating at different voltages, so propagation delays would not be identical depending on the voltage domain. Delays should be added using several inverters on one voltage

domain in order to be synchronized with the other voltage domain. This technique can work quite well in simulation, but after implementation it wouldn't be precise due to process variability – as the delay of an implemented inverter can not be guaranteed to be exactly the same as in simulation.

Because of the lack of proper delay control that could lead to severe issues on the cascode power stage, this structure has not been selected for implementing the level-shifter.

3.2.3.2 Comparator-based level-shifter

A comparator-based level-shifter is selected in order to address the shortcomings of the latch-based structure. The structure is built around a differential pair and current mirrors. The differential pair acts as a comparator and depending on its state, a current is mirrored through the chosen branch allowing for charging or discharging MOSFET gates.

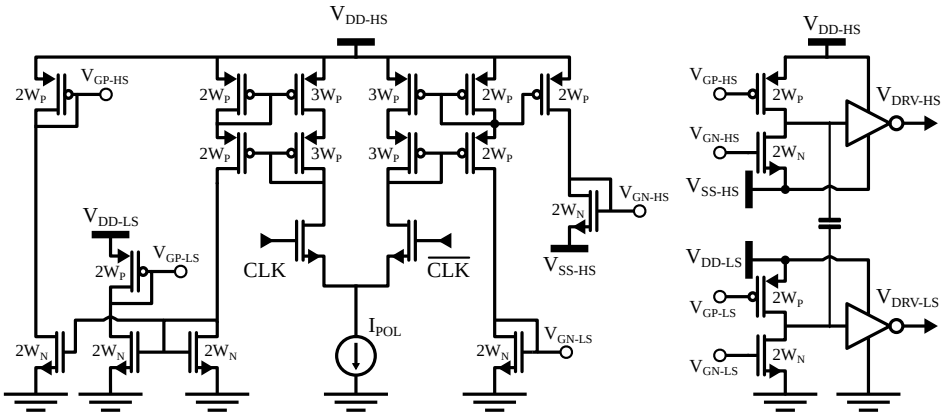


Figure 3.16 – Comparator-based level-shifter for the standard power stage.

The circuit designed for the standard power stage is depicted in Figure 3.16. The associated waveforms are depicted in Figure 3.17. When the voltage at the CLK input is higher than the one at the $\overline{\text{CLK}}$ input, most of the current goes through the left side of the circuit. Current is then mirrored through the P-MOSFET at the input of the inverters, charging the gates of the P-MOSFETs and the N-MOSFETs, making the outputs ($V_{DRV\text{-}HS}$ and $V_{DRV\text{-}LS}$) switch to a low value.

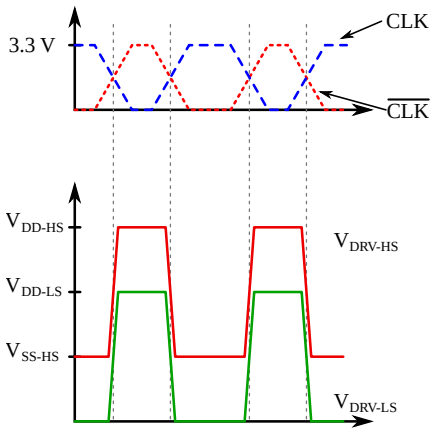


Figure 3.17 – Waveforms of the comparator-based level-shifter for the standard power stage.

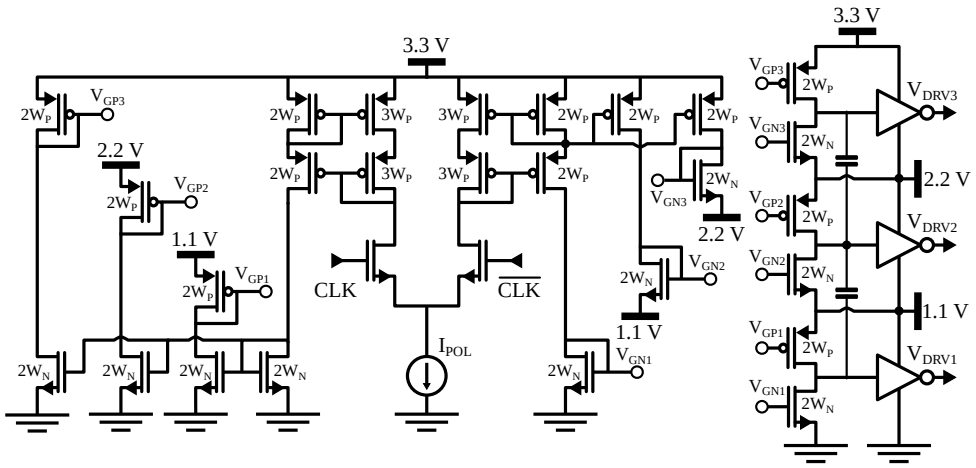


Figure 3.18 – Comparator-based level-shifter for the cascode power stage.

For the cascode power stage, the same structure is utilized. The full circuit is depicted in Figure 3.18 and the waveforms in Figure 3.19. The circuit has three outputs (V_{DRV1}, V_{DRV2} and V_{DRV3}) and voltages are stacked. It behaves in the same manner as the level-shifter for the standard power stage.

For both circuits (Figure 3.16 and Figure 3.18), current mirroring doesn't

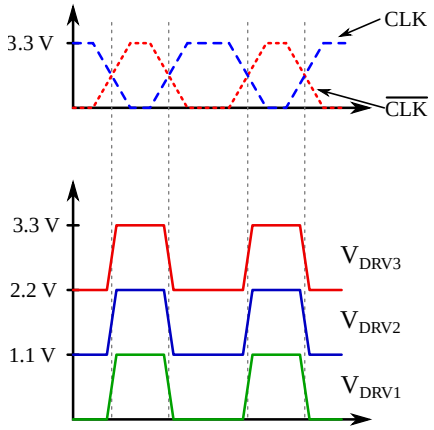


Figure 3.19 – Waveforms of the comparator-based level-shifter for the cascode power stage.

need to be precise in absolute value to have properly timed output signals. The key point to ensure is that the mirroring is the same across the two voltage domains. A design with sufficient matching should achieve this. In order to counterbalance any parasitic mismatch in the mirrors, small floating capacitors (approximately 90 fF in Figure 3.16 and two times 28 fF in Figure 3.18) have been added to force crosstalk effects between the output inverters.

Figure 3.20 shows the input and output waveforms of the level-shifter of the cascode power stage (Figure 3.18). Output voltage is shown for the two cases: with and without the two floating capacitors (28 fF) at the level-shifter output. A better synchronization is seen when the floating capacitors are present. A delay of approximately 1 ns is observed from the input to the output.

The downside of this structure is that it requires a DC current source, which adds a DC power consumption. There is also a trade-off between circuit speed, power consumption and area – and more area allows for better matching. In order to get high-speed behavior, either MOSFETs are designed very small (leading to small parasitic capacitances) or current is set to a relatively high value (allowing for fast charging and discharging of parasitic capacitances). The issue is that small MOSFETs makes matching difficult and high current increases the power consumption.

It has been decided to use small MOSFETs (minimum length, 400 nm)

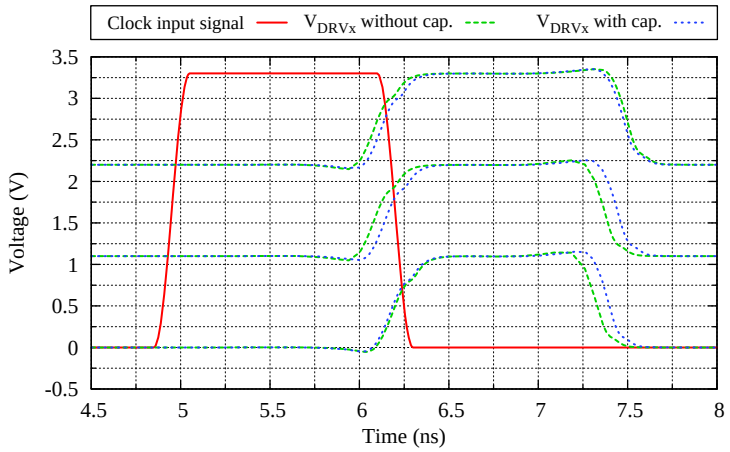


Figure 3.20 – Three-output level-shifter waveforms with and without floating capacitors.

and small polarization current. However the MOSFETs are not too small in order to ease the matching by using identical unit cells, and at least two unit cells per MOSFET. The unit width of the P-MOSFETs (W_P) is fixed to 1 µm and the unit width of the N-MOSFETs (W_N) to 600 nm for both level-shifters (Figure 3.16 and Figure 3.18). With these values, timing performance is achieved with a polarization current (I_{POL}) equal to 40 µA approximately, leading to a total power consumption of 350 µW for both configurations. Minimum pulse width achievable with this current is 900 ps and maximum skew between signals is 40 ps, which are both acceptable values for proper power stage driving.

3.2.4 Current reference

The designed level-shifter requires a current reference. The circuit proposed in [Ogu97] is selected as it features low sensitivity with respect to technology and temperature. Furthermore it is auto-biasing, meaning that no start-up circuitry is necessary.

The designed circuit is depicted in Figure 3.21. It only requires a power supply, and the circuit sinks a constant current through transistor N_4. The

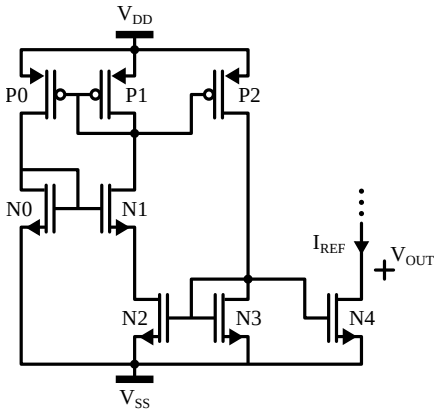


Figure 3.21 – Current source circuit.

MOSFET sizes are summarized in Table 3.6. The same current source is utilized for both the cascode and the standard converter.

Table 3.6 – Design values for the current source.

	P0	P1	P2	N0	N1	N2	N3	N4
Width (µm)	0.5	0.5	1	2	8	0.5	0.5	12
Length (µm)	3.2	3.2	3.2	0.4	0.4	12.8	12.8	1.6

The circuit creates a 44 µA current sink and draws only 420 nA from the V_{DD} power supply. The supply voltage is equal to 3.3 V. The current gain from N3 to N4 is equal to 192. Current sink capability has been simulated for various V_{OUT} voltages (from 0.5 V to 3.3 V) and various temperatures (from 0 °C to 125 °C). Simulation results are presented in Figure 3.22.

Current at the output of the current source is sufficiently stable when varying the voltage as ±5 % maximum variation is observed when varying the voltage. The output current is also hardly affected by temperature: from 0 °C to 125 °C the variation of less than 4 %.

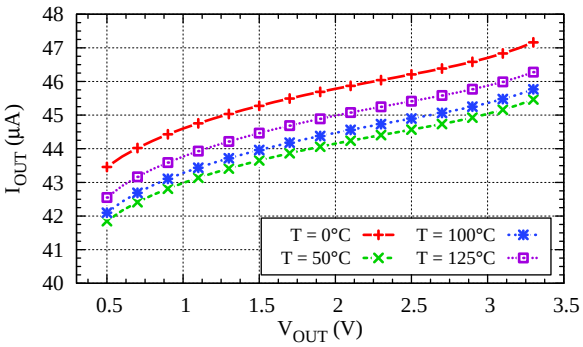


Figure 3.22 – Current source simulation over several output voltages and temperatures.

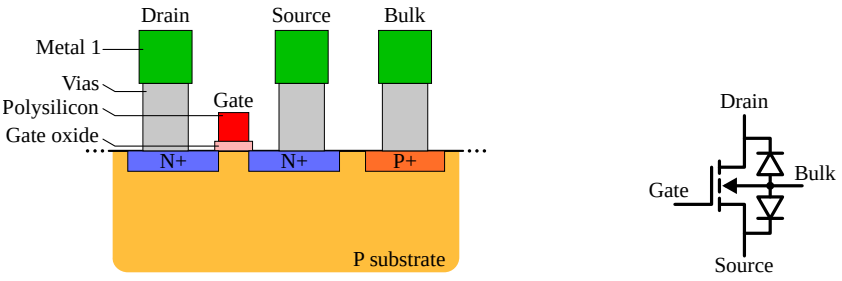
3.3 Cell design layout considerations

This section presents several important layout issues that are considered during the design. As some considerations apply to several cells, this section doesn't follow a cell by cell structure, but rather focuses on important layout considerations and then presents the cells impacted by these considerations.

Three major devices are utilized for the implementation (regardless of the voltage rating): the N-MOSFET, the P-MOSFET and the N-MOSFET in an Active Well (AW). Cross-sections of these structures are presented in the following paragraphs. Schematics are based on 1.2 V devices size but are willingly not on scale as lengths have been adapted for simplification purposes.

The cross-section of an N-MOSFET is depicted in Figure 3.23a. As the substrate is P-type doped, it simply consists of two N+ zones for the drain and source contacts. Bulk is directly connected to the substrate, so its potential can not differ from the substrate potential. The equivalent electrical circuit of the transistor structure is presented in Figure 3.23b. The bulk contact creates two junctions, between bulk and drain and between bulk and source.

The cross-section of a P-MOSFET is depicted in Figure 3.24a. As the substrate is P-type doped, it requires an N-well for the P-MOSFET body. In this N-well, two P+ zones are added for the drain and source contact. The bulk is connected with an N+ zone on the N-well. The equivalent electrical

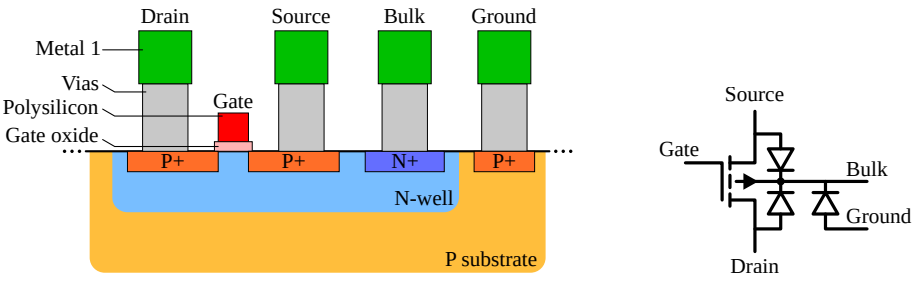


(a) Cross-section of a N-MOSFET.

(b) Equivalent circuit of a N-MOSFET.

Figure 3.23 – N-MOSFET structure.

circuit of the transistor structure is presented in Figure 3.24b. Using an N-well creates a parasitic junction between the substrate (P-type) and the bulk (N-type). As the body voltage of the P-MOSFET is usually higher than the substrate, the parasitic junction is reversed-biased, so it has no impact on the circuit behavior.



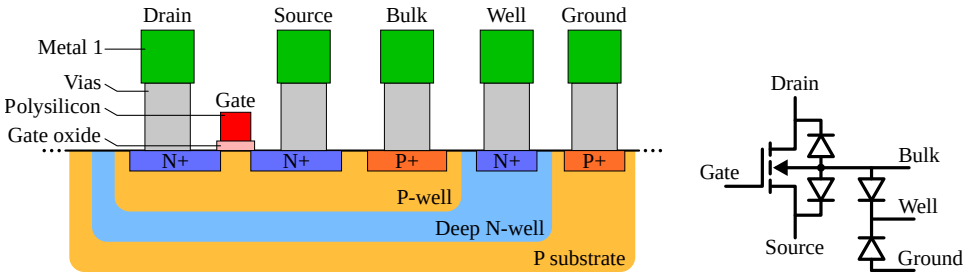
(a) Cross-section of a P-MOSFET.

(b) Equivalent circuit of a P-MOSFET.

Figure 3.24 – P-MOSFET structure.

The last structure is an N-MOSFET with Active Well (AW). The objective of this structure is to have an N-MOSFET with a bulk voltage different than the voltage of the substrate. This is achieved by using a P-well inside a deep N-well. The structure is depicted in Figure 3.25a. Inside the P-well, the N-MOSFET AW behaves in the same way as the regular N-MOSFET. Using the

P-well and the deep N-well adds an electrode (N-well contact) to the MOSFET structure, as well as two parasitic junctions (one between N-MOSFET body and deep N-well and one between substrate and deep N-well). The equivalent circuit of the structure is presented in Figure 3.25b. The voltage applied on the deep N-well electrode should always be equal or higher than the voltages of both the transistor body and the substrate. A classical approach is to fix this voltage to the highest voltage available on the chip, ensuring that the two parasitic junctions are reversed biased.



(a) Cross-section of an N-MOSFET AW.

(b) Equivalent circuit of an N-MOSFET AW.

Figure 3.25 – N-MOSFET AW structure.

All presented structures are available as 1.2 V and 3.3 V devices. The difference between theses two devices are the minimum gate length and the gate oxide thickness. Figure 3.26 presents a 3.3 V N-MOSFET. Compared to Figure 3.23a, gate is longer and oxide is thicker.

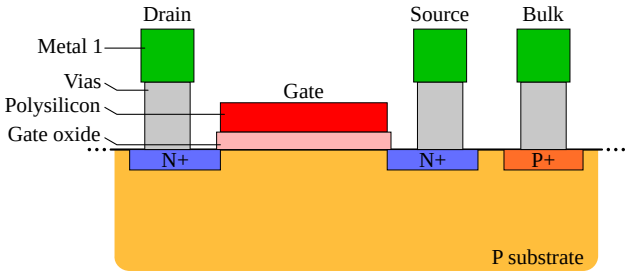


Figure 3.26 – Cross-section of a 3.3 V N-MOSFET.

3.3.1 On-chip switching noise

High frequency switching of large transistors with high switched current generates parasitic voltages and currents, that can be assimilated to an electrical noise. This noise is a critical issue as it can for instance disturb adjacent circuits or induce substrate current, which can in return generate latch-up issues [Gre73]. Layout needs to be mitigated with the objective to avoid these issues.

The use of guard-rings is a common approach for addressing this kind of issues. The objective is to ensure that any generated parasitic current can be captured by a low impedance path to ground or a voltage source. So any potential source of parasitic current should be enclosed inside a guard-ring, as well as sensitive circuit part.

In the case of active well design, layout is even more critical as the stacking of deep N-well and P-well on top of the P-substrate creates a parasitic PNP bipolar transistor.

3.3.1.1 Classical guard-ring approach

A classical guard-ring approach is to enclosed the N-MOSFET region inside a P+ diffusion connected to ground, and the P-MOSFET region inside an N+ diffusion connected to power supply. A cross-section and top view of P-MOSFET and N-MOSFET with guard-rings are presented in Figure 3.27. The guard-ring GR-0 is connected to the N-MOSFET body, and usually tied to the source of the transistor (or to a lower voltage value). The guard-ring GR-1 is connected to the P-MOSFET body, which is also usually connected to the source of the transistor (or to a higher voltage). Guard-ring GR-0 of the N-MOSFET is also utilized as a second guard-ring of the P-MOSFET, shielding the N-well of the possible perturbation from the ground. This makes the protection less area consuming.

The guard-ring should be connected to a reference voltage with a low impedance path in order to ensure a proper protection. Guard-ring width can be adjusted depending on the amount of current it could see. In the case of large MOSFETs, an important guard-ring is recommended.

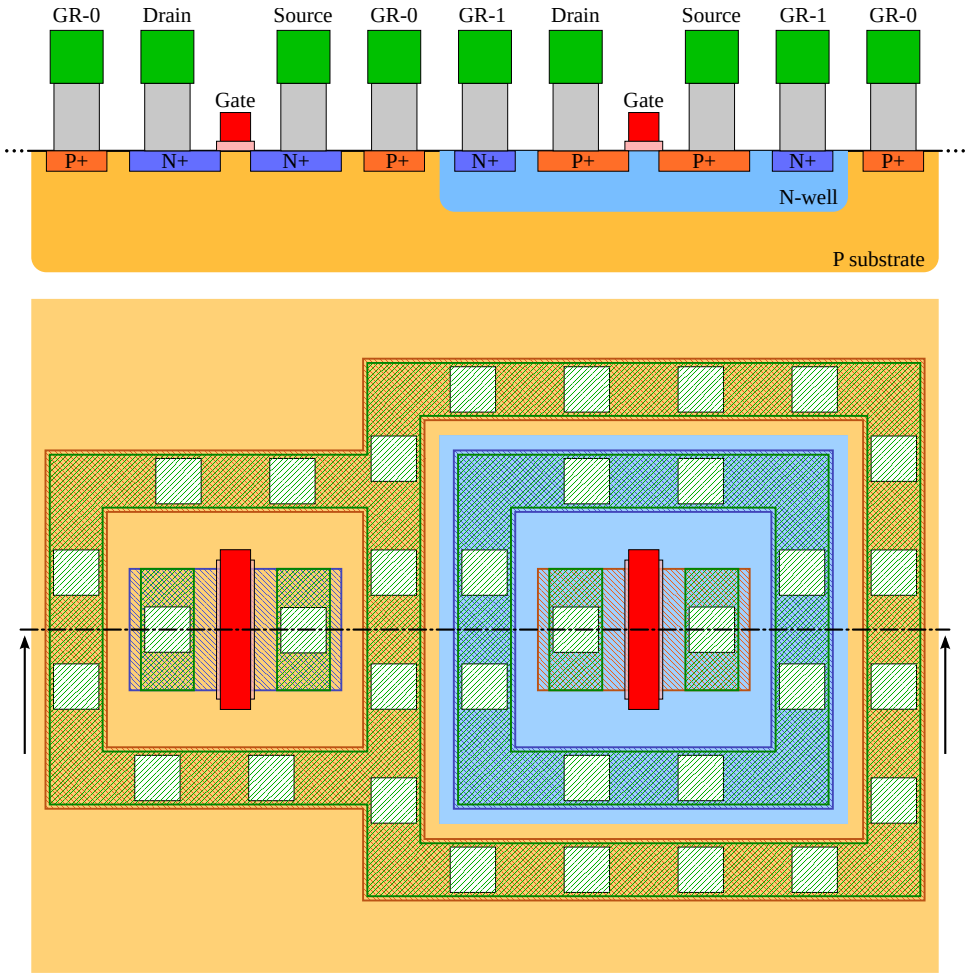


Figure 3.27 – Guard-ring protection scheme for P- and N-MOSFETs cross-section and top view.

3.3.1.2 Active-well guard-ring approach

In the active-well structure, having a good isolation between MOSFET body and substrate is critical for the correct behavior of the cascode power stage. In this power stage, each MOSFET has its source connected to the bulk, which is at a different potential than the ones of IC substrate. The deep N-

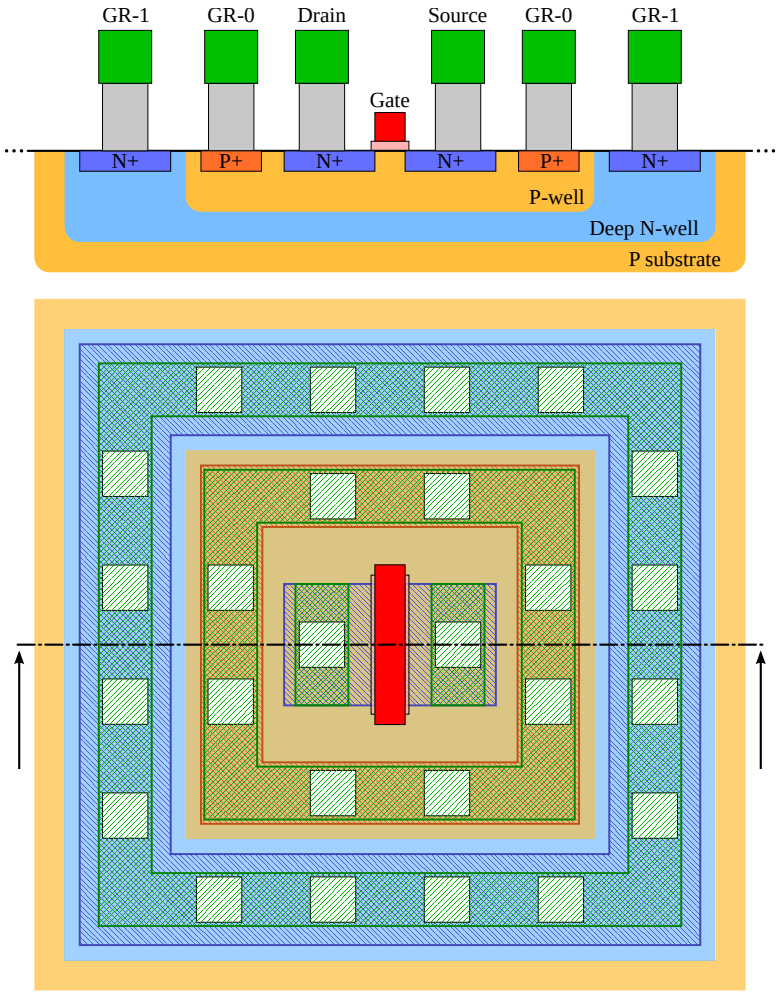


Figure 3.28 – Guard-ring protection scheme for N-MOSFET in active well cross-section and top view.

well ensures this isolation. However its must be connected to a high voltage through a low impedance path. This is achieved by using a supplementary guard-ring connected to the deep N-well all around the MOSFET.

In the circuit design, all deep N-wells have been connected to 3.3 V. This value has been chosen for two main reasons. The first one is that it provides a reliable protection by polarizing any parasitic junction in reverse bias as

this is the highest voltage of the circuit. The second reason is that it should reduce the wells' parasitic capacitances by increasing the Space-Charge Region (SCR) (also called the depletion region). Switching should then be less lossy as capacitance values are decreased. However, no impact of the deep N-well voltage value has been seen in simulation. The models probably doesn't take into account this effect.

Having these guard-rings is area consuming, especially when following design recommendation as guard-rings' width and spacing are in the order of few micro-meters. In designs where area is a concern some techniques can be used to limit the impact of guard-rings, e.g. associating guard-rings of P-type and N-type devices. As the presented design is not area constrained, no specific area reduction method has been used.

3.3.2 Parasitic capacitance and resistance of metal routing

Large P- and N-MOSFET are implemented as multi-fingers structures. The structure is presented in Figure 3.29 for a N-MOSFET. Having fingers in parallel creates an alternating disposition of source and drain contacts. All the following considerations assume such a layout.

Using multi-fingers MOSFET makes the current flowing in two directions inside the MOSFET. In Figure 3.29, current (represented using dashed lines in the cross-section) is flowing from drain to source. From the gate perspective, current flows either from left to right or from right to left. This behavior has an impact on matching, which is discussed in Part 3.3.3.

In terms of drain and source contacts, this structure is quite area efficient as drain and source contacts of parallel fingers are shared. In the chosen implementation, and for practical design issues, the outer contact is always a source contact. This implies that the full structure always has one more source contact than the number of drain contacts, making the access path of the MOSFET not symmetrical. However due to the very high number of fingers per MOSFET cell (around a hundred) the asymmetry does not have much impact. To simplify any further calculation, the numbers of drain and source contacts is considered to be half the number of gate fingers in calculations involving metal resistance – meaning that one source contact finger is not accounted for.

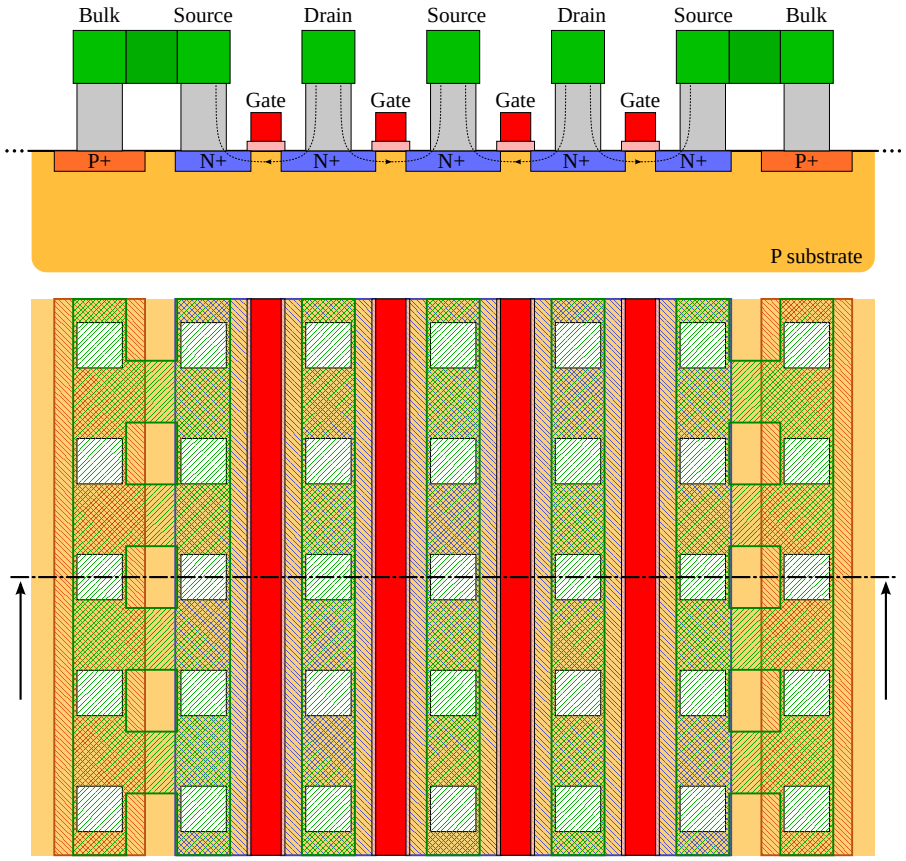


Figure 3.29 – Layout of a N-MOSFET using multiple parallel fingers.

3.3.2.1 Metal stack parasitic elements

Routing and layout of power MOSFETs mostly consists of placing vias and metal lines to get the current flow in and out of the chip. Available metal layers are fixed for a given technology. In this case, eight metal layers are available. The metal stack is depicted in Figure 3.30. The first five metal layers (M1, M2, M3, M4 and M5) have the same characteristics, and then metal is getting increasingly thicker (M6, M7 and M8). Adjacent metal layers are connected using vias (from V0 to V7). Dimensions of the vias follow those of the metal layers: the first five (V0 to V4) are identical, and the last three

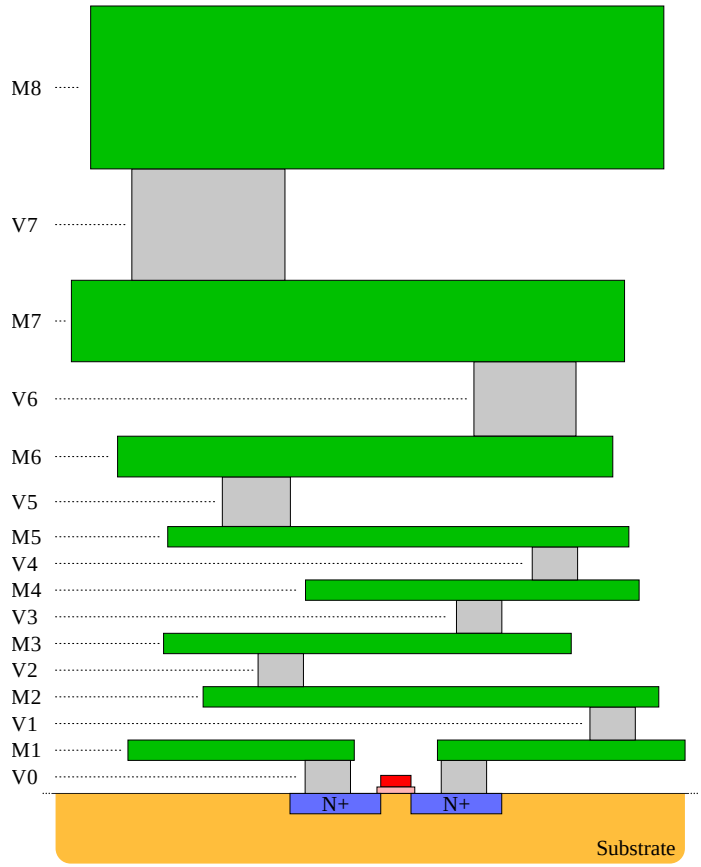


Figure 3.30 – Metal stack of the considered technology (not on scale).

(V5 to V7) are getting increasingly larger.

The issue of any metal stack is that it adds unavoidable series resistance for any interconnect. This added resistance degrades the performance in two major ways: increase in propagation delays and increase in power losses. Furthermore, metal routing also creates capacitances, e.g. the case of two adjacent lines on the same layer or two aligned plates on successive layers. These capacitances also increase propagation delays. In a switching circuit, these capacitances will decrease performance by adding switching losses.

A important concern is to quantify the impact of the routing on the considered device. This impact should be evaluated prior to layout to be able to

adapt design before wasting too much time by redesigning. The evaluation is done based on given technology characterization of metal and via resistance. The resistance values of vias and metal layers is summarized in Table 3.7.

Table 3.7 – Resistance of vias (left) and metal layers (right) of considered technology.

	Resistance
V0	50 Ω
V1	4.5 Ω
V2	4.5 Ω
V3	4.5 Ω
V4	4.5 Ω
V5	1.7 Ω
V6	0.35 Ω
V7	0.06 Ω

	Sheet resistance
M1	300 mΩ/□
M2	300 mΩ/□
M3	300 mΩ/□
M4	300 mΩ/□
M5	300 mΩ/□
M6	61 mΩ/□
M7	22 mΩ/□
M8	11 mΩ/□

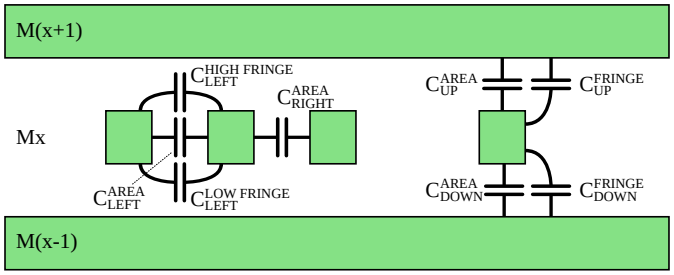


Figure 3.31 – Parasitic capacitances of metal layers.

The parasitic capacitances of metal layers are evaluated following Figure 3.31. Capacitances are evaluated for a given metal layer, assuming that it is surrounded by previous and next metal layers. This defines several capacitances, some related to areas and the others related to fringes. These capacitances are calculated per unit length of the considered metal layer, at minimum width. These capacitances can be divided in three practical values:

a top capacitance, a bottom capacitance and a side capacitance. They are defined by the following relations:

$$C_{TOP} = C_{UP}^{AREA} + C_{UP}^{FRINGE} \tag{3.1}$$

$$C_{BOT} = C_{DOWN}^{AREA} + C_{DOWN}^{FRINGE} \tag{3.2}$$

$$C_{SIDE} = C_{RIGHT} = C_{LEFT} = C_{LEFT}^{AREA} + C_{LEFT}^{HIGHFRINGE} + C_{LEFT}^{LOWFRINGE} \tag{3.3}$$

The values of these capacitances can be used to evaluate the capacitance increase due to routing. Critical capacitances of the power stage transistor are the gate capacitance and the drain-to-source capacitance. In advanced process, the value of the side capacitance becomes larger than the value of the top and bottom capacitances as the thickness of the metal lines becomes larger than their minimum width. Side-by-side routing then creates important parasitic capacitance and should be carefully evaluated.

Another problem arising from the important thickness of metal lines is their vertical resistance. In the case of getting current from a pad to the substrate and then to a pad again, current is flowing vertically through the metal lines. The issues is that vertical resistance is not a usually available design parameter.

3.3.2.2 Routing propositions

A simple analytical evaluation of routing is carried out to evaluate whether or not the impact of routing can be neglected. A MOSFET built using N fingers has $N/2$ drain contacts and $(N/2 + 1)$ source contacts, but only $N/2$ source contacts are considered for easier calculations. Assuming that X vias V0 can be put by finger, the access resistance is then:

$$R_{DRAIN} = R_{SOURCE} = \frac{R_{V0}}{X}\frac{2}{N} \tag{3.4}$$

$$R_{DS} = \frac{R_{V0}}{X}\frac{4}{N} \tag{3.5}$$

The same approach can be used to take into account the other vias.

A 1.2 V N-MOSFET with ten fingers of 10 µm each has an on-state resistance of approximately 6 Ω (600 Ω µm). It is possible to place approximately

50 vias V0 along the 10 µm contact finger. This means that the increase in resistance due to the vias V0 is approximately 400 mΩ. This resistance is not negligible compared to the initial on-state resistance, especially when considering that this is only the first level of vias, and metal thickness is not considered.

These observations, correlated with some test designs and parasitic device extraction on metal and via resistances, have shown that for the 1.2 V N-MOSFET metal stack resistance is far from being negligible, and design must be adapted to counterbalance the issue.

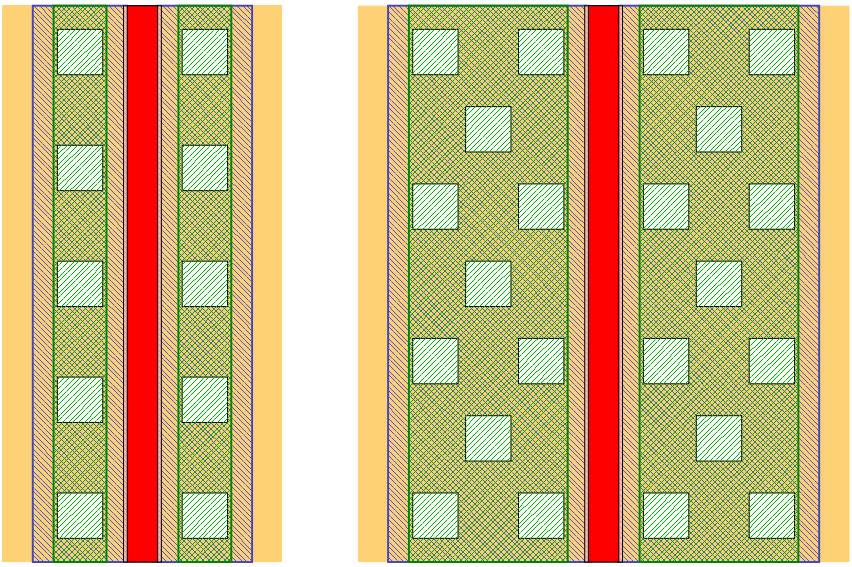


Figure 3.32 – Classical (left) and proposed (right) N-MOSFET finger structure.

The proposed strategy is to rebuild the MOSFET finger using larger drain and source contact zones. Figure 3.32 presents a top view of both the classical (left) and proposed (right) approach. Increasing the contact zone allows for higher number of vias and also increases the surface of metal on top of the transistor, making routing less resistive. This technique helps achieving better N-MOSFET performance, i.e. less parasitic resistance without increasing parasitic capacitances.

A supplementary proposed strategy to optimize metal routing is the placement of the vias. When considering the stacking of the vias, two approaches are possible. The first one is to align all via layers, creating a straight path for the current. The second approach is to alternate the via placement, making the current path more shaped. Both approaches are depicted in Figure 3.33 and Figure 3.34.

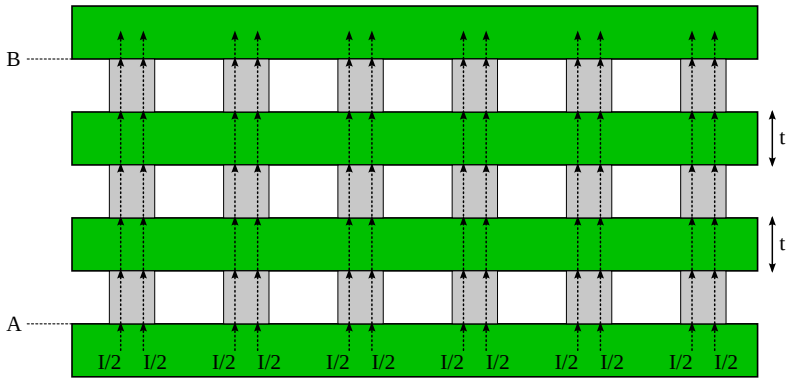


Figure 3.33 – Aligned-vias stacking structure.

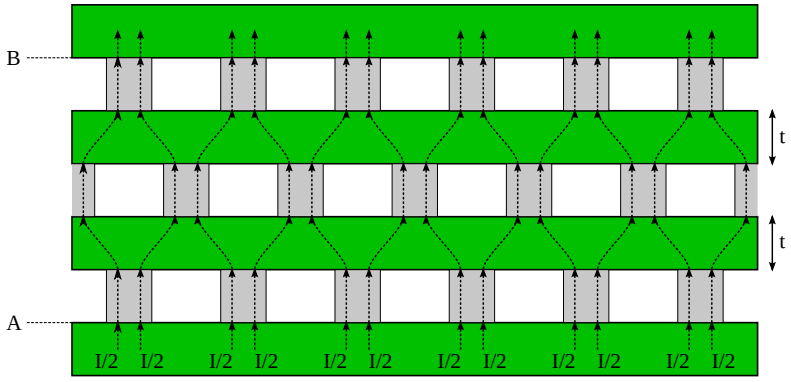


Figure 3.34 – Alternated-vias stacking structure.

In order to compare these two structures, the conduction losses (RI^2) between plane A and plane B have been analytically computed. The assumption is that the current path in the metal lines of the alternated structure is in-

creased by $\sqrt{2}$ compared to the aligned structure. Vertical resistance of metal lines between two aligned vias is noted R_M and resistance of vias is R_V. The resistance value of metal lines between two alternated vias is then $R_M\sqrt{2}$. Total conduction losses in the aligned case are then:

$$P_{ALIGN} = 6R_V I^2 + 6R_M I^2 \tag{3.6}$$

In the alternated case, losses are expressed as:

$$\begin{aligned} P_{ALTERN} &= 6R_V I^2 + 12\sqrt{2}R_M \left(\frac{I}{2}\right)^2 \\ &= 6R_V I^2 + 6R_M \frac{I^2}{\sqrt{2}} \end{aligned} \tag{3.7}$$

When comparing expression in Equation (3.6) and in Equation (3.7), we see that the alternated vias disposition allows to decrease the conduction losses due to metal thickness. It is thus the preferred strategy for routing the power MOSFETs.

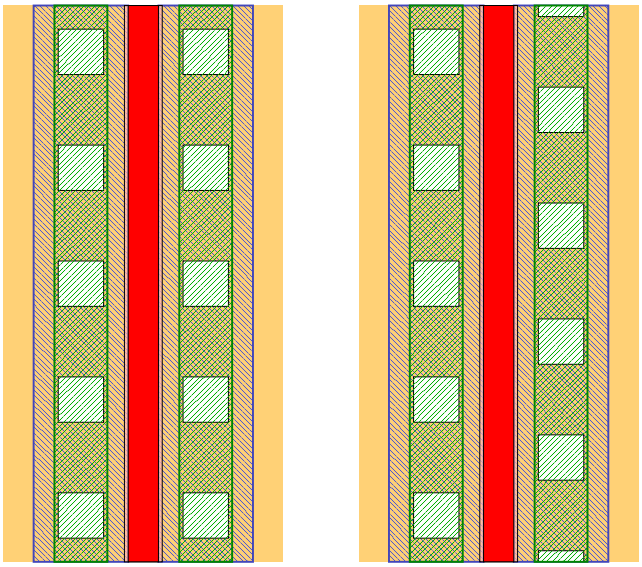


Figure 3.35 – Classical (left) and reduced capacitance (right) vias placement.

In order to limit the parasitic capacitances, metal routing of different nets should have an important spacing. However increasing the spacing might

reduce the surface of metal, thus increases the resistance which is not wanted. One strategy to reduce parasitic routing capacitances without modifying the amount of metal is to optimized the placement of vias. This approach is presented in Figure 3.35. On the right, via-to-via capacitance is reduced as distance between via surface is increased.

In terms of metal routing, parasitic capacitances are unavoidable. The side capacitances have been limited by preferring few large metal lines for routing instead of many narrow lines. This limits the side-by-side routing.

3.3.3 Matching issues

The behavior of some circuits can be very sensitive to process variability. The layout must ensure that implemented circuits will be as little sensitive as possible to these process variations. However these variations mostly affect absolute design values, e.g. channel resistance value or transconductance. Relative design values (e.g. relative difference in channel resistance of two adjacent identically designed transistors) can be well controlled if layout take into account the process variability. Some process variations can be predictable and taken into account. These predictable variations are essentially linked to the environment of the laid-out part. Matching strategies are well known and techniques used in this are very classical ones.

If two MOSFETs, MOS1 and MOS2, are required to be similar, they must have the same surroundings to ensure that process (e.g. etching, metal deposition) develops similarly for both MOSFETs. Current should also flow in the same direction in the two MOSFETs. The use of dummy structures is necessary to achieve good matching. A matched structure using dummies is presented in Figure 3.36. Without the *Dum1* and *Dum2* structures, the

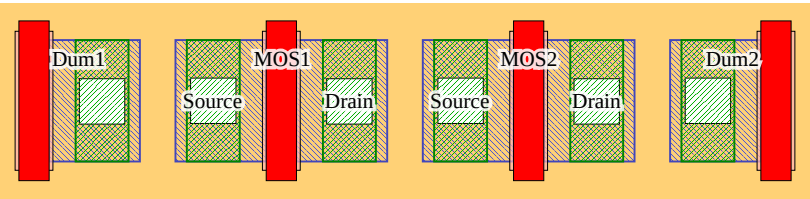


Figure 3.36 – Example of matched structure using dummies.

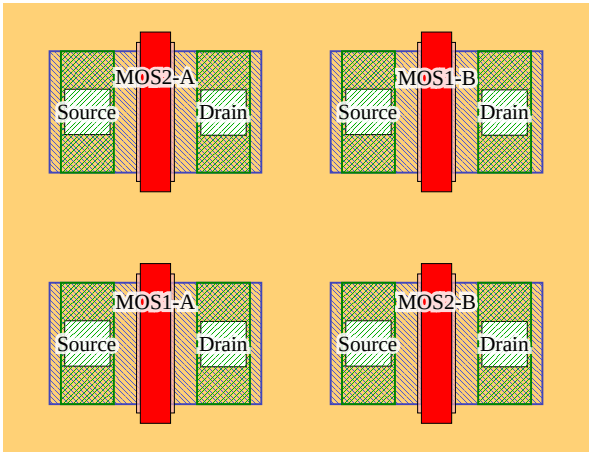


Figure 3.37 – Example of matched structure using common centroid approach.

source of MOS1 would not have the same environment as the source of MOS2, meaning that the two devices would not be properly matched.

Matching devices by taking into account random process variations can be difficult. A classical approach is to use common centroid designs, presented in Figure 3.37 for two devices. The strategy is to split devices in two or more identical elements, and place these part so that they have a common barycenter. In such a structure, if the process variation is gradual, the resulting two MOSFETs should be equally affected by the variation, making them properly matched. Using a common centroid structure doesn't prevent from using dummies to provide the same surroundings to all elements.

These two matching strategies have been used for the design of the current reference, the level-shifter and the delay cells. Long and/or large MOSFETs have been split into several identical elements, that were either connected in series (for long MOSFETs) or in parallel (for large MOSFETs).

3.4 Layout of converters

This section presents the layout of the standard and cascode converters. In addition to cells presented in Section 3.2, some minor ones were added, but

as they do not have key roles in the converter behavior, they were knowingly omitted in the design presentation The presented layout is only for the 100 MHz configurations. The 200 MHz versions are very similar: they differ only at the output (power stage size and associated drivers).

3.4.1 Sub-circuit cells layouts

3.4.1.1 Generic cells

Some cells were designed to be used for both standard and cascode power converters. These are the cells that are placed before the level-shifter. They are the input clock buffer and the current reference.

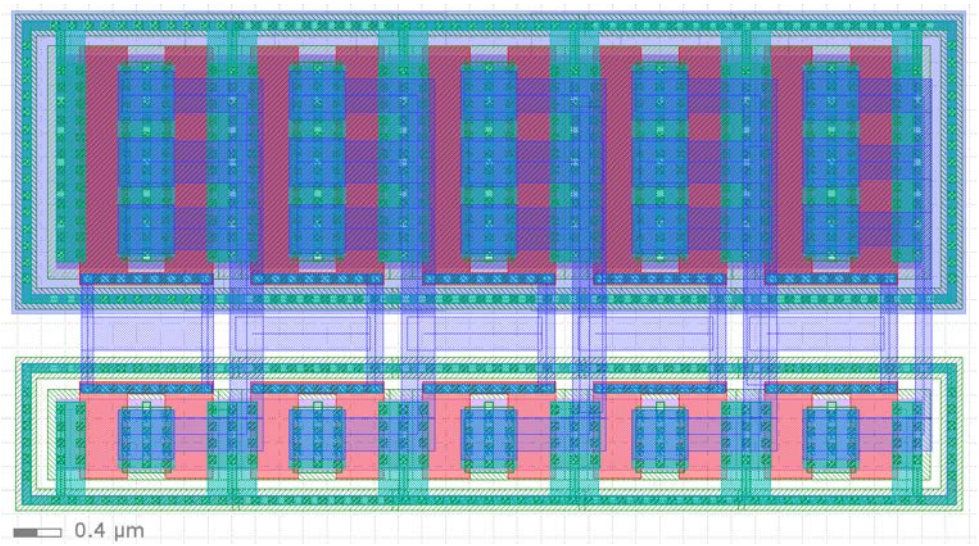


Figure 3.38 – Layout of the input clock buffer.

Input clock buffer layout is presented in Figure 3.38. Input is on the left and output on the right. It only consists of five inverters. Its role is to reshape the clock input signal (steeper slew rate) and to generate the two complementary clock signals required for the level-shifter (signals taken after the fourth and the fifth inverter). P-MOSFETs area and N-MOSFETs area are respectively shielded using guard-rings to avoid high frequency noise propagation through the substrate.

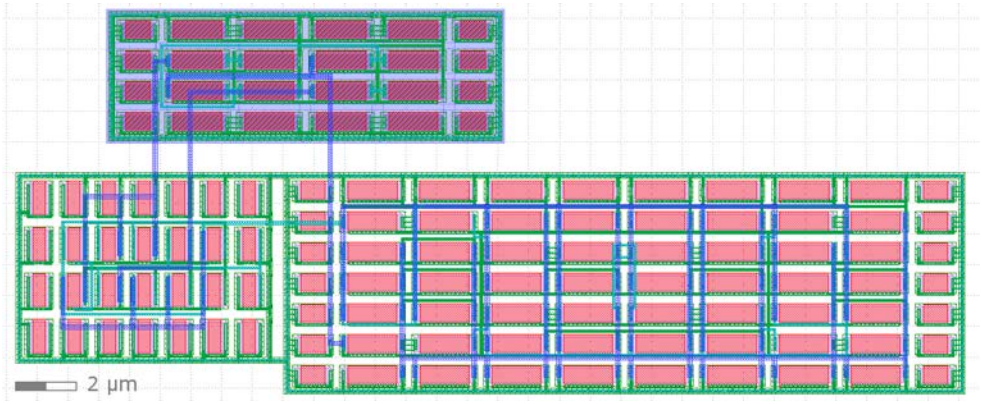


Figure 3.39 – Layout of the current reference.

The current reference layout is presented in Figure 3.39. It is the implementation of the circuit presented in Figure 3.21. Current sink pin is on the lower right. It is built using identical unit MOSFET cells for matched transistors, spread in three areas: a P-MOSFETs area and two N-MOSFET areas. Dummy structures are added around these areas to guarantee proper matching of all unit cells. Again, areas of P- and N-MOSFETs are protected using guard-rings, but in this case this is more to avoid being perturbed by noise than to limit the noise emission.

3.4.1.2 Standard converter cells

Following the input clock buffer and the current reference is the level-shifter (Figure 3.40). It is the implementation of the circuit presented in Figure 3.16. Input is at the lower left and outputs are at the right. Matched transistors are segmented into unit cells and dummies are added to ensure matching and precise current mirroring. Outputs of the level-shifter are identically designed for the same reasons. The two outputs are coupled using the 90 fF interdigitated MOM capacitor.

Following the level-shifter a synchronization line has been added, depicted in Figure 3.41. This cell has not been presented in Section 3.2 as it does not provide an additional functionality in the circuit. Inputs are at the upper left and right and outputs at the lower left and right. This part is built using two-

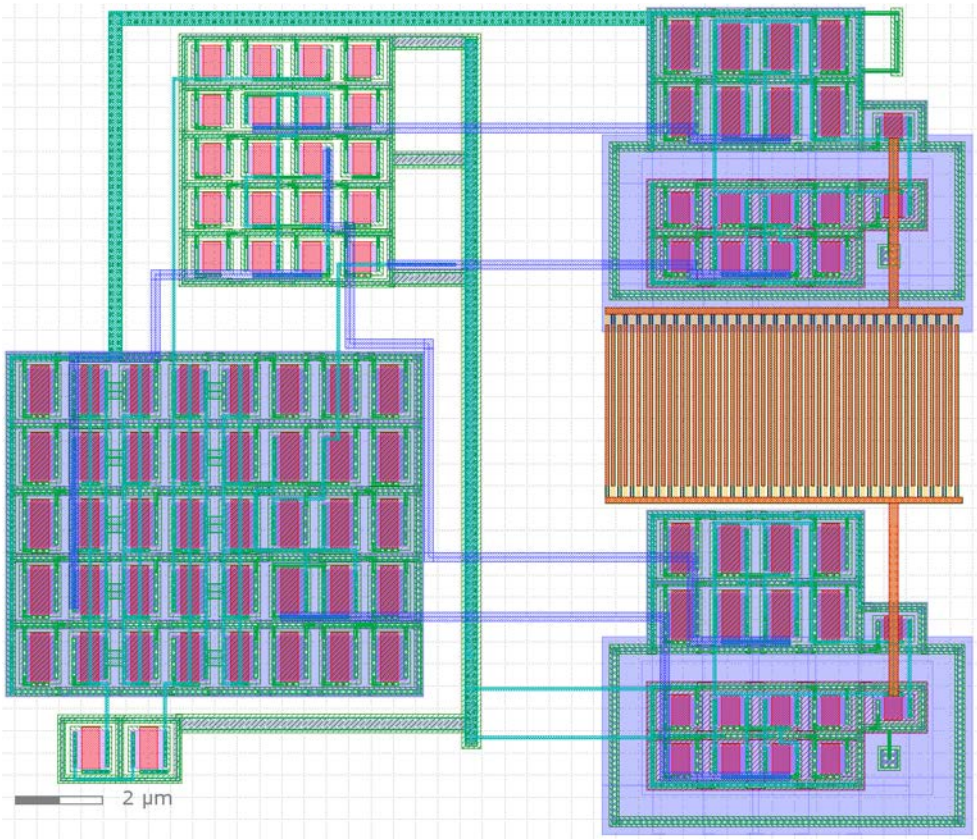


Figure 3.40 – Layout of the level-shifter for the standard converter.

times four small inverters capacitively coupled at their outputs. Its role is to force driving signals to be perfectly synchronized. As the output of the level-shifter should already be synchronized (verified in post-layout simulation), this cell can be a bit superfluous, but has still been added to have the guaranty of good synchronization. This cell has not been presented in Section 3.2 as it does not provide an additional functionality in the circuit. As MOSFETs are small, and signals already relatively well synchronized at the input, power consumption of this circuit is not significant.

The layout of the drivers of the standard power stage is presented in Figure 3.42. The schematic of this cell is depicted in Figure 3.12 Inputs are at

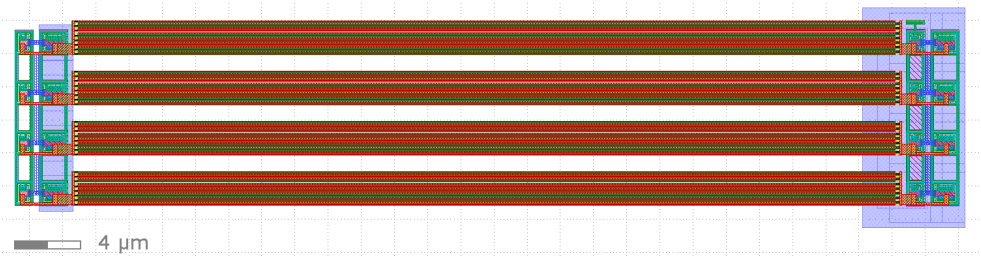


Figure 3.41 – Layout of the synchronization line for the standard converter (flipped 90° clockwise).

the top, and outputs at the bottom. The first small cells are the ones that create the proper dead-time, then big cells are the tapered buffers.

The drivers then are feeding the power stage, presented in Figure 3.43. Driving signals come from the left and V_{LX} node is in the mid-right. The immediate drivers of the power P-MOSFET and N-MOSFET are included in this cell as each transistor has a its own driving signal.

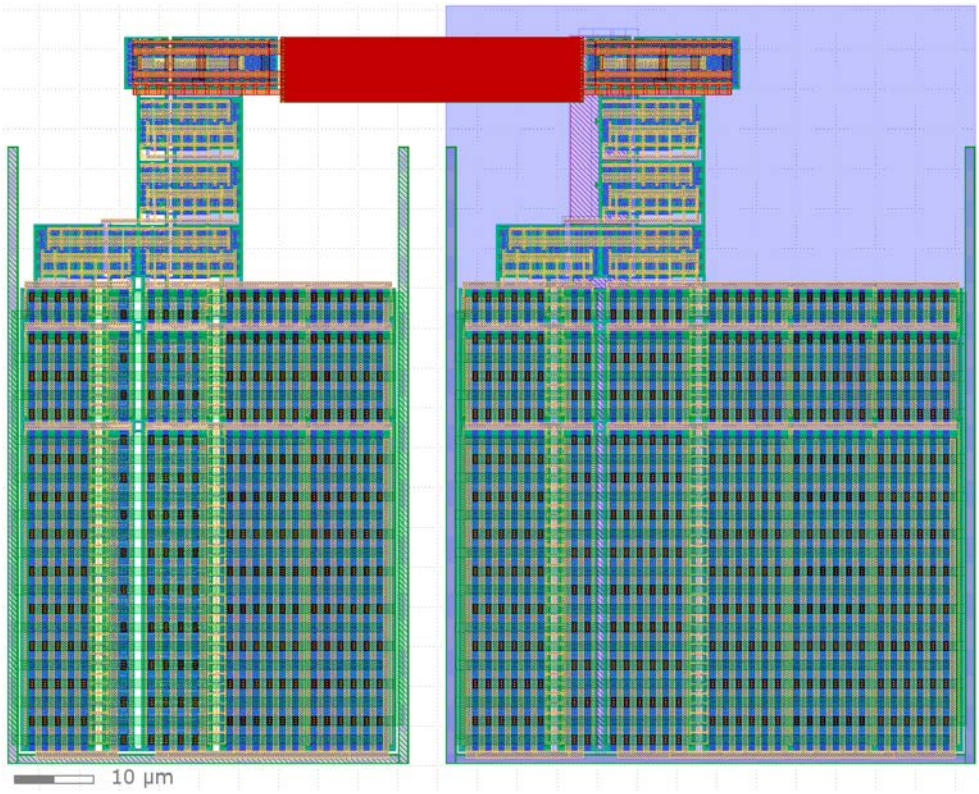


Figure 3.42 – Layout of the drivers for the standard converter (flipped 90° clockwise).

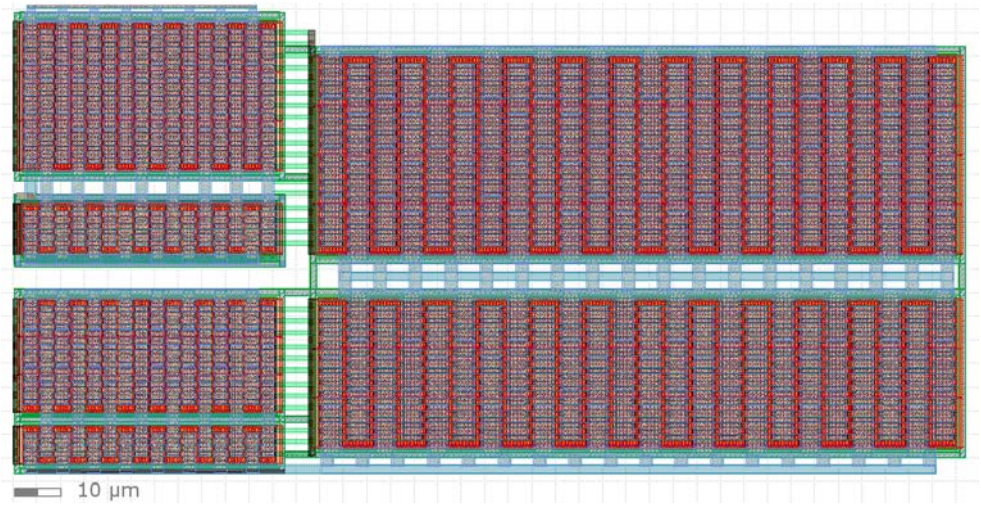


Figure 3.43 – Layout of the power stage of the standard converter.

3.4.1.3 Cascode converter cells

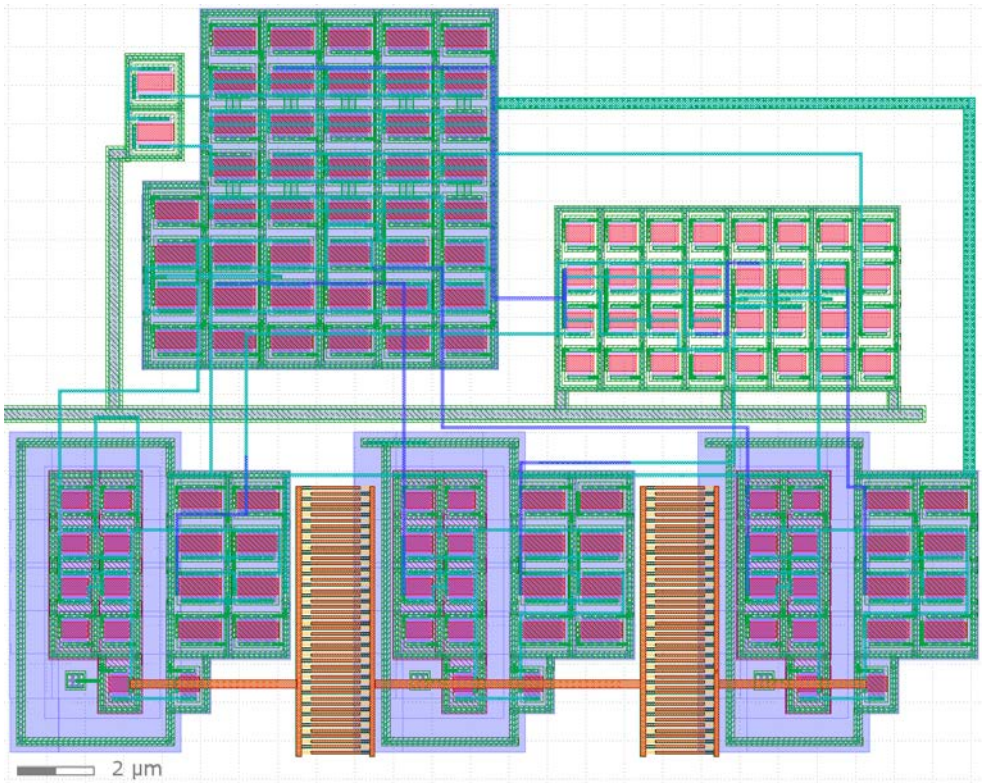


Figure 3.44 – Layout of the level-shifter for the cascode converter (flipped 90° clockwise).

The layout of the level-shifter for the cascode converter is presented in Figure 3.44. It is the implementation of the circuit presented in Figure 3.18. It is almost identical to the level-shifter of the standard converter, except that it features three outputs (at the lower left, middle and right). The three outputs are coupled using two 28 fF interdigitated MOM capacitors.

As for the standard converter, a synchronization line has been added, depicted in Figure 3.45. Inputs are at the upper left, middle and right and outputs at the lower left, middle and right. This part is built using three-times four small inverters capacitively coupled at their outputs. Its role is the

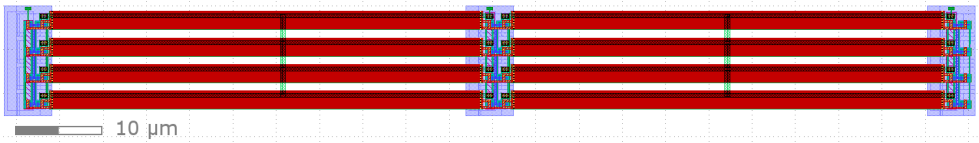


Figure 3.45 – Layout of the synchronization line for the cascode converter (flipped 90° clockwise).

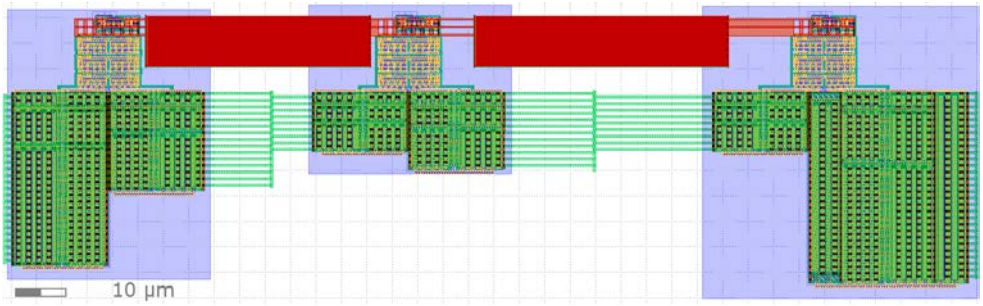


Figure 3.46 – Layout of the drivers for the cascode converter (flipped 90° clockwise).

same as in the standard converter. The two major differences are the number of signals (three instead of two) and the type of MOSFET utilized. Here only 1.2 V MOSFET are used for design.

The layout of the drivers of the cascode power stage is presented in Figure 3.46. This figure is the implementation of the schematic presented in Figure 3.13. The first small cells on top are the ones that create the proper dead-time, then big cells are the tapered buffers. Output signals are at the lower end of the picture. Placement of the drivers is performed to match the power stage.

The drivers are then feeding the power stage, presented in Figure 3.47. Polarization MOSFETs are included in the power stage cell. In this implementation, we can easily identify the three P-MOSFETs and N-MOSFETs connected in series.

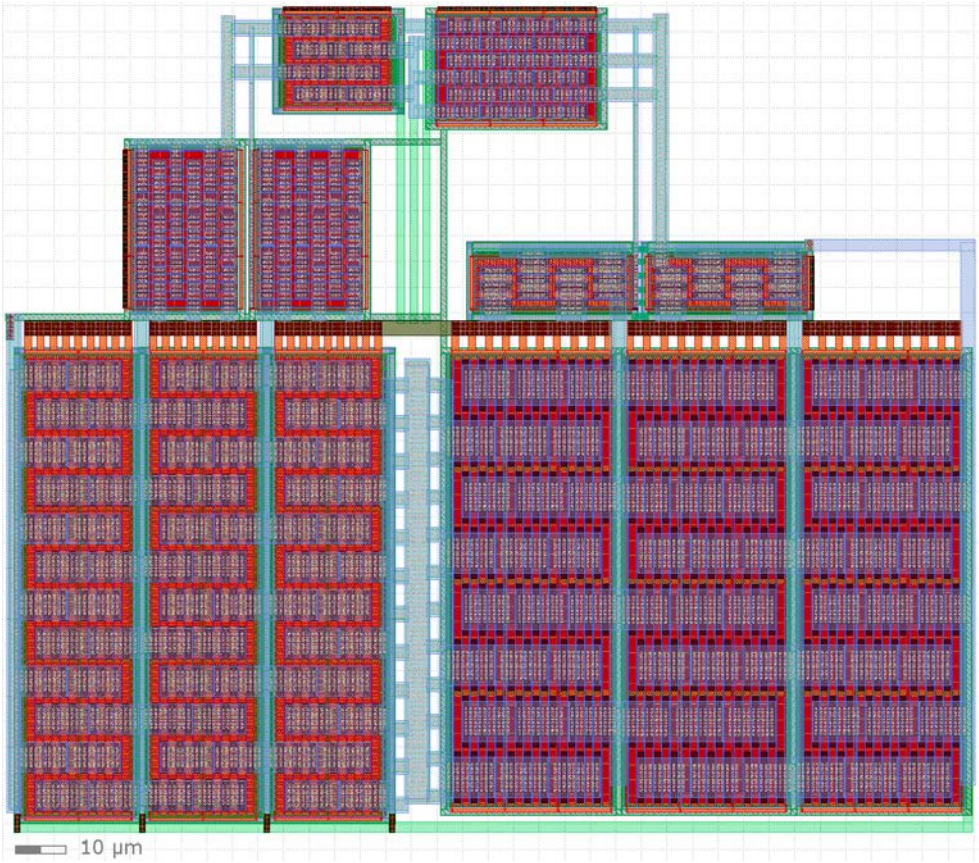


Figure 3.47 – Layout of the power stage of the cascode converter (flipped 90° clockwise).

3.4.2 Full converter layouts

All the previously presented cells are then connected together to build the open-loop converter. The layout of the standard and the cascode converter are depicted in Figure 3.48 and Figure 3.49 respectively. In both pictures, clock input is on the left, and output of the power stage on the right. From these two views, we see that the difference in power stages doesn't impact much the total area of the converters as they are quite comparable (0.042 mm^2 for the standard and 0.048 mm^2 for the cascode) but form factor is a bit differ-

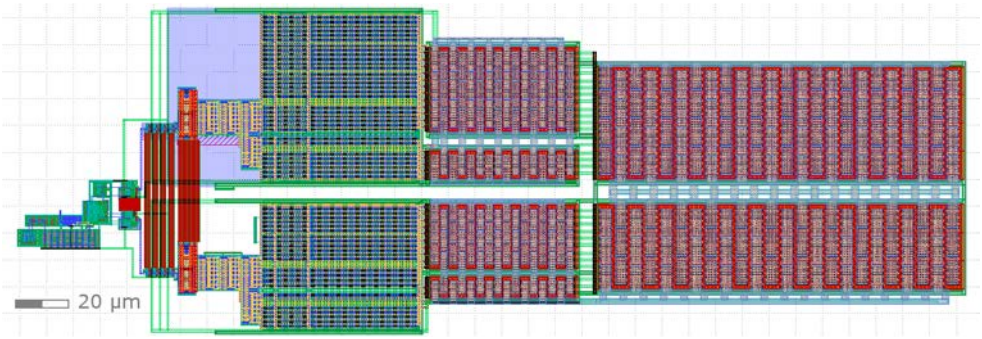


Figure 3.48 – Layout of the standard open-loop converter.

ent. The relatively constant area comes from the fact that despite requiring more devices, the cascode power stage uses much thinner MOSFETs than the standard one, making the overall area not significantly affected. Furthermore, in both cases, most of the space is occupied by the power stage and the associated drivers. In the case of the cascode power stage, the space between the drivers and the power stage has been increased to meet Design Rule Check (DRC) constraints. An better design would be to put the drivers as close as possible to the power stage, but density issues made that impossible.

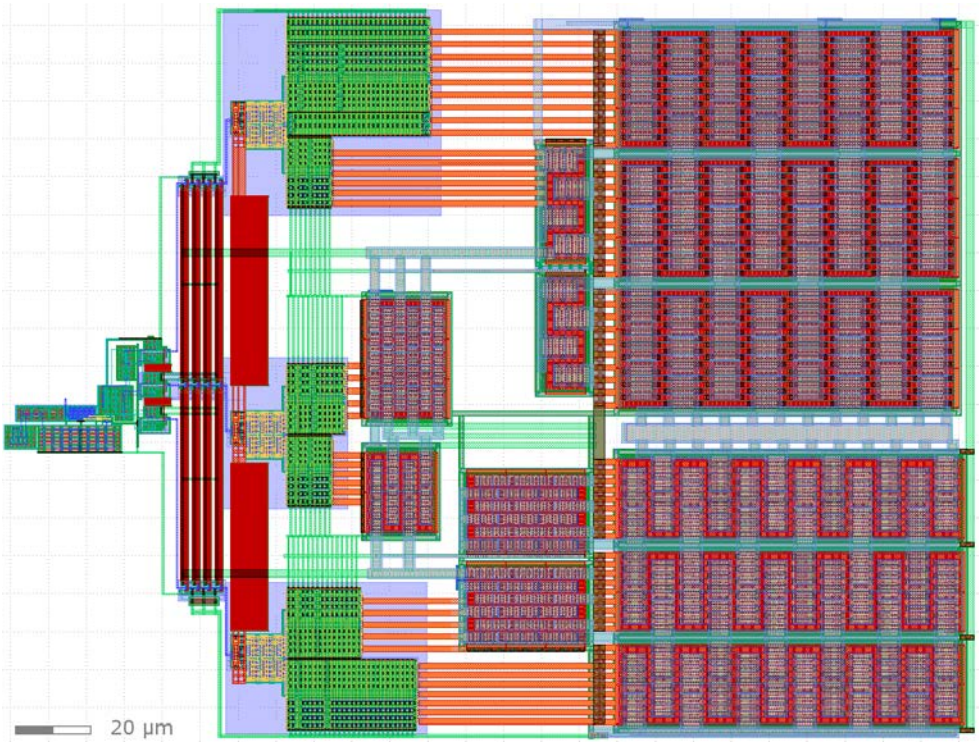


Figure 3.49 – Layout of the cascode open-loop converter.

3.5 Chip-level considerations

Once the converter is fully designed, it needs to be placed on-chip and connected to the pads. This section presents the major concerns faced at this design step. They include the converter placement, the placement of on-chip capacitors and the top-level routing.

3.5.1 Converter placement

The available silicon area is restricted to two dice of $1\,\mathrm{mm}^2$ each. So each $1\,\mathrm{mm}^2$ needs to contain two converters as we want to test four converters. The placement of the converters must account for the pads position. The pads are constrained by the design of the interposer. An optimum approach would be to co-optimize the interposer and the placement of the converter on the chip.

However this approach could not be used as this was not compatible with interposer and IC respective manufacturing details. As a result the interposer was designed beforehand, IC has then to adapt to it. Interposer design is detailed in Section 4.2. Furthermore, only one interposer design is available, so both ICs must have a compatible ball-out with the interposer.

The die is going to be flipped on top of the interposer. A four-by-four pad matrix is used for this. Two converters will be put on chip, but only one will be connected. The selection of the converter assembled will be done during assembly, by rotating the chip of 180° or not. This implies that placement can be done by focusing on one half of the chip, and then the placement of the other converter will be similar. Luckily all four designed structures have similar footprint. This will help for achieving pin compatibility of all structures.

One important thing to note is that because of the flip-chip assembly, pin position when designing the IC are mirrored with respect to the position they have on the interposer.

The pad positions and associated input/output signals are shown in Figure 3.50 and in Figure 3.51. The two chips are very similar, as their respective pad positions are the same. The V_{REFA}, V_{REFB} and V_{REFC} are voltage supplies that are going to be used for the drivers, but no voltage values are constrained.

The placement of the converters is done to minimize the power path. It has been chosen to minimize the distance from the V_{DD} and V_{SS} pads to the converter to reduce as much as possible the parasitic resistance and inductance. Parasitic inductance is even more critical than resistance, as due to high frequency operation, it could generate ringing (i.e. over-voltage when switching) that could damage the power transistors, especially in the case of the cascode power stage.

The issue of parasitic inductance and resistance is less critical for the other voltage supplies as the current drawn is much smaller than through power supply pads. Regarding the V_{LX} pad, having a parasitic inductance is not an issue at all as it is connected in series to an inductor. However parasitic capacitance of this critical node can be an efficiency killer, thus a too long net might not be optimal. For the clock signal, almost no current is drawn

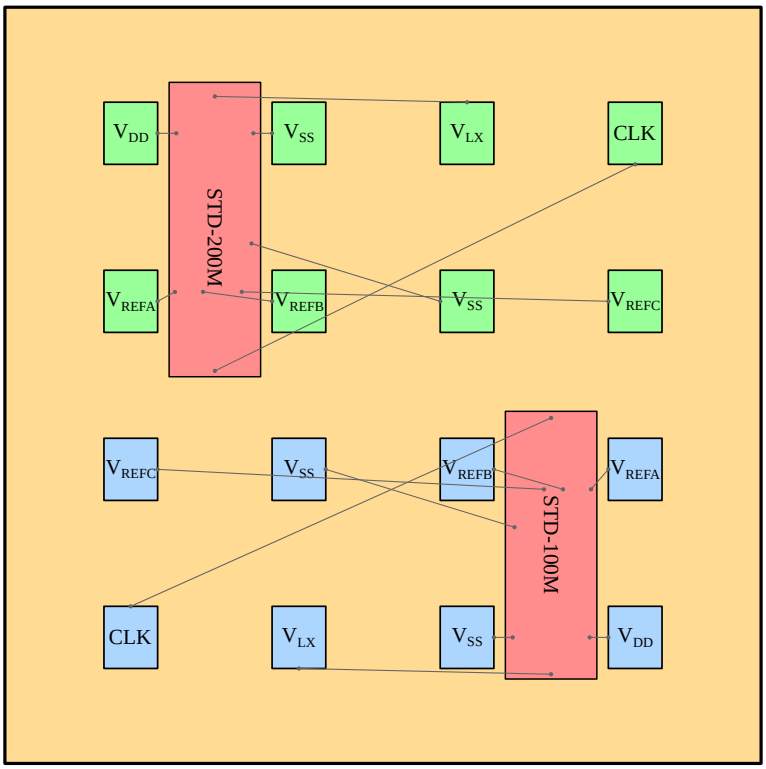


Figure 3.50 – Pad matrix, associated input/output signals and converter positions for the standard converters.

and wavelength is much higher than 1 mm at 200 MHz so propagation effects doesn't need to be accounted for.

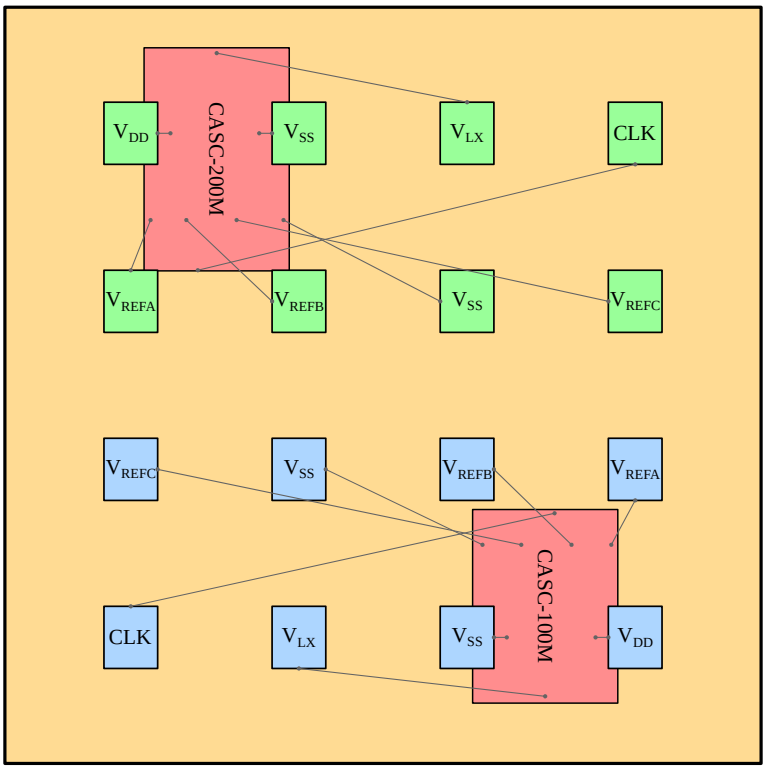


Figure 3.51 – Pad matrix, associated input/output signals and converter positions for the cascode converters.

3.5.2 On-chip capacitors

The converter only occupies a small area of the chip. The space left is filled with capacitors to provide better decoupling of the voltage supplies. This decoupling is not required by design, but might help to limit voltage oscillations during commutations.

Chosen capacitors type are MOM capacitors. The unit cell structure is presented in Figure 3.52. The reason to choose MOM over MOS capacitors is that for 3.3 V rating, this type of capacitor was presenting an equivalent density as the MOS capacitors due to the important number of metal layers. Furthermore this type of capacitors is very well distributed across the metal layers, making the parasitic inductance less important than in other structures.

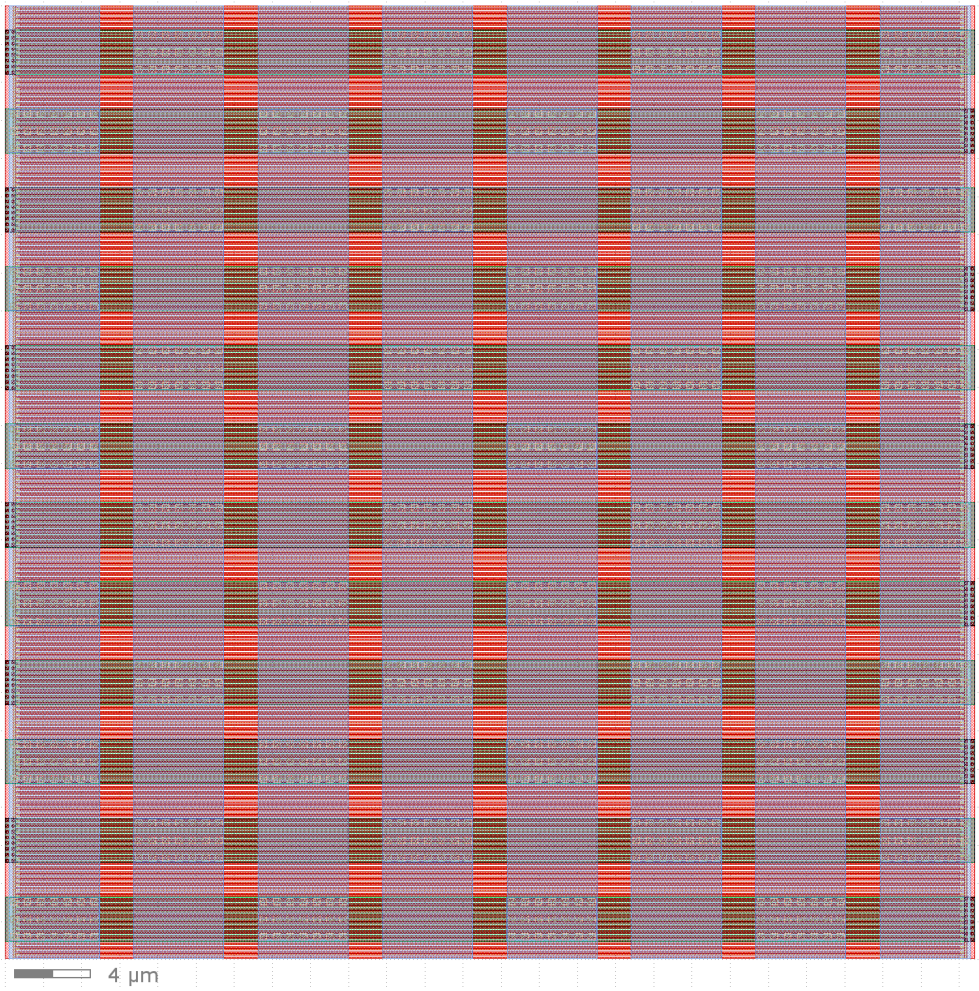


Figure 3.52 – Layout of a MOM capacitor cell.

The capacitor cell is built using interleaved metal fingers of the first five metal layers. Then two metal layers are added vertically and horizontally on top of it and connected to both electrodes of the capacitor, allowing for easy matrix design of these capacitor cells.

In order to maximize the on-chip decoupling, MOM capacitors are shared between 100 MHz and 200 MHz configurations. The drawback of this approach is that current source and level-shifter of both converters will be active when

the chip will be connected for testing. However since both configurations have the same input stage, decoupling losses under measurement should not be an issue. As clock input of unused converter will be properly tied, no additional losses should be added.

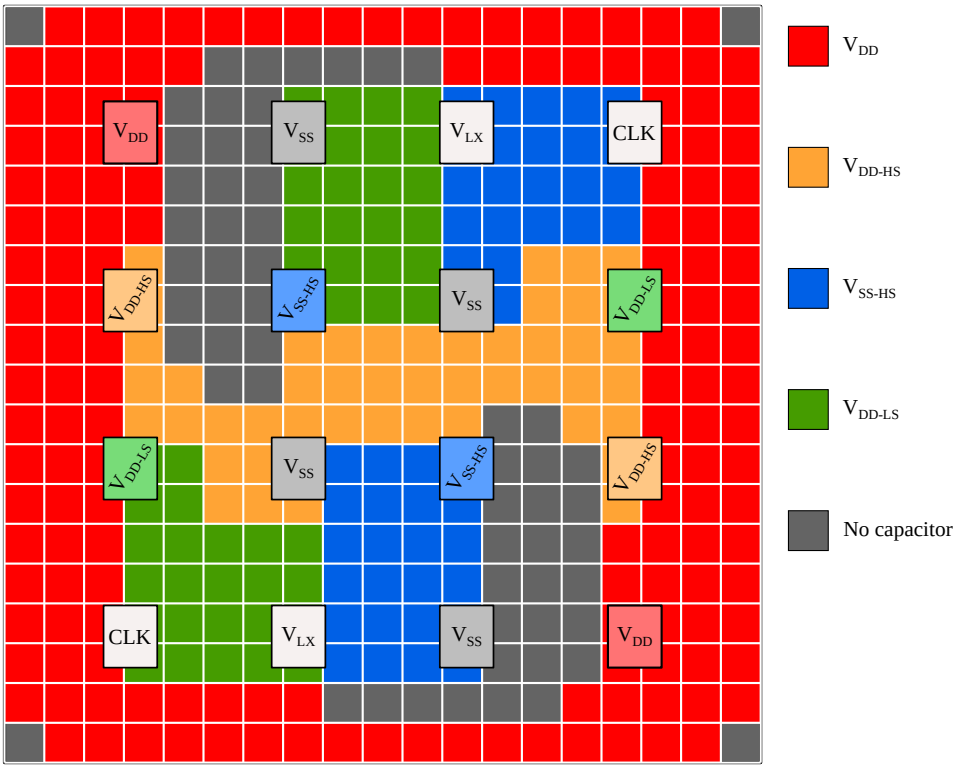


Figure 3.53 – Decoupling capacitors distribution over voltage domains for standard converters.

Each capacitor cell is 50 µm by 50 µm and has a capacitance of 7.3 pF. A spacing of 2 µm is put between each capacitor cell. In order to place the capacitor cells, the chip is divided into 19 by 19 squares of 52 µm. The placement of the cells for the various voltages are presented in Figure 3.53 and Figure 3.54 for the die with standard converters and the die with cascode converters respectivily. No capacitor cells could be put in the corners as the seal-rings of the dice were using some of the corners' area.

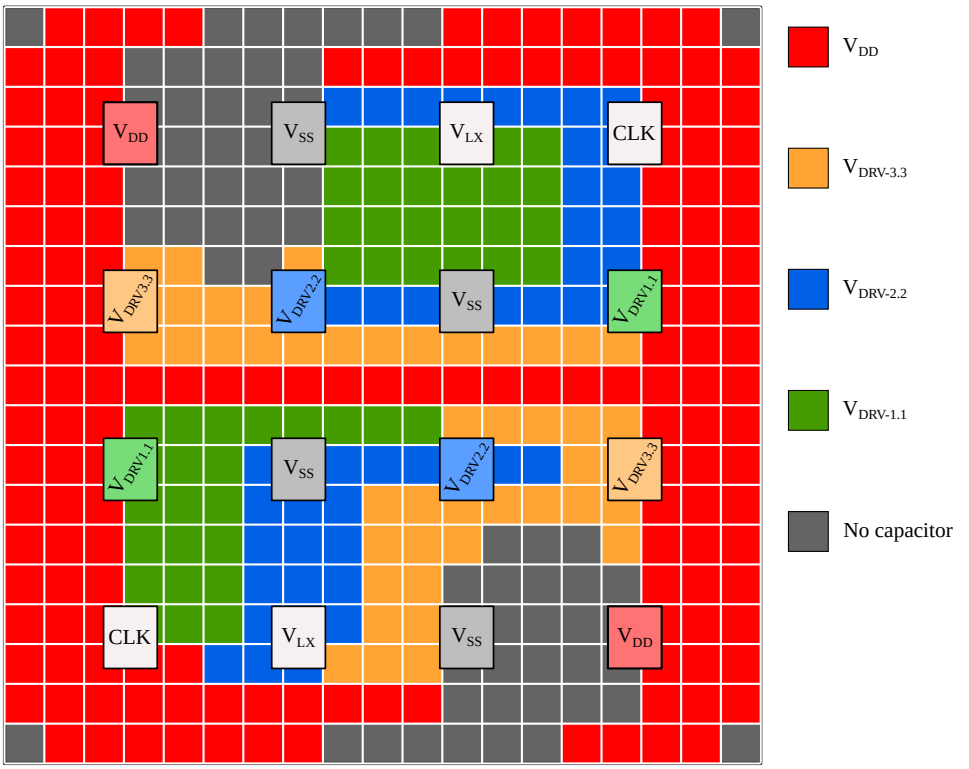


Figure 3.54 – Decoupling capacitors distribution over voltage domains for cascode converters.

In the end, more than 2 nF could be embedded on each die. Capacitance distribution is detailed in Table 3.8. A higher capacitance value is put on the V_{DD} net as this is the most critical and requires as much decoupling as possible.

Table 3.8 – On-chip capacitance distribution for standard (left) and cascode (right) dice.

"Standard" die		
	Cells	Capacitance
V_{DD}	158	1153.4 pF
$V_{DD\text{-}HS}$	48	350.4 pF
$V_{SS\text{-}HS}$	48	350.4 pF
$V_{DD\text{-}LS}$	48	350.4 pF

"Cascode" die		
	Cells	Capacitance
V_{DD}	155	1131.5 pF
$V_{DRV\text{-}3.3}$	46	335.8 pF
$V_{DRV\text{-}2.2}$	47	343.1 pF
$V_{DRV\text{-}1.1}$	47	343.1 pF

3.5.3 Top-level routing

Routing at the top level is performed using the last, thicker metal line. This routing is here to connect the pads to the inputs and outputs of the converter, and connect the capacitors that are not yet connected together – i.e. non-adjacent islands of capacitors belonging to the same voltage domain. Metal is also added on top of power transistors to reduce as much as possible their resistance. Top-level routing of the standard die and of the cascode die are presented in Figure 3.55 and Figure 3.56 respectively.

For the power output net (V_{LX}), as the distance from the MOSFETs to the pad is not short, routing is done using the last two metal layers of the metal stack, with multiple parallel lines. No MOM capacitors have been placed below this line to allow for routing.

Connection to the capacitors is done using metal fingers. Parasitic series resistance to the decoupling capacitors is limited by placing as many fingers as possible.

Once all the routing is done, all the parasitic elements of the full chip have been extracted (RC parasitic extraction), reduced and post-layout simulation was used to validate the full chip. The parasitic extraction of the full chips took a lot of computing time (approximately one day for each), as well as the reduction, which is necessary to be able to simulate anything in the end. Simulating without reduction would create a huge netlist that the simulator could not handle. However even with reduced extracted netlist, simulation is time consuming, thus only few switching periods have been simulated, no

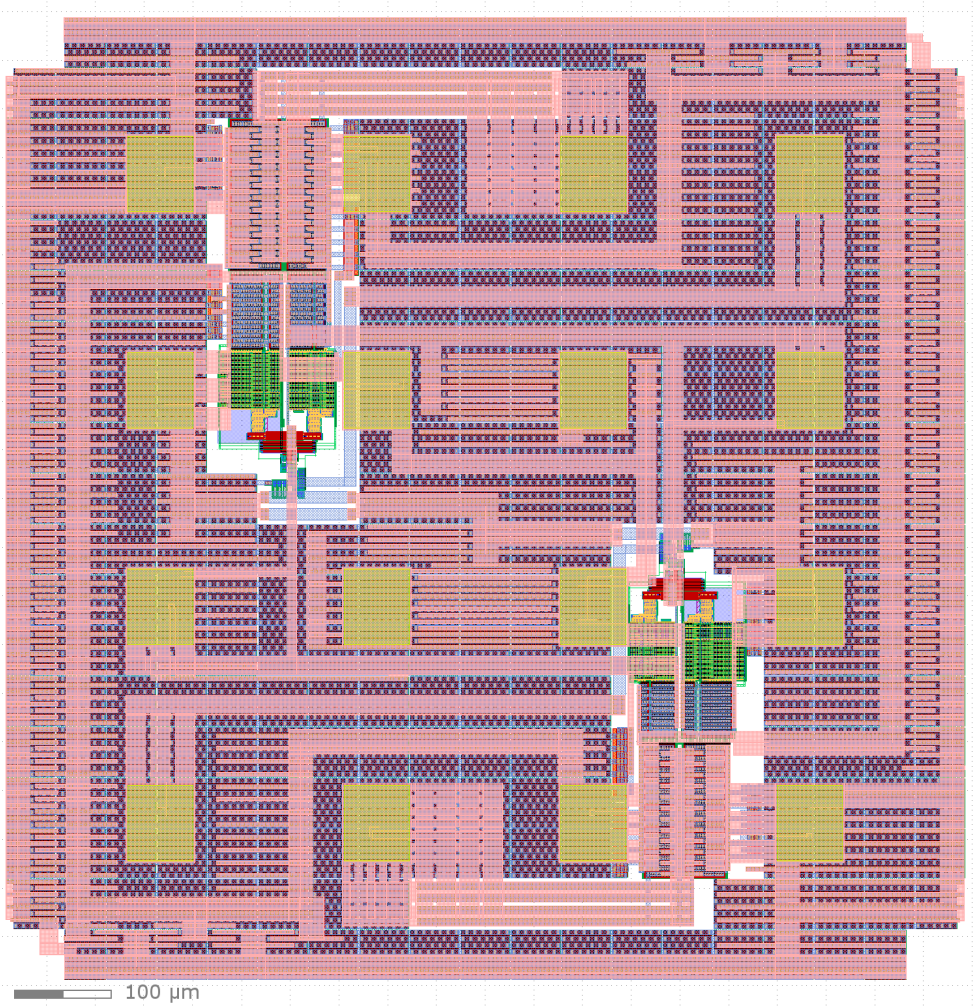


Figure 3.55 – Layout of the full chip with standard converters.

LC filter could be added in simulation because of too large transients (tens to hundreds of switching periods). Post Layout Simulation (PLS) results are detailed in the following part, along with the measurement results.

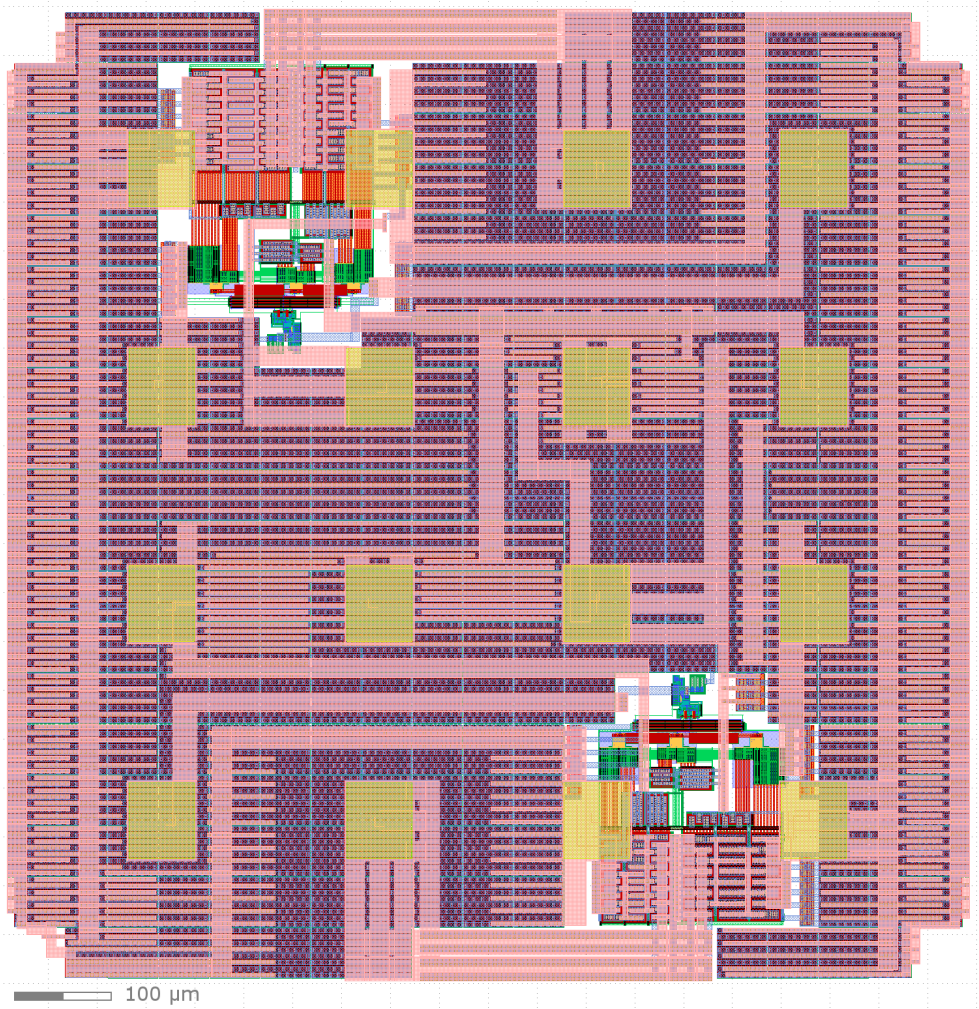


Figure 3.56 – Layout of the full chip with cascode converters.

3.6 Conclusion

This chapter detailed the central work of the thesis, i.e. the design of the integrated circuits. The presented design methodology is a top-down approach, from system to sub-cells. An output-to-input flow was developed, each designed part was setting precise specifications for the preceding one. The first

step to design was a schematic optimization. Dedicated cells for the cascode power stage have been designed, such as the three-outputs level-shifter.

Following the schematic optimization, all cells have been laid-out using the selected technology (40 nm bulk CMOS). Layout recommendations toward the high frequency operation were presented. Strategies to limit added capacitances and resistances have been proposed and utilized in the design process. Layout of the constituting cells of the standard and cascode converters have then been presented, and some area considerations were developed.

Chip-level considerations were then presented, taking into account the constraints due to the passive components. These considerations have included the on-chip placement for least performance degradation and on-chip decoupling strategies. In the end two similar chips are designed and manufactured. One chip embeds classical converters (using a standard power stage), and the other one features converters with the cascode power stage.

A micro-photograph of the manufactured die is presented in Figure 3.57. This die is the one that embeds the standard converters. The corresponding layout view is presented in Figure 3.55.

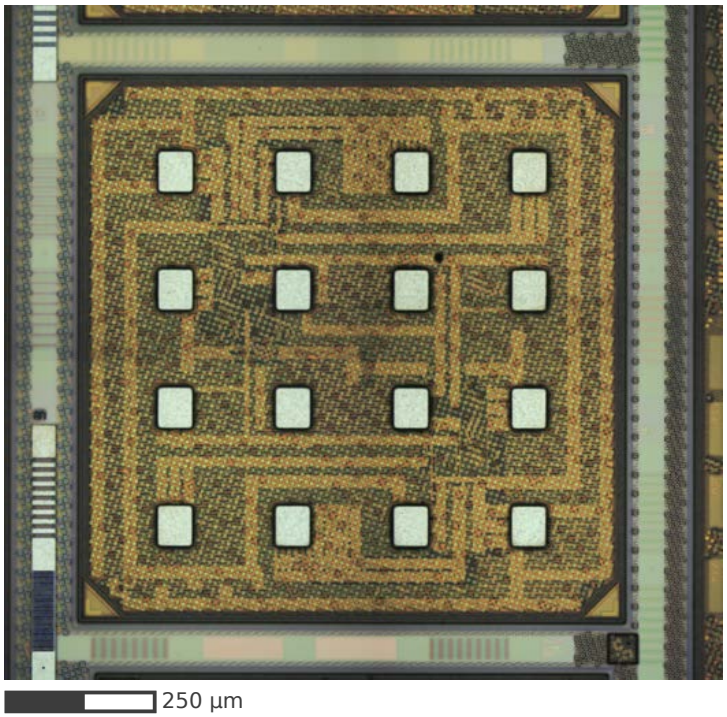


Figure 3.57 – Micro-photograph of the manufactured IC (embedding standard converters).

Chapter 4

Tests and measurements results

Contents

This chapter presents experimental measurements on the various samples of DC-DC converters. Some specific considerations of high frequency, low voltage testing are presented. Tests include individual measurements on passive devices (capacitive and inductive) as well as some ones on the active dice. Converter assemblies are tested and performances are confronted to simulation evaluations and validated.

4.1 Testing particularities

This section details some considerations about testing. It also presents the test equipment along with their major specifications.

4.1.1 Challenges

The major challenge is the high switching frequency operation. A +100 MHz square wave contains many high frequency harmonics. Capturing these high frequency harmonics is difficult due to the limited bandwidth of the equipment. Furthermore any small parasitic inductance and capacitance becomes significant at high frequency.

A major issue when measuring current and/or voltage is the impedance added by the measurement equipment. For instance, a voltage probe usually adds a resistance and capacitance. A current probe adds resistance and/or inductance (depending on the probe type). At high frequency, a capacitance in the range of a pico-farad can be very significant. Adding these parasitic elements can decrease the circuit performances and modify the waveforms, meaning that the "true" waveform might not be accessible. Adding any parasitic inductance and/or capacitance can also be critical for it triggers resonant circuits that can generate oscillations.

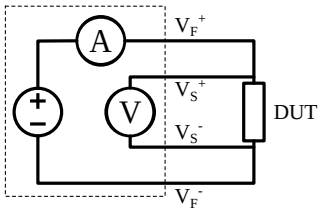


Figure 4.1 – Four-point measurement principle of operation.

Measurement addresses also low voltage. This means that voltage measurements need to be performed carefully to ensure that the accuracy is sufficient. Because of IR-drop, the position of the measurement setup matters a lot. Precise voltage measurements require a four-point approach(Kelvin method), as presented in Figure 4.1. Because of the small dimension of the system, achieving a true four-point measurement is difficult. Probes can not be placed where wanted due to physical constraints.

Regarding the measurements of the passive components, the concern is that actual values of components are in the range of parasitic component values. Inductances are in the range of tens of nano-henries, what is the equivalent inductance of a wire of few tens of millimeters.

4.1.2 Testing equipment

The equipment for testing was selected based on the frequency, parasitic components and accuracy constraints, developed in the previous part. The main concern is on frequency performance as high bandwidth is usually not found in classical equipment.

4.1.2.1 Impedance measurements

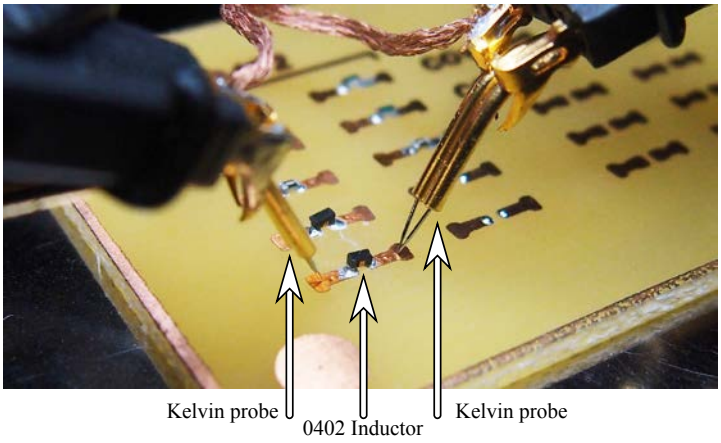


Figure 4.2 – 0402 commercial inductor under high frequency true-Kelvin probes.

An Agilent 4294A impedance-meter is used for the standalone tests of passive components. It features a four-point measurement with a bandwidth up to 110 MHz. In addition to the impedance-meter, probes are added to get contacts to the passive components. True-Kelvin coaxial probes are utilized in order to have four-points measurements up to 110 MHz. A picture of an 0402 commercial inductor under the true-Kelvin probes is presented in Figure 4.2. Probes are shielded very close to contact points allowing for high frequency measurements.

The equipment has been evaluated in terms of precision using equations from the datasheet [Agi08]. Maximum measurement errors on 1 nF capacitor and 10 nH inductor are presented in Figure 4.3. From this evaluation we see

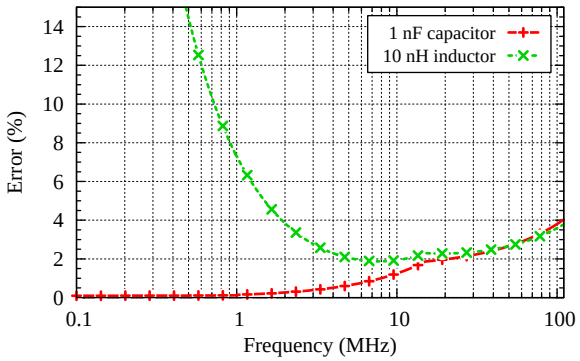


Figure 4.3 – Maximum relative errors for impedance measurement on capacitor and inductor using Agilent 4294A.

that capacitors should be measured with a good precision. However small inductor measurement precision is not guaranteed until relatively high operating frequency. The issue is that at high frequency, a good measurement accuracy requires a precise compensation and calibration.

4.1.2.2 Time-domain measurements

Several probes are needed to observe signal in time domain, e.g. switching waveforms and currents. Currents are measured using Tektronix CT6 AC probes (2 GHz bandwidth) and voltages using Tektronix TAP1500 active probes (1.5 GHz bandwidth). CT6 probe inserts a parasitic inductance of 1.5 nH along the current path, and theAP1500 has an input impedance of 1 MΩ and a less than 1 pF. All signals are visualized on a Tektronix DPO 7254 oscilloscope (2.5 GHz bandwidth, 40 GS/s).

A high frequency pulse generator is utilized, Agilent 81132A (data/pulse generator up to 660 MHz) to generate square wave signals required for clock signals. In some tests, this generator is associated with a buffer, a Texas Instruments THS4302 (wideband amplifier), to get more output current capability than the pulse generator alone.

4.1.2.3 Power measurements

Losses and power measurements are performed at DC voltage power supplies level. Since inputs and outputs of the converter are DC values, measurements can easily be performed using Source-Measurement Unit (SMU) as power supplies to ease the current measurements. An electronic DC load (BK8600) is used to allow for straightforward load change. All power supplies and loads are capable of four-point measurement for accurate voltage measurement.

4.2 Decoupling capacitors and interposer

The capacitive interposer is designed by IPDiA. Capacitor technology already has industrial applications, so deep-trench process is not a high risk. The novelty of the designed passive components is the very high frequency operation for a decoupling application in a power converter.

4.2.1 Manufactured interposer

A picture of the capacitive interposer is presented in Figure 4.4. The capacitors C_{REF1}, C_{REF2} and C_{REF3} are 11 nF capacitors, utilized for decoupling of the various power supplies of the drivers. The capacitor C_{IN} is the main input decoupling capacitor. Its value is 33 nF. The last capacitor is C_{OUT}, a 16 nF capacitor used for output voltage filtering. Other elements on the interposer are the IC landing pattern (a 4-by-4 pad matrix) on which the IC will be flipped and an 0402 SMD landing pattern for commercial inductor soldering. compared to values listed in Section 2.5, capacitor values have been adjusted by the interposer supplier to ease the design.

Regarding the IC landing pattern, the upper half of the pads are not connected, except for the pad at the upper left. This pad is connected to the clock input of the spare converter in the IC die. The pad is tied down to ground to properly disable this not connected converter.

The design of the interposer was guided by two main constraints: minimizing the parasitic inductance between the main input capacitor and the IC landing pattern (V_{IN} net) and minimizing the parasitic capacitance of the net between the IC landing pattern and the inductor (switching node, V_{LX}

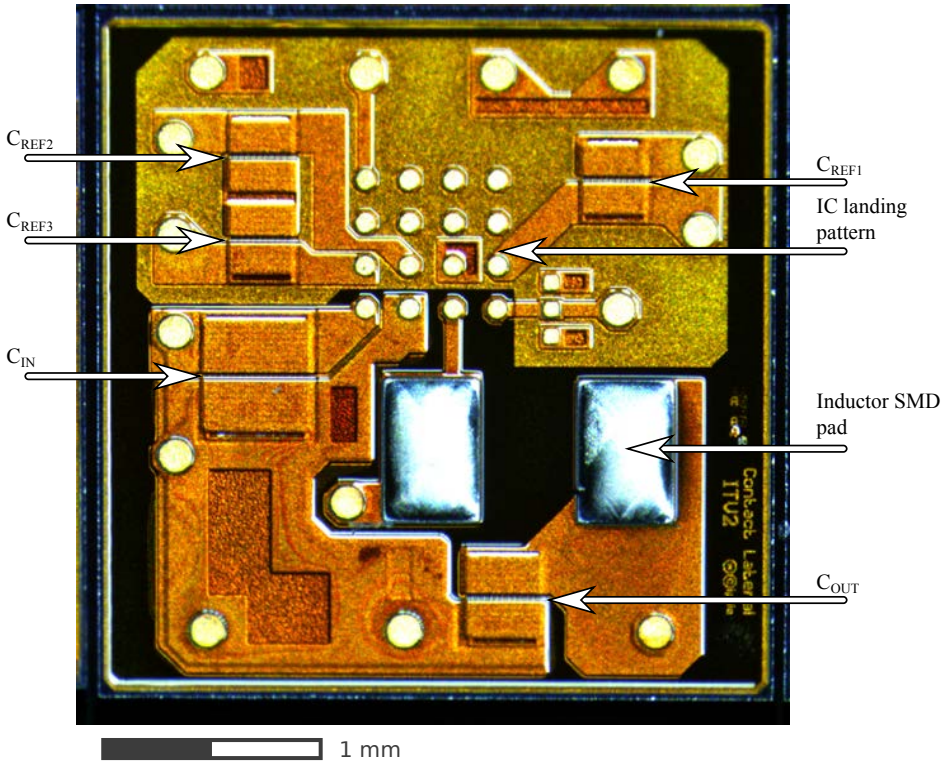
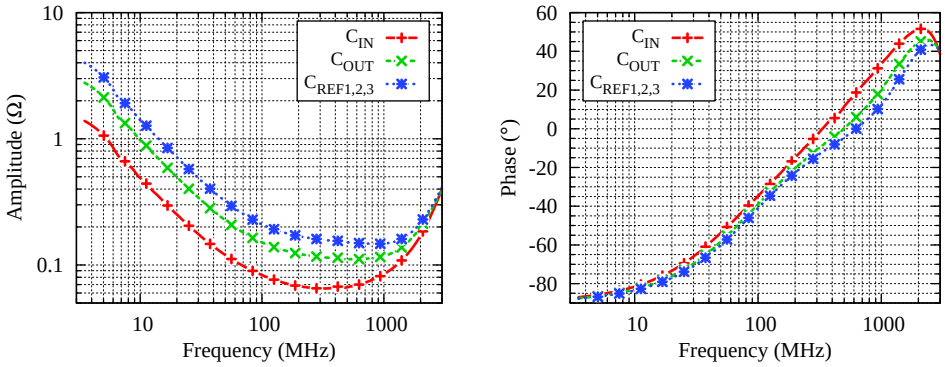


Figure 4.4 – Micro-photograph of the capacitive interposer.

net). Too much parasitic inductance from the decoupling capacitor to the IC landing pad would result in ringing during switching operation, creating over-voltage across power switches that could result in a breakdown of the devices. The presented design keeps this parasitic inductance very limited (less than 400 pH) as the pads are very close (approximately 200 µm) to the capacitor and large metal lines are used as well. 0402 landing pad is the main contributor to the parasitic capacitance of the V_{LX} net. Metal line from IC landing pad to inductor is kept thin and short to limit the capacitance. The interposer is not yet fully optimized as measurements pads are added.

The parasitic capacitance between V_{LX} net and ground has been evaluated with the impedance-meter. A value of 6.5 pF has been measured. This value has been taken into account in the design, with a notable impact on the drivers'

delay values. Measurement of the input net parasitic inductance could not be achieved because of its too small value. Measurement precision is not sufficient below 1 nH.



(a) Amplitude measurements.

(b) Phase measurements.

Figure 4.5 – Impedance measurements of the three designed trench-capacitors.

Capacitances have been characterized by the manufacturer (IPDiA) using a Vector Network Analyzer (VNA) up to 3 GHz. De-embedded impedance measurements are presented in Figure 4.5 for amplitude and phase. From the impedance amplitude measurement (Figure 4.5a) we can extract the capacitance value (C_{MEAS}) and the ESR (minimum of the amplitude), assuming that the capacitor is equivalent to a series RLC circuit. The SRF is reached when the phase (Figure 4.5b) crosses the zero axis. Extracted values are presented in Table 4.1.

Table 4.1 – Measured parameters of designed capacitor structures.

	C_{MEAS} (nF)	ESR (mΩ)	SRF (MHz)
C_{IN}	33	70	330
C_{OUT}	16	110	490
$C_{REF1,2,3}$	11	150	630

Capacitance values correspond to the design values. In term of ESR, it is fairly small for the input capacitor, so associated losses should be minimal.

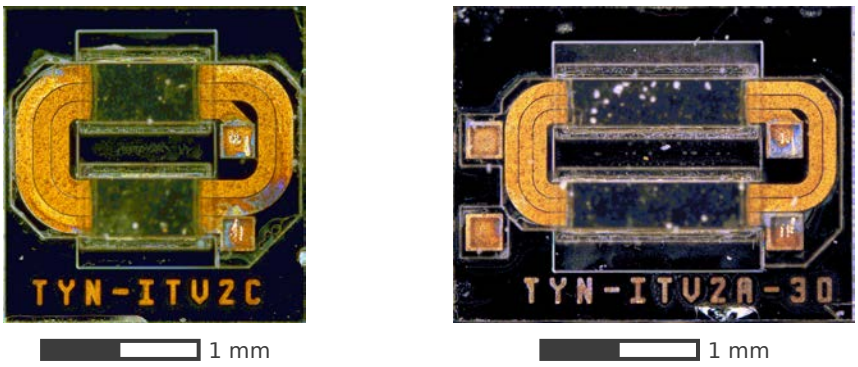
Each capacitor features an SRF higher than 200 MHz, so it should operate properly and provide efficient decoupling. It is possible to get an ESL from the SRF values. In our case, each capacitor has an ESL of approximately 10 pH. These low parasitic component values and the shortness of the routing paths from the capacitors to the IC pad-matrix make the interposer very well suitable for high frequency operation.

4.3 Integrated magnetic inductors

Inductor structures were selected based on the considerations presented in Section 2.4. Several integrated inductor structures were designed and then characterized under probes using the impedance-meter (as depicted in Figure 4.2).

4.3.1 Designed structures

Four inductor structures were designed. Two are single inductors, and the two others are coupled inductors according to the ones listed in Section 2.5. These inductors are using a thin layer of magnetic material (NiFe) to enable high frequency operation.

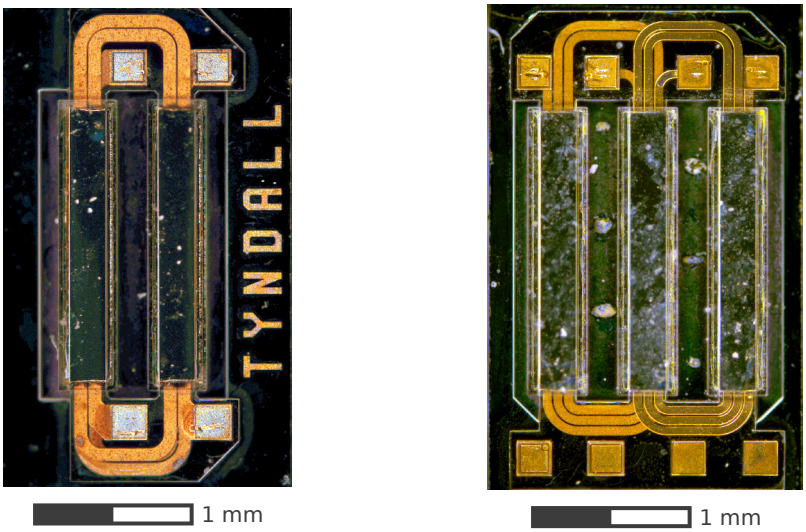


(a) 20 nH inductor. (b) 30 nH inductor.

Figure 4.6 – Micro-photographs of designed single inductors.

Micro-photographs of the single inductor structures are presented in Figure 4.6. They are designed and manufactured by Tyndall National Institute.

They consist of a copper trace disposed as a racetrack and a magnetic core around the traces on the two long sides of the inductor.



(a) 35 nH coupled (k=1) inductors. (b) 45 nH coupled (k=0.4) inductors.

Figure 4.7 – Micro-photographs of designed coupled inductors.

Pictures of coupled inductors are presented in Figure 4.7. The tightly coupled structure (Figure 4.7a) is built with two copper traces stacked and sharing the same magnetic core. The loosely coupled structure (Figure 4.7b) is also built using two copper traces, but only half of each trace shares the same magnetic core.

In addition to these custom designed structures, two commercial inductors from Coilcraft are also used for testing. These inductors are a 36 nH and a 60 nH in 0402 SMD packages, references PFL1005-36NMRU and PFL1005-60NMRU respectively.

4.3.2 Inductor testing

The inductors are first tested using the impedance-meter. All measurements are performed after compensation/calibration procedure. However impedance measurement only allows for harmonic testing. As the inductor will be used

in a switching circuit, inductors should be tested using a square wave voltage stimuli. To address this issue, inductors have been tested with such voltage waveforms and measured in time domain.

4.3.2.1 Harmonic testing

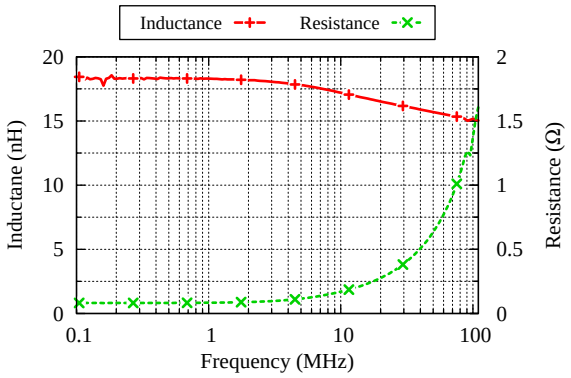


Figure 4.8 – Harmonic characterization of the 20 nH inductor.

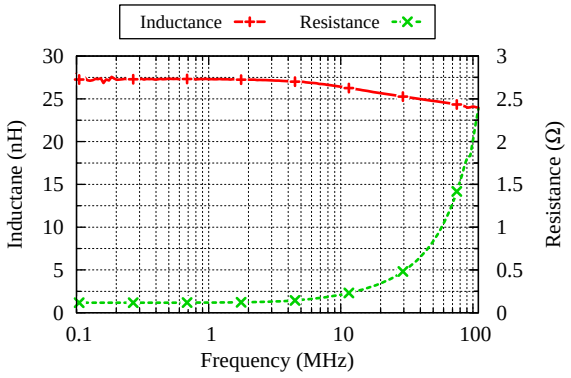


Figure 4.9 – Harmonic characterization of the 30 nH inductor.

Characterization of the single phase structures are presented in Figure 4.8 and Figure 4.9 for the 20 nH and 30 nH respectively. The inductance values of both devices are approximately −10 % lower than the design values. This error can be explained by a variation in the thickness of the magnetic material. The

DC resistance of the 20 nH is 80 mΩ and it is 120 mΩ for the 30 nH inductor, which gives a value of 4 mΩ/nH for both structures.

The frequency behavior is quite similar for the two structures. The inductance value starts to decrease around 4 MHz and the resistance increases simultaneously. Inductance value at 110 MHz is still significant, around 85 % of the low frequency value.

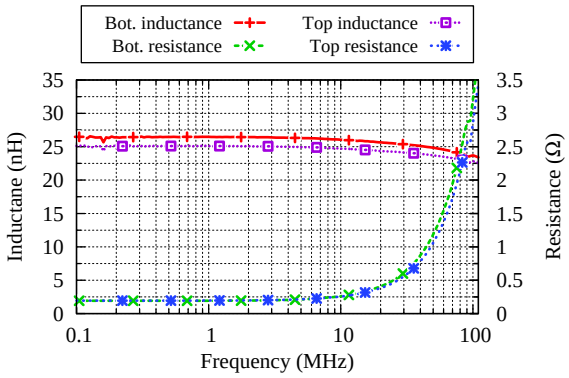


Figure 4.10 – Harmonic characterization of the 35 nH coupled inductor (k=1).

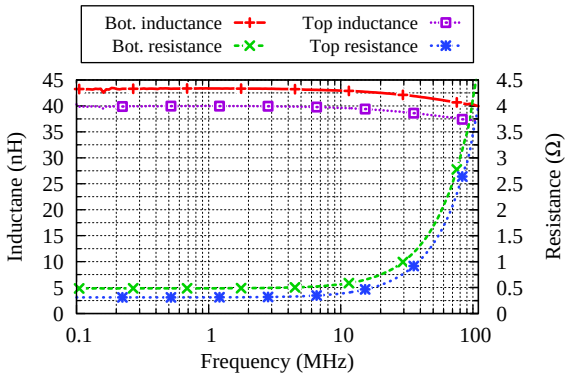


Figure 4.11 – Harmonic characterization of the 45 nH coupled inductor (k=0.4).

For the coupled devices, only self-inductance of each winding has been measured using the impedance-meter. Each winding has been measured as

a single inductor, the other winding being left unconnected. Windings are identified by their physical position inside the device, that can either be top (for the winding above the other one) or bottom (for the winding below the other one). Measurement results are presented in Figure 4.10 and Figure 4.11 for the 35 nH and the 45 nH structures respectively.

In both structures the bottom winding has a slightly higher inductance and resistance value. DC resistance of the 45 nH structure is quite important, almost 10 mΩ/nH. For the 35 nH structure, inductance value is almost 10 % lower than the design value, which might impact the efficiencey figures of the converter. The inductance and resistance values are respectively decreasing and increasing similarly as with the single inductors. This characteristic is expected as these inductors were fabricated using the same process, so frequency performance is similar.

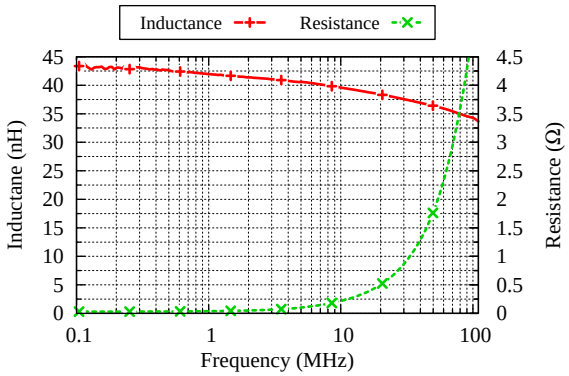


Figure 4.12 – Harmonic characterization of the 36 nH commercial inductor (PFL1005-36NMRU).

The commercial inductor devices are also measured, as their inductance value is given for a frequency around 8 MHz in the datasheet and only DC resistance is available. Characterization gives more accurate data on these devices. Measurement results for the 36 nH and the 60 nH inductors are presented in Figure 4.12 and Figure 4.13 respectively.

These inductors feature a really low DC resistance (30 mΩ for the 36 nH inductor and 44 mΩ for the 60 nH inductor). The DC resistance (around 0.8 mΩ/nH) is much lower than the values of Tyndall devices, but the volume

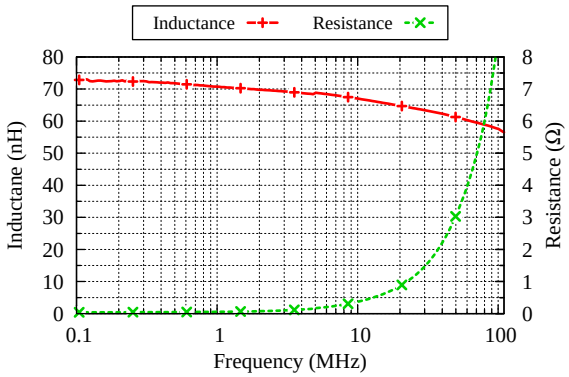


Figure 4.13 – Harmonic characterization of the 60 nH commercial inductor (PFL1005-60NMRU).

of the commercial inductors is higher. Their low frequency inductance value is slightly higher than their nominal value, but their specified inductance value is met around 10 MHz, which was expected. The resistance rises faster with frequency than in the Tyndall devices, meaning the magnetic material/process utilized in the commercial inductor is less suitable for high frequency operation.

4.3.2.2 Time-domain testing

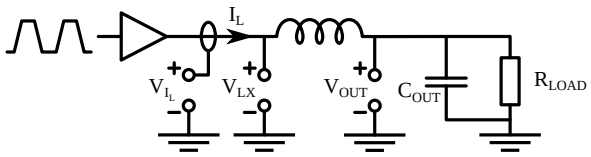


Figure 4.14 – Schematic of the test circuit for the inductors.

Inductor structures are tested in time-domain to evaluate how they would behave in conditions similar to the ones of a buck output filter. Power stage is emulated using a wideband amplifier with high output current capability (TI THS4302 amplifier) and a capacitor and a resistor are added at the output. Capacitor value is 20 nF and resistance load is 10 Ω. Test circuit schematic is presented in Figure 4.14. The current through the inductor is measured

using CT6 probe. Input (V_{LX}) and output (V_{OUT}) voltages at the inductor terminals are measured as close as possible to the inductor to get the true voltage across the inductor. For coupled inductors testing, the same capacitor and resistor are utilized, and a power stage emulator and current sense are added.

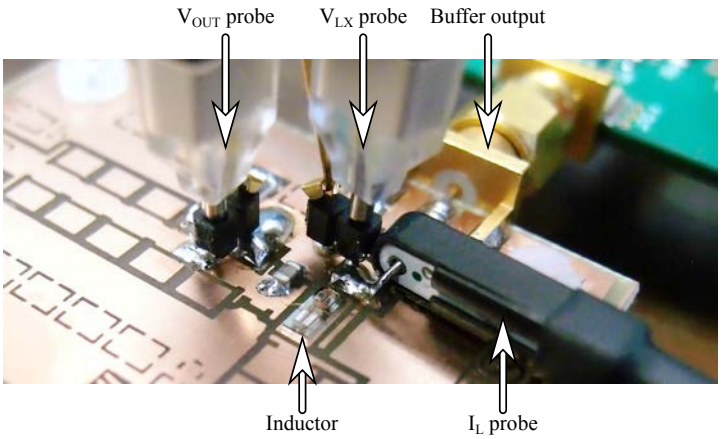


Figure 4.15 – Picture of the test bench for the inductors.

Despite being fairly simple in principle, voltage measurements on this test bench were quite difficult, especially at high frequency. Parasitic inductances combined to capacitance at the input of the voltage probes are creating resonant loops. As the inductor is wire-bonded to the test board, true voltage measurement across the inductor is not possible. Input and output bonding wires are included in this voltage measurement. A picture of the inductor and the probes is presented in Figure 4.15.

With the measurement, it is possible to compute the DC output current (V_{OUT}/R_{OUT}) and the voltage across the inductor terminals ($V_{LX} - V_{OUT}$, noted V_L). Computing the output current is necessary to get the full current through the inductor as the CT6 probe only provides AC measurements. Based on these measurements (current and voltage across the inductor) it is possible to calculate an equivalent inductance and resistance value.

This LR identification is performed using an optimization loop. Current is calculated using L, R values by numerical integration of the voltage waveform.

Current is calculated using a recursive function, defined in Equation (4.1), for a set of I_0, L and R parameters.

$$\begin{cases} I_L[0] &= I_{L,0} \\ I_L[n] &= I_L[n-1] + \Delta I_L[n] \\ \Delta I_L[n] &= \dfrac{\Delta T}{L}\left(\dfrac{V_L[n] + V_L[n-1]}{2} - R \times I_L[n-1]\right) \end{cases} \tag{4.1}$$

Then the equation yields a calculated current waveform, which is compared to the measured waveform using mean square distance. This process is iterated over a list of I_0, L and R values until the mean square distance is minimized. Result of this identification process is presented in Figure 4.16. Calculated current after identification matches well the measured current. An inductance value of 33.4 nH and a resistance of 2.23 Ω are returned. Inductance value is higher (+8 nH approximately) than the value measured with the impedancemeter. This is explained by the fact that in the test circuit some copper traces and the bonding wires located between the two voltage probes are included in the inductor measurement. Few millimeters copper traces and wires are enough to create an error around 10 nH.

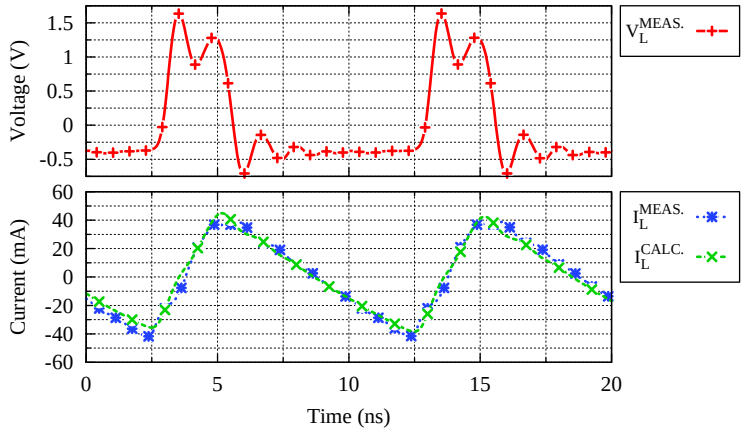


Figure 4.16 – Measurements and calculated waveforms for the 30 nH inductor at 100 MHz, 25 % duty cycle.

Table 4.2 – Summary of identification results at various frequencies for a 30 nH single inductor.

Frequency (MHz)	L (nH)	R (Ω)
5	35.5	0.7
10	34.5	0.9
20	33.9	1.5
50	33.0	1.9
100	33.1	2.2

The coupled inductors were similarly measured and identified. In this case, two interdependent currents are measured, as well as two V_{LX} voltages. Currents are still calculated using recursive formulas, presented in Equation (4.2).

$$\begin{cases} I_{L1}[0] &= I_{L1,0} \\ I_{L2}[0] &= I_{L2,0} \\ I_{L1}[n] &= I_{L1}[n-1] + \Delta I_{L1}[n] \\ I_{L2}[n] &= I_{L2}[n-1] + \Delta I_{L2}[n] \\ \Delta I_{L1}[n] &= \dfrac{\Delta T}{(1-k^2)\,L_1}\left(\dfrac{V_{L1}[n]+V_{L1}[n-1]}{2} - R_1 \times I_{L1}[n-1]\right) \\ & \quad +k\sqrt{\dfrac{L_2}{L_1}}\left(\dfrac{V_{L2}[n]+V_{L2}[n-1]}{2} - R_2 \times I_{L2}[n-1]\right) \\ \Delta I_{L2}[n] &= \dfrac{\Delta T}{(1-k^2)\,L_2}\left(\dfrac{V_{L2}[n]+V_{L2}[n-1]}{2} - R_2 \times I_{L2}[n-1]\right) \\ & \quad +k\sqrt{\dfrac{L_1}{L_2}}\left(\dfrac{V_{L1}[n]+V_{L1}[n-1]}{2} - R_1 \times I_{L1}[n-1]\right) \end{cases} \tag{4.2}$$

Identification process concerns seven parameters in this case, which are the two initial current values, the two inductance values, the two resistance values and the coupling factor. This makes this identification less straightforward than in the single inductor case. Results of the coupled inductors

identification are presented in Figure 4.17. Matching between measurements and calculations is quite fair.

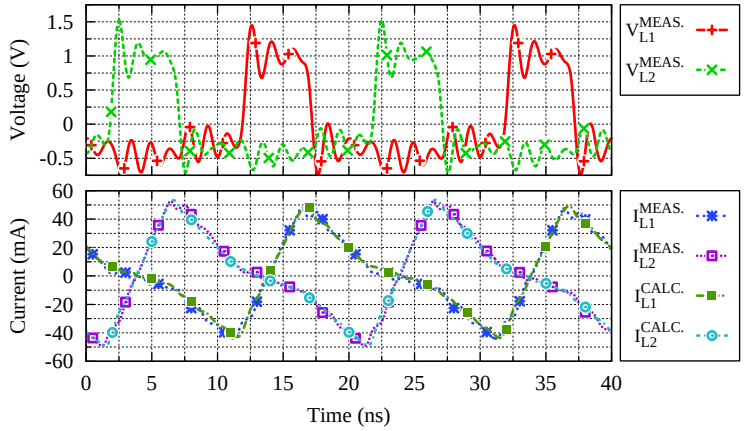


Figure 4.17 – Measurements and calculated waveforms for the 45 nH coupled inductors at 50 MHz, 25 % duty cycle.

Table 4.3 – Summary of identification results at various frequencies for a 45 nH coupled inductors.

Freq. (MHz)	L_{BOT} (nH)	R_{BOT} (Ω)	L_{TOP} (nH)	R_{TOP} (Ω)	k (-)
5	47.9	1.0	44.5	0.8	0.33
10	47.5	1.1	43.7	1.0	0.33
20	47.0	2.0	46.5	1.7	0.32
50	49.2	2.4	45.0	1.5	0.31
100	53.4	3.0	48.7	1.8	0.31

Identification results for single and coupled inductors are presented for various frequencies in Table 4.2 and Table 4.3 respectively. Results are consistent with harmonic characterization, especially for the single inductor. For coupled inductors, when the frequency increases, inductance values tend to increase, which is not an expected behavior. However, identification is not very effective at high frequency. The coefficient of determination (R^2) between calculated

and measured current waveforms is below 0.9 at 100 MHz for the coupled inductors, meaning that identification might not be very accurate. This is due to the non-linearities of the magnetic inductors that are not taken into account during identification.

The identification gives information on the coupling factor, which is around 0.33. Since parasitic inductances are added on each phase (due to copper traces and bonding wires) the true coupling factor value is a bit higher than the one from the identification. As it was designed to be around 0.4, measurements are consistent.

These time-domain measurements have shown that harmonic measurements and simple LR model of the inductor can be sufficient. This validates the model that was utilized during the specification and design of the output filter.

4.4 Converter

This section details the various test configurations and the associated measurements. The testing is divided in two categories: the single die testing and the full converter assembly testing.

4.4.1 Single die

Only the die with the standard converter was available as a standalone chip. Thus single die test setup and measurements are not available for cascode power stage.

4.4.1.1 Tests setup

The tests with the single die have two major objectives: first validate the functionality of the designed IC, and second do a preliminary performance assessment. Two PCBs were designed for this, and the die was assembled using wire-bonding. As the die includes two converters, both converters were connected. A picture of the chip-on-board assembly is presented in Figure 4.18.

Decoupling capacitors are 0402 commercial capacitors from Murata, with values chosen to be close to the interposer capacitor values. Inductors are the

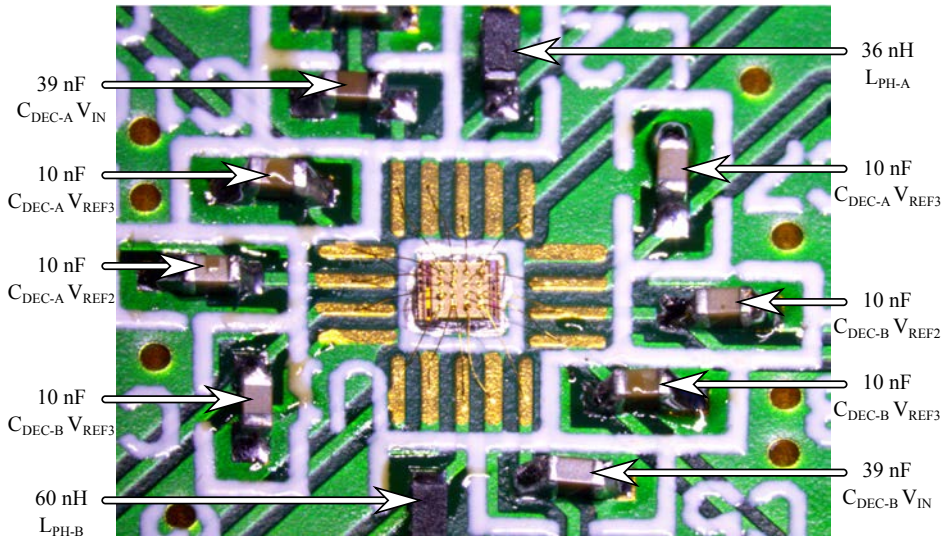


Figure 4.18 – Picture of the test-board for the single die measurements.

same as the ones tested in Section 4.3. Components references are presented in Table 4.4

Table 4.4 – References of inductors and capacitors used on test-boards.

Reference	Manufacturer	Value	Function
GRM155R71C393KA01D	Murata	39 nF	Input decoupling
GRM155R71C103KA01D	Murata	10 nF	Drivers decoupling
GRM155R71C183KA01D	Murata	18 nF	Output decoupling
PFL1005-36NMRU	Coilcraft	36 nH	Power inductor
PFL1005-60NMRU	Coilcraft	60 nH	Power inductor

Capacitors are placed as close as possible to the die for effective decoupling. However, ceramic capacitors with high values do no have a very good high frequency performance. There is a risk that decoupling is not done properly due to resonance issues.

Test-boards are equipped with voltage probing points at V_{LX} and V_{OUT} nodes. Furthermore the connection of the CT6 current probe in series with

the power inductor is available in a test configuration for validation purposes.

4.4.1.2 Measurements

The first measurements showed that the converter was operating properly. Main waveforms are presented in Figure 4.19 for 100 MHz switching frequency and high impedance load, i.e. no output DC current. The 200 MHz version is measured at 100 MHz switching frequency as decoupling using ceramic capacitors does not allow for such high frequency testing. In terms of switching waveforms, both versions are very similar.

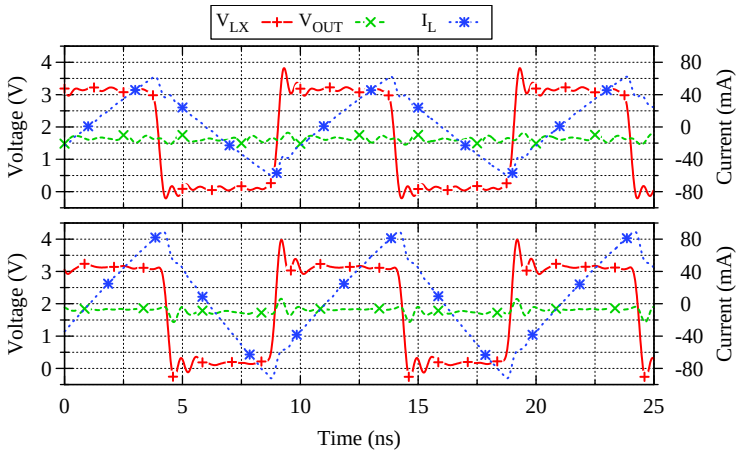


Figure 4.19 – Measured voltage and current waveforms on the two standard converters, 100 MHz version on top, 200 MHz version at the bottom.

The parasitic coupling between nodes is very problematic to achieve precise measurements. This major issue is illustrated by Figure 4.20. It shows the measured waveform of the output voltage of the 100 MHz converter in two cases: at the top when the V_{LX} node is probed, and at the bottom when it is not. Probing the V_{LX} node generates a lot of high frequency oscillation at the V_{OUT} node. This can be explained by the fact that the probing circuit can be modeled as an LC circuit (input impedance in series with parasitic inductance) and adding this LC circuit at the V_{LX} node has a significant impact on the converter. The issue of parasitic interconnection components is further discussed in the case of the 3D assembly in Part 4.4.2.

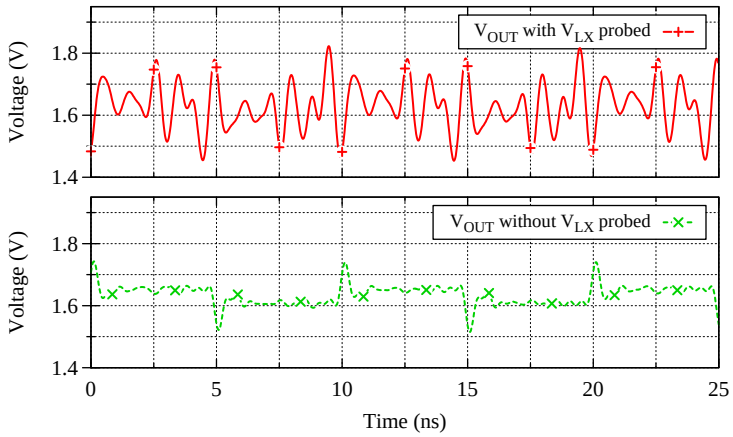


Figure 4.20 – Measured output voltage when the V_{LX} node is probed (top graph) and when the V_{LX} node is not probed (bottom graph).

A way to circumvent the probing issue would be to use on-chip voltage sense circuit (fully optimized in simulation for low loading of the circuit) that could be then probed without impacting the behavior of the converter. How-

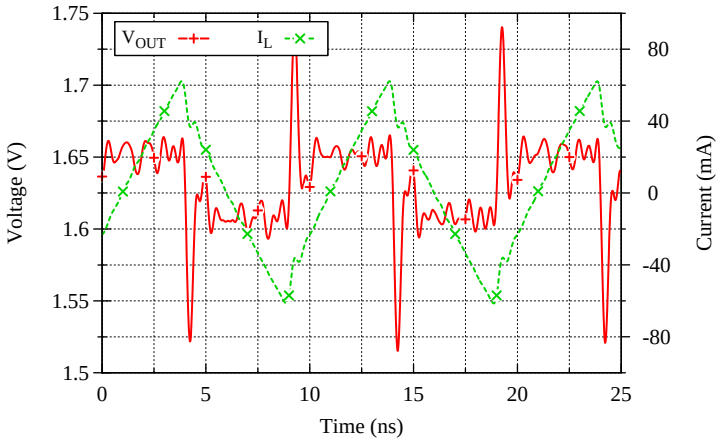


Figure 4.21 – Measured output voltage and inductor current at 100 MHz switching frequency.

ever this approach requires a full re-design of the chip, which could not be done here.

A close-up view on output voltage (along with inductor current) is presented in Figure 4.21. Output voltage is approximately a square wave, centered around 1.63 V with an amplitude of ±25 mV approximately. Having a square wave voltage means that the main contributor to the voltage ripple is the parasitic inductance – if it were the parasitic resistance, voltage would be triangular, and if it were the capacitor, voltage waveform would be parabolic. It is possible to estimate this parasitic inductance. Current slope is approximately 24 mA/ns, which generates a voltage change across the inductor of 25 mV approximately. Parasitic inductor is then close to 1 nH. This confirms the fact that ceramic capacitors have too high parasitic inductance for proper high frequency operation.

Following the functional validation and the time-domain measurements, a test bench has been set up for steady-state performance primary assessment. As the demonstrator here is not the final one, no in-depth analysis is presented. Efficiency and losses figures are further detailed using measurements on final assembly.

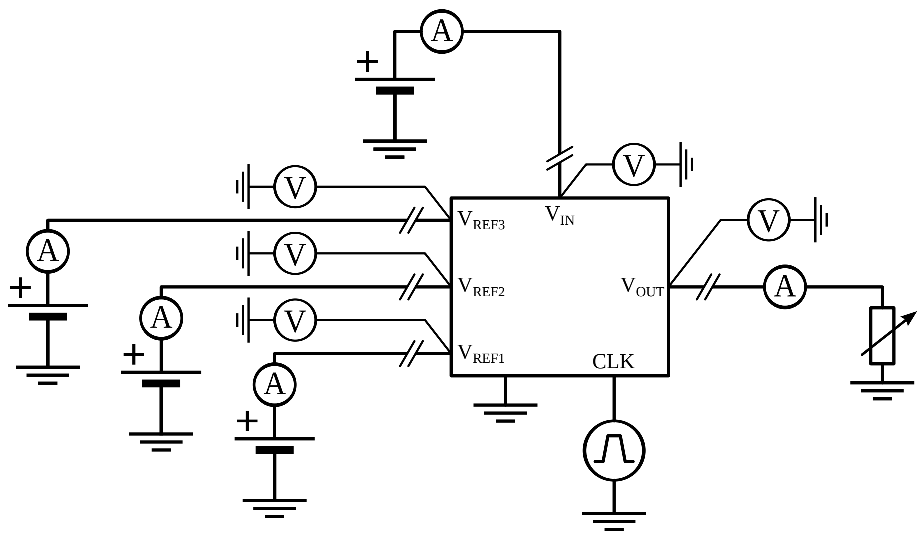


Figure 4.22 – Synoptic of the performance measurement test-bench.

A simplified schematic of the performance measurement test-bench is presented in Figure 4.22. The converter (with decoupling capacitor and output inductor) is seen as a black box, with four voltage inputs, one clock input and one voltage output. Four independent voltage sources are utilized for measurements, of which both current and waveforms are monitored. Due to the length of connection wires, it is a fair assumption that current is considered continuous through all voltage sources. Thus measurement is carried out in DC. Voltage is sensed as close as possible to the converter. It is also sensed in DC. Load is a programmable electronic DC load that emulates a constant resistor. Power from the clock generator is not monitored.

All devices are driven by a software that sets up and measures the current and voltage values of all sources and the load. Using a software allows for exhaustive measurements. The 100 MHz version of the converter with the standard power stage has been measured for a given set of switching frequency, duty cycle and load current. Frequency was swept from 60 MHz to 130 MHz every 10 MHz, duty cycle from 20 % to 80 % every 5 % and load current from 0 mA to 400 mA every 50 mA, with the addition of 5 mA, 25 mA and 75 mA specific values.

The evolution of the output voltage with the duty cycle is presented in Figure 4.23 for various load currents and switching frequencies. In an ideal buck converter, all the curves should be superimposed straight lines. However due to IR-drop across switches and inductor, output voltage decreases with the current. The issue highlighted in Figure 4.23 is that some curves are not straight lines at all, meaning that the converter doesn't operate properly. This is highly visible at high load current, and especially at 70 MHz and 130 MHz switching frequency. An erratic behavior is observed, meaning that the converter is not switching properly. As it appears mostly at high load current, it is probably due to the input decoupling capacitor: as it features a high ESL, a high current is drawn and makes the voltage drop, so the high-side switch has its V_{GS} voltage that decreases, making the switch to close. Unwanted resonance effects also play a role in this behavior as it appears most at specific frequencies. Unfortunately measuring such effects is impossible as any probing on the system would change the system itself (e.g. add the input capacitance of the probe) and alter its behavior. Buck converter at high frequency is prone

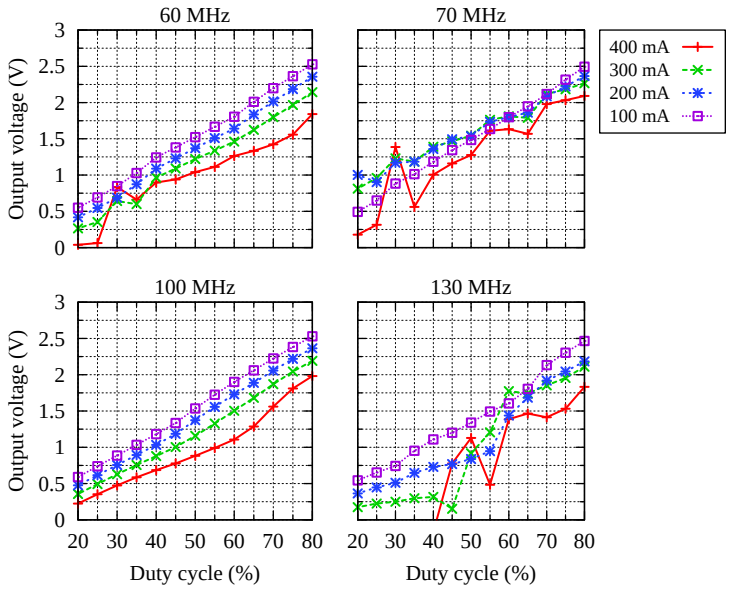


Figure 4.23 – Output voltage evolution of the converter on board with duty cycle for various switching frequencies and load currents (100 MHz standard converter).

to chaotic behavior and bifurcations are possible. This was not explored.

Converter operates relatively well around 100 MHz and below 400 mA. Performance can then be assessed using a restricted set of switching frequencies. Figure 4.24 shows the evolution of each losses contributor with frequency at 150 mA load current, 1.65 V output voltage ($V_{IN}/2$). Losses of the high-side (HS) and low-side (LS) drivers are proportional to frequency, which was expected. Power stage losses include the output filter losses. They seem to decrease first and then increase. This means that some losses are due to ripple (which decreases linearly with frequency) and some to capacitance charging and discharging (which increase linearly with frequency). However due to the issues seen in Figure 4.23, no definitive conclusion can be made based on these measurements.

Efficiency of the converter has been evaluated based on losses measurements (drivers, power stage and output filter). Results are presented in Fig-

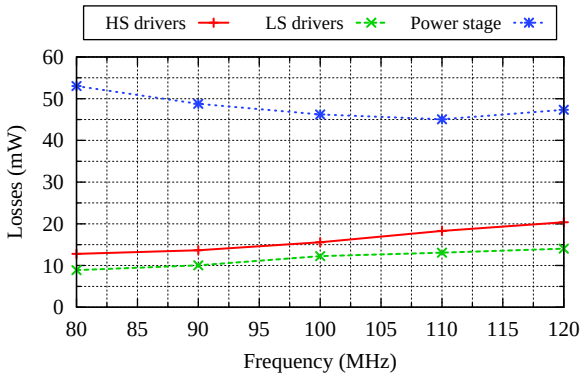


Figure 4.24 – Losses breakdown at 150 mA load current, 1.65 V output voltage ($V_{OUT}/V_{IN} = 0.5$), 2 V drivers' voltage swing.

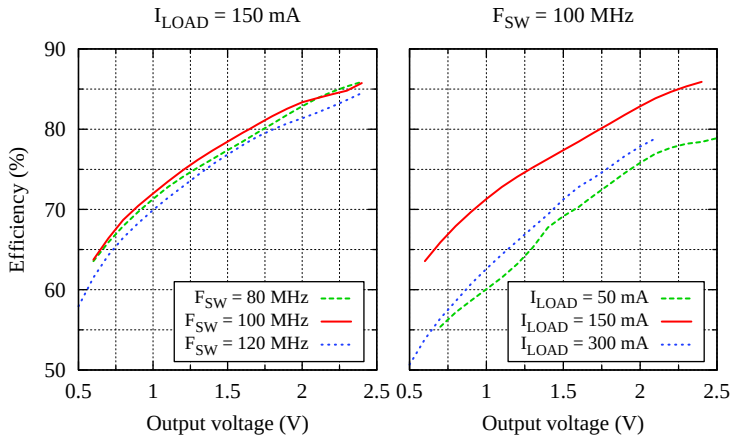


Figure 4.25 – Efficiency measurements for various output voltages, switching frequencies and load currents.

ure 4.25. Best efficiency results are achieved for 150 mA load current, which is consistent as the 100 MHz converter has been optimized for 140 mA load current. The efficiency curves also show some variations due to weak decoupling capacitor issues. Efficiency results are expected to be better in the assembly using the capacitive interposer. No comparison with simulation is presented here because of the unreliable operation of the converter. More comprehensive

measurement results are presented in the case of the 3D assembly.

4.4.2 Interposer assembly

Following the preliminary tests of the IC, the die was flipped on top of the capacitive interposer. Both cascode and standard power stages were assembled this way.

4.4.2.1 Tests setup

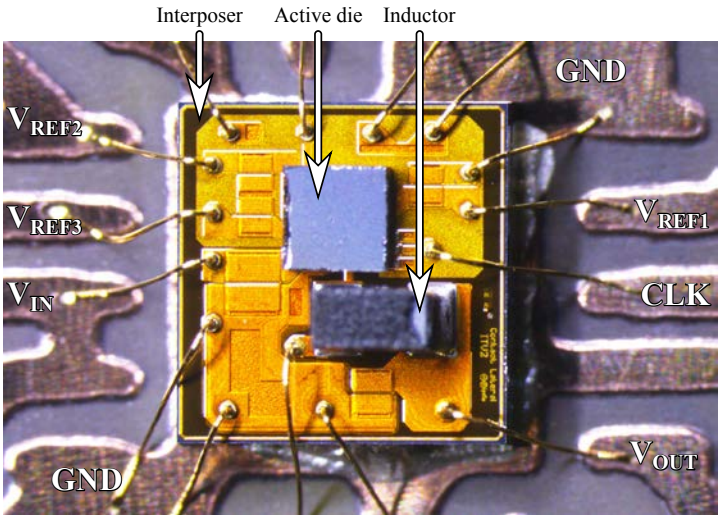


Figure 4.26 – Micro-photograph of the converter assembly on interposer.

A picture of the assembly is presented in Figure 4.26 with the names of the various inputs/outputs. The converter assembled onto the interposer uses the same 0402 SMD inductor as in the previous tests. The interposer/IC assembly is then wire-bonded on a test-board that allows for easy connection with the various inputs and outputs. A picture of the test-board is presented in Figure 4.27. All configurations (100 MHz/200 MHz and standard/cascode power stages) are using the same test-board. Doing so makes the comparison effective as only ICs and/or inductors are changed.

For performance measurements the same bench as the one for the chip on-board is utilized (see Figure 4.22 on page 178). Furthermore no additional

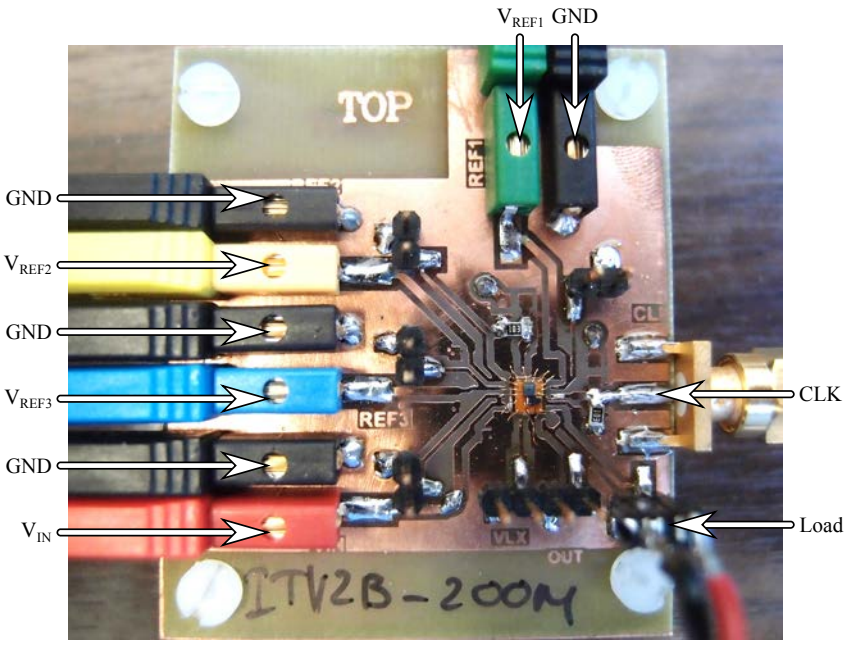


Figure 4.27 – Test-board utilized for full converter measurements.

passive components are added on the test-board. As capacitors embedded in the interposer are similar in value as the decoupling capacitors used on the test-board, comparison between the two assemblies is possible, allowing to quantify the gain from using very close deep-trench capacitors.

A equivalent schematic of the test setup is proposed in Figure 4.28. Main parasitic inductances and capacitances are put on the circuit. Only main input voltage and output are considered, the three voltage references were not added for the sake of readability. Critical parasitic elements are the two V_{LX} capacitances ($C_{D-V_{LX}}$ and $C_{I-V_{LX}}$) that generate oscillations and losses at the V_{LX} node. Parasitic capacitance between V_{OUT} and V_{LX} ($C_{I-L_{PH}}$) creates unwanted high frequency coupling between these two nodes. All parasitic ground inductances also require to be minimized to avoid voltage ringing. At the probe end, both access inductances and input capacitance make it difficult to properly measure any time-domain waveform. However the 3D assembly still presents better characteristics in terms of parasitic interconnection than

the on-board assembly.

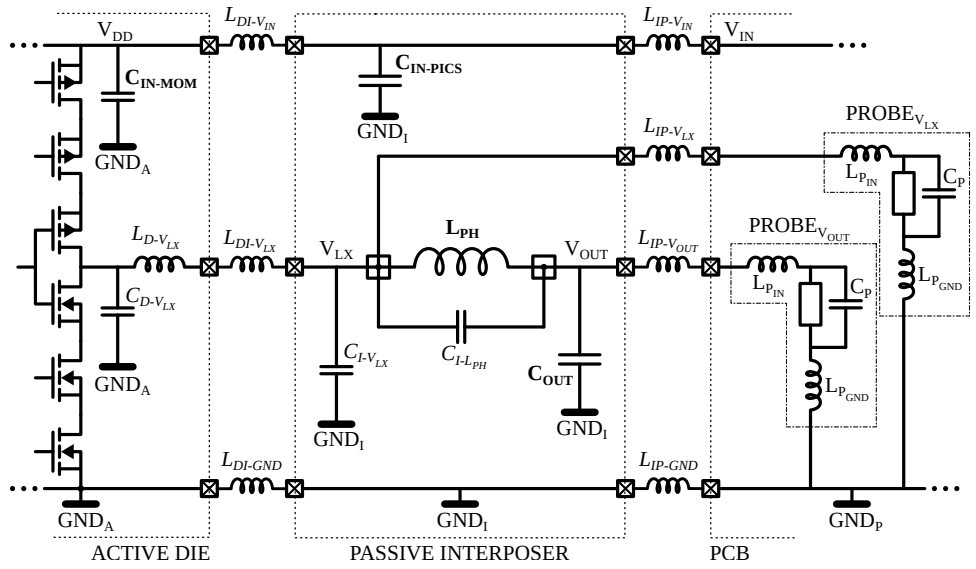


Figure 4.28 – Equivalent circuit with main parasitic interconnection components of the interposer 3D assembly connected to test-board.

4.4.2.2 Measurements

Measurements have been carried out on several configurations. Presented measurement results focus on the followings:

- 100 MHz standard power stage, allowing for performance comparison with board assembly,
- 100 MHz cascode power stage, allowing for performance comparison with 100 MHz standard power stage,
- 200 MHz standard power stage, allowing for performance comparison with 100 MHz standard power stage.

Figure 4.29 shows the measured waveforms of the standard power stage (top graph) and the cascode power stage (bottom graph). They were measured

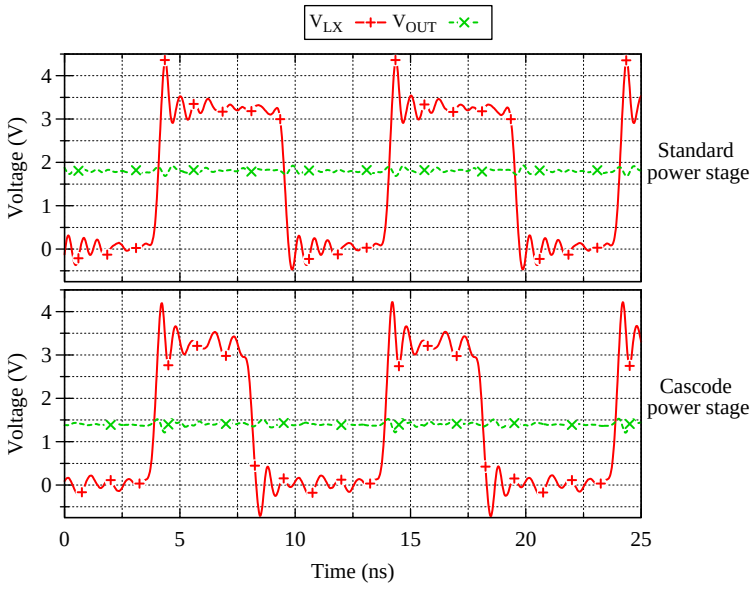


Figure 4.29 – V_{LX} and V_{OUT} voltage waveforms of standard and cascode converters.

in the same conditions. The difference in duty cycle is that the cascode power stage has an output voltage with a duty cycle complemented with respect to clock input, which is not the case for standard power stage. In both cases output voltage was measured when the V_{LX} probe was disconnected. What is remarkable is that it is impossible to distinguish cascode power stage from the standard power stage only by looking at voltage waveforms. This confirms that the MOSFETs in series in the cascode power stage are effectively acting as a single macro-switch.

References voltages have been measured for both power stage structures. Waveforms are presented in Figure 4.30. For the standard power stage, the high-side driver is supplied between V_{REF3} and V_{REF2} (respectively set at 3.3 V and 1.3 V for a 2 V swing) and the low-side driver between V_{REF1} (set at 2 V) and the ground. For the cascode power stage, V_{REF3}, V_{REF2} and V_{REF1} are respectively set to 3.3 V, 2.2 V and 1.1 V. On the cascode power stage, voltages are much less oscillating than on the standard power stage. As

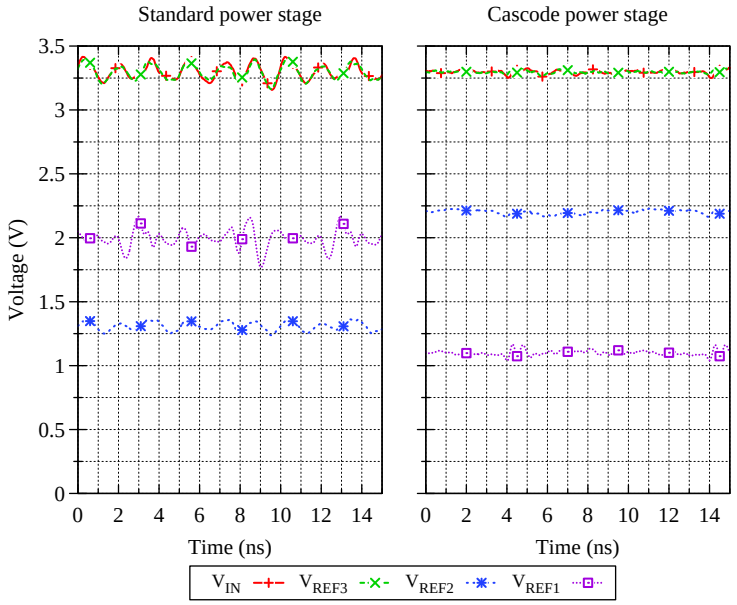


Figure 4.30 – Input and reference voltages waveforms for both standard and cascode power stages.

the physical configuration is the same in both cases, this can be explained by the fact that the drivers of the cascode power stage require less peak currents than the ones of the standard power stage. The $^{\mathrm{d}I}/_{\mathrm{d}t}$ is thus limited compared to the standard power stage. As for the main input voltage V_{IN}, it shows less oscillations in the cascode power stage as the capacitance between the V_{IN} node and the V_{LX} is much lower in the case of the cascode power stage than in the case of the standard power stage. This is due to the fact that in the cascode power stage, drain-to-source capacitance of MOSFETs are put in series, thus the resulting values are divided by three.

It is also remarkable that in both cases, V_{IN} and V_{REF3} are almost identical. This can be explained by the fact that these two voltage nets are routed very close to each other (both on the interposer and on the test-board) making them capacitively coupled.

Despite some high frequency oscillations, reference voltages are fairly constant. The capacitance value of 10 nF for the reference voltages decoupling

seems then a satisfactory value.

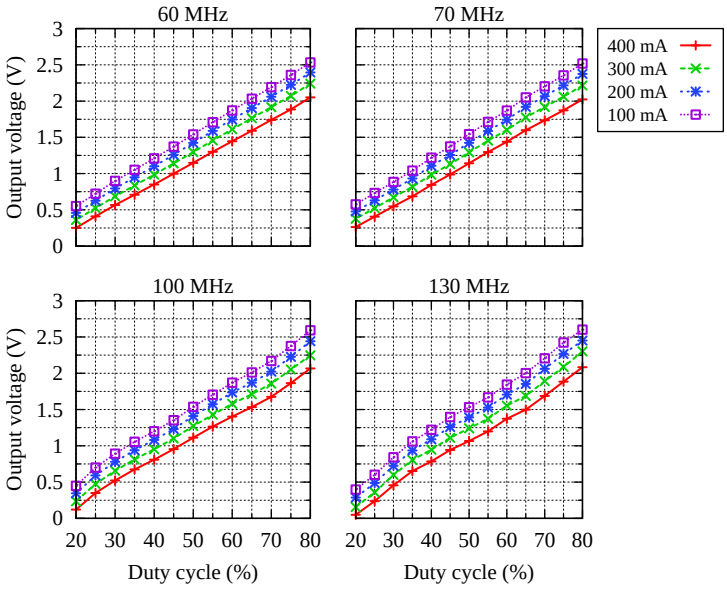


Figure 4.31 – Output voltage evolution of the on-interposer converter with duty cycle for various switching frequencies and load currents.

Similarly to the on-board converter, the output voltage for various duty cycles, load currents and switching frequencies has been measured for the standard converter on interposer. Measurement results are presented in Figure 4.31. Compared to results in Figure 4.23, here output voltage is consistent with duty cycle and load current. Each curve is a straight line (for all measured currents and frequencies) meaning that decoupling with the interposer is effective in any condition. This observation confirms the need for very close, low-ESL decoupling capacitors when it comes to very high-frequency switching converters.

The 100 MHz versions of converters with standard and cascode power stages are compared in terms of losses for various load currents and switching frequencies. Results are presented in Figure 4.32, including measurements and Post Layout Simulation (PLS) results. The standard converter has been measured up to 130 MHz and the cascode converter up to 150 MHz. Drivers'

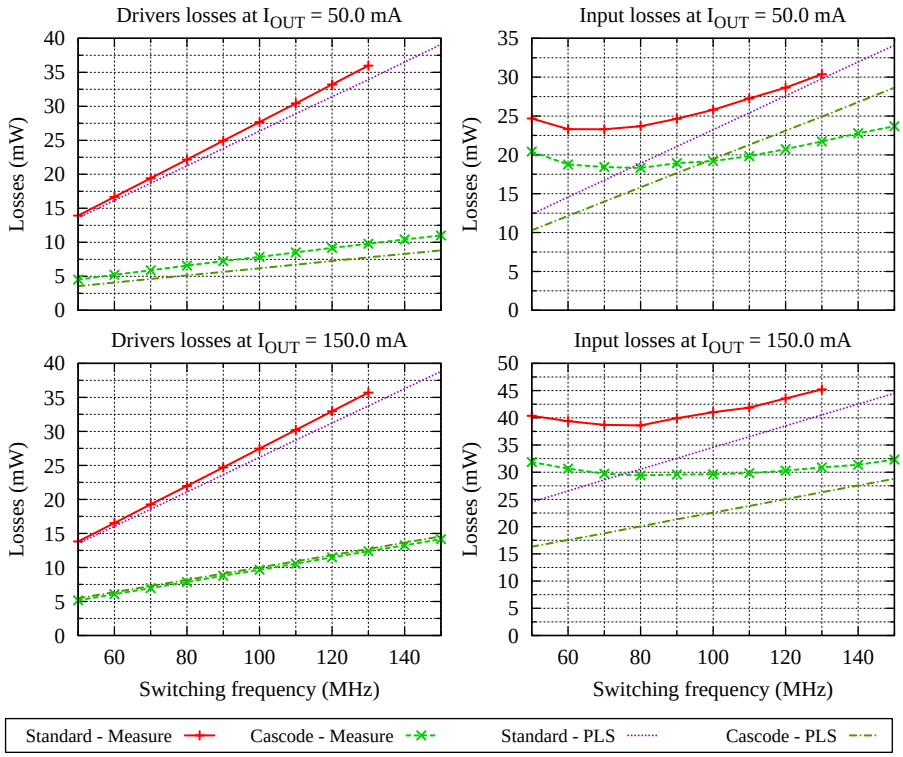


Figure 4.32 – Losses of standard and cascode converters at 1.2 V output voltage.

losses and main input losses (including power stage only losses and output filter losses) are presented. In all cases, losses in the cascode converter are smaller than losses of the standard converter. The drivers' losses of the standard converter are independent of the load current, whereas drivers' losses of the cascode power stage are slightly increasing with the load currents. Both behaviors were observed in PLS. The increase in drivers' losses with the frequency is much less important for the cascode power stage than for the standard power stage, meaning that gate capacitances of the MOSFETs are less.

On the input losses side, as both test structures (standard and cascode) are using the same output filter, losses difference is only due to power stage. The difference is explained by the fact that the cascode power stage has a

lower drain-to-source capacitance and resistance, thus switching and conduction losses are decreased. At 150 mA load current, as conduction losses increase, the advantage of cascode power stage is clearly seen. These results confirm that the three low-voltage MOSFETs in series are exhibiting a better switching/conduction losses figure of merit (presented in Part 2.3.2) than a single 3.3 V device.

For the drivers, measurements are very close to post-layout simulations. As post-layout simulations were performed using ideal voltage sources, this means that decoupling is efficient, and voltage oscillations seen in Figure 4.30 do not affect the operation of the drivers in a critical way. On the main input losses, there is a relatively important difference, especially at low frequency. This is because in PLS, inductors are considered as constant, ideal current sources (for simulation runtime considerations), so no current ripple is simulated, as well as no inductor losses. This impacts the RMS current value that goes through the switches, as well as the discharging of the output capacitor through the low-side switch when the inductor current becomes negative, which happens at low load current and switching frequency. Offset between PLS results and measurement results can be explained by the fact that PLS doesn't take into account the inductor ESR and the parasitic resistances due to interconnection. A parasitic resistance is introduced when connecting the active die to the interposer (resistance of a micro-bump), and also when connecting the assembly to the test-board (resistance of a bonding wire).

Power consumption of the converters has been measured when no clock signal is applied. Measured losses are then the DC losses of the converter. These losses include the current source and the level-shifter's power consumption, as well as leakage currents. As reference voltages of the two on-chip converters are internally connected, measurements take into account both converters. This is not a critical issue because the two on-chip converter are using the same current source and level-shifter. DC losses of a single converter are then directly half of the measured losses.

Table 4.5 compares the post-layout simulation results to the measurements. DC losses of standard and cascode converters are similar. For the standard converter, measurements are in-line with PLS results. However, this is not the case for the cascode converter. Simulation seems to be pessimistic. The issue

Table 4.5 – DC losses of standard and cascode power converters.

	PLS	Measurements
Standard converter	419 µW	434 µW
Cascode converter	461 µW	350 µW

could be that due to process variation, absolute current values are not the ones that were simulated. As only one device is measured, it is very difficult to confirm (or invalidate) this conclusion.

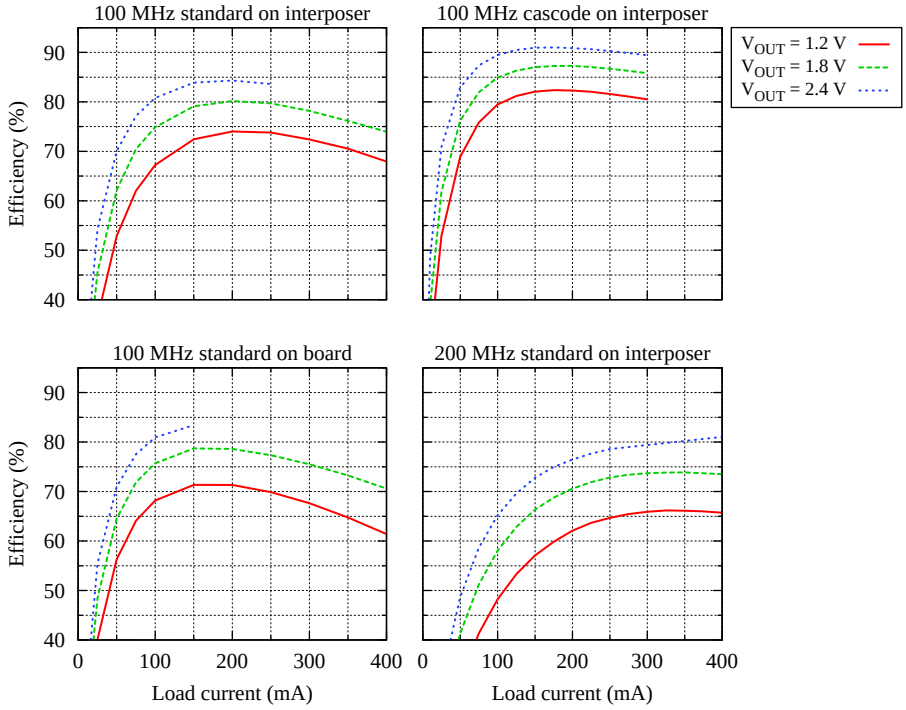


Figure 4.33 – Efficiency comparison of the measured converters.

Global efficiency results against load current are presented in Figure 4.33. Efficiency is calculated from losses measurements at 2.4 V, 1.8 V and 1.2 V output voltages. The standard converters have been characterized up to 400 mA

and the cascode converter up to 300 mA. For an output voltage of 2.4 V, the efficiency curve of the standard converter on interposer stops at 200 mA, and at 150 mA for the standard converter on board. This means that an 80 % duty cycle is not sufficient for 2.4 V output at these load currents. The cascode converter presents significantly higher efficiency results than the other converters for all output voltages. This result is the logical consequence of the losses measurements presented in Figure 4.32.

Thermal images of the converter are presented in Figure 4.34. They were acquired using an infrared camera *IR FlexCam® Ti55*. No precise calibration was carried out, as well as no non-reflective layer was deposited on the assembly. These two actions are necessary for precise, quantitative thermal imaging. This is no limitation as only qualitative information were sought from the following images. These thermal image are acquired for various switching frequencies and load current configurations. The upper right one is when the converter is off, so its temperature is uniform. Copper is reflecting some infrared, but interposer assembly seems to have fairly uniform emissivity. The two images in the middle are when the converter is switching, but no load current is drawn. At 100 MHz, hot spot is the inductor, losses are due to current ripple. At 200 MHz, IC heats a bit, but inductor heats even more. As ripple should decrease, losses inside the inductor are supposed to be caused by dynamic losses in the magnetic material. Heating of the IC is caused by switching losses, which are doubled compared to 100 MHz. The last row shows the temperature at 150 MHz for both 200 mA and 400 mA load currents. At 200 mA load current, IC does not heat much, and inductor is the hot spot. In this configuration, temperature is equivalent to the 200 MHz switching frequency but at no load current. At 400 mA, the assembly starts to heat up more. Conduction losses are increased by a factor of four compared to the previous case. Inductor is still the hottest spot, as conduction and hysteretic losses are adding up. However, the temperature increase is less than 20 °C over the ambient temperature, validating the fact that no cooling system is required.

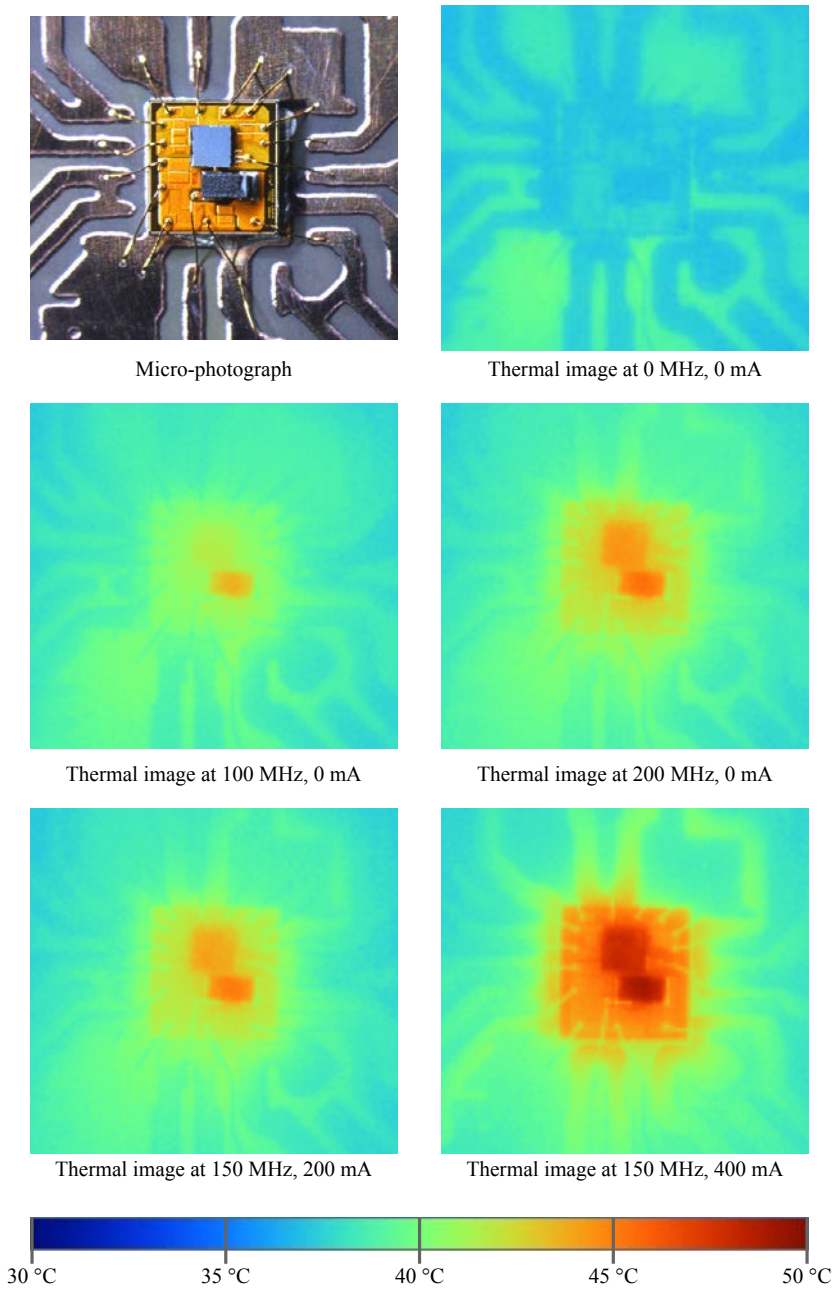


Figure 4.34 – Thermal images of the standard, 200 MHz converter.

4.4.3 State-of-the-art status

Measurement results are then compared to the current state-of-the-art of integrated DC-DC converters. State-of-the-art data is based on presented landscapes in Part 1.3.1.3. A comparison of the demonstrated results against the state-of-the-art is proposed in Figure 4.35. Efficiency is plotted against the conversion ratio (V_{OUT}/V_{IN}) and data points are categorized with respect to the switching frequency of the converter.

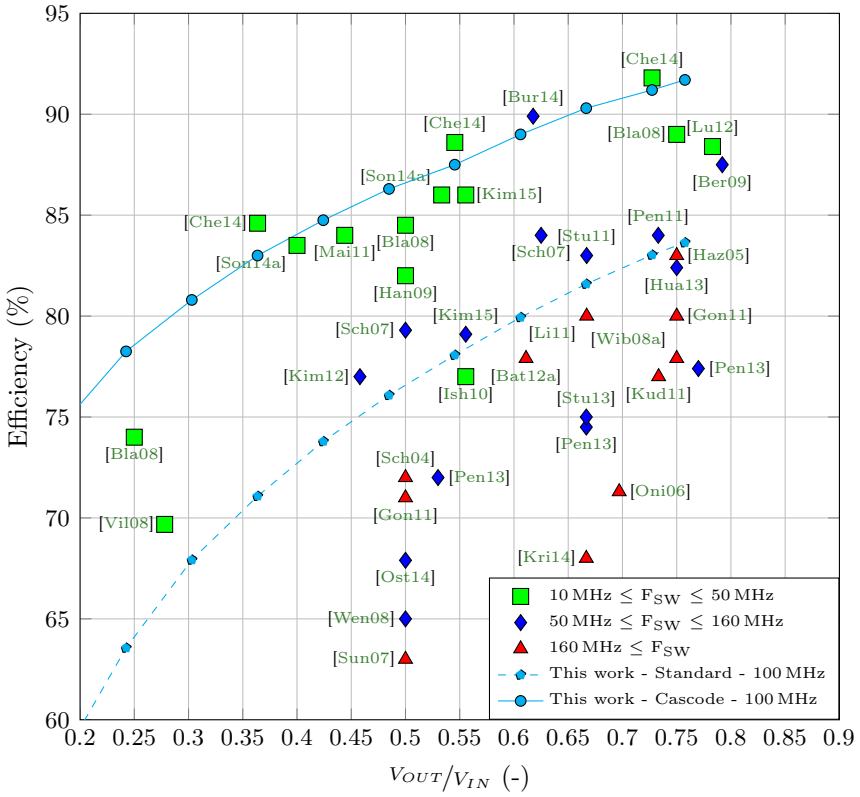


Figure 4.35 – Efficiency versus conversion ratio of demonstrated converter along with state-of-the-art results.

The designed standard converter displays figures that are in-line with the state-of-the-art. Measured efficiency figures are close to the achieved efficiency of the mid-switching frequency (between 50 MHz and 160 MHz). This is an

expected result, as no specific care was taken to push the efficiency of this particular converter. Efficiency of the cascode converter is overall 8 % higher than the standard converter. Measured efficiency is then comparable with low-switching frequency converters (from 10 MHz to 50 MHz). These efficiency results validates the interest of the 3-MOSFETs cascode power stage structure for DC-DC power conversion. Being able to operate at higher switching frequencies reduces the required passive components values, impacting the area in a positive manner (for given passive components technologies).

4.5 Conclusion

Testing issues have been presented, as well as the impact and the limitations of the measurement equipment. These considerations are essential to assess the validity of the measurement results. Test setups were developed by taking into account these issues, and results were critically analyzed.

The developed tests and presented results allowed to validate independently each converter constituent, and then system-level measurements assessed the converter performance. The interposer has demonstrated to be much more efficient for high frequency decoupling than the classical on-board passive components, allowing for a proper behavior of the converter up to 200 MHz switching frequency. System-level measurements using the magnetic inductors developed in the frame of the project have not been carried out, but their characterization can give some insights on their behavior. Compared to the commercial inductors, they should be a bit more lossy (as they feature higher DC resistance) but provide better high frequency decoupling due to their better high frequency characteristics.

In the end, the interest of the cascode power stage has been clearly demonstrated based on exhaustive measurement results. A comparison with the state-of-the-art confirms this interest, as efficiency of the cascode structure is comparable with the one of the converters switching at a frequency a decade below.

Chapter 5

General conclusion

The work supports the demonstration of a high-switching frequency SMPS with a significant efficiency. From Chapter 1 it was identified the idea of a coupled-inductor multi-phase buck converter. In the frame of the project, the goal was then to validate experimentally the feasibility of a two-phase buck converter. Early design analyses have pointed out the superior performances of standard, 1.2 V core digital MOSFETs but unable to sustain a 3.3 V input voltage. Though not new the cascode configuration was selected. Besides literature was lacking experimental results about the selected configuration.

5.1 Summary of contributions

The proposed cascode converter addresses some key issues faced within integrated DC-DC converters. Main contributions are the following:

- The choice of converter architecture is a key issue in the design process. Some insights on this issue have been developed and presented in Chapter 2, focusing on high-switching frequency considerations.
- When chosen or imposed, the silicon technology significantly impacts the resulting converter. A methodology for analyzing and choosing the best candidate silicon technology is developed in Chapter 2. Despite using simple models the methodology has demonstrated effectiveness, i.e. results prove agreement with simulations.
- An innovative broad power stage structure has been validated in Chapter 4 after design in Chapter 3. A significant performance gain has been demonstrated compared to a classical approach for a similar technology.

- An original 3D assembly has been tested in Chapter 4 and compared to a classical approach, justifying the interest of a 3D structure for very high frequency power supplies.
- Finally Figure 4.35 (page 193) establishes that the broad power stage structure is capable of similar performances as structures operating a decade of switching frequency below but with significantly lower passive component values. The footprint is thus positively impacted.

The presented work addressed the major issue of designing high voltage power electronics using low-voltage, digital core MOSFETs of a CMOS technology. This strategy further enables the possibilities of on-chip voltage regulation (thanks to core digital devices) but does not prevent to deliver improved Power Management Units (PMUs).

5.2 Perspectives

The access to silicon has limited this study to an open-loop structure for it was more relevant to assess the feasibility of a cascode power stage in a 3D assembly. The work may not be qualified as "definitive". Future works may be foreseen to address short-term issues. Based on the expectations of these near-future activities, the concept can be projected further in mid-term and long-term future activities. A road-map of these perspectives is presented in Figure 5.1, and each step is further detailed in the following paragraphs.

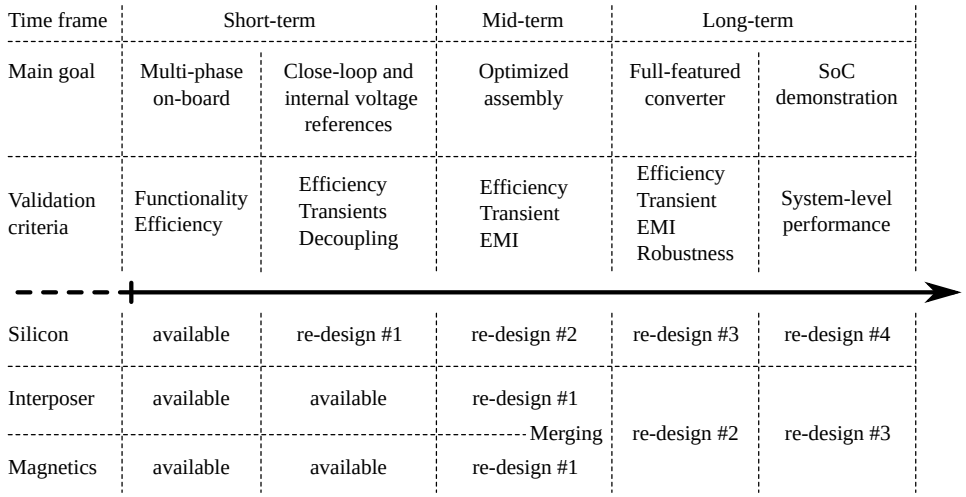


Figure 5.1 – Road-map of perspective activities.

5.2.1 Short-term issues

Optimized test setups are worth the effort as they will provide a better environment to existing DC-DC samples for the goal of more accurate time-domain measurement. It was shown the impact of parasitic passive component on waveforms and the parasitics due to the test-board should be eliminated as much as possible.

On-board multi-phase testing necessitates to report two DC-DC samples on a test-board. Due to parasitic interconnection components, the experiment is expected to assess only the validity of the concept, i.e. the comparison of the several coupled inductor structures as discussed in Part 2.4.2.2.

Close-loop control is mandatory to achieve a so-called DC-DC converter. A new silicon test-chip is needed but can be designed so as to accommodate existing interposer and magnetic devices. The goal of experiment is to measure transient performances and verify impact of control loop on the overall efficiency. Several control schemes are possible and a study will be welcome prior to design to select the appropriate one.

On-chip voltage references should replace the current off-chip DC supplies. A 3:1 switched-capacitor ladder is suggested to provide $V_{DD}/3$ and $^2V_{DD}/3$ on-chip. The goal of experiment is to verify the impact on efficiency as this specific switched-capacitor converter has been already demonstrated.

5.2.2 Mid-term issues

Optimized 3D assembly is expected to verify multiple issues. The current interposer is not optimized for the sake of measurements. Besides magnetic components are soldered on the interposer, and not fabricated on the interposer. Optimizing the interposer for the two latter goals will provide a kind of definitive DC-DC converter. Of course a two-phase structure with adequate control is expected. Nevertheless a four-, or even eight-phase structure, could be considered so as to get a comparison more straightforward with the state-of-the-art result in [Bur14].

Improved silicon chip is an issue to consider with the here above perspective. The reliability of the cascode structure operation should be more extensively addressed. In particular it has not been tested how sensitive it is to EMI aggressions. Probably some protection schemes have to be implemented. In the same order of consideration, a specific Electro-Static Discharge (ESD) protection scheme has to be developed and tested. Obviously all improvements at silicon level (on the active side) must be put in perspective with the design of the interposer. A co-design approach may be fruitful to some extent.

5.2.3 Long-term issues

Full-featured converter is the ultimate goal as a PMU. One major aspect that was neglected so far is the operation of the converter in Discontinuous Conduction Mode (DCM). The selected cascode structure presented in Figure 3.4 (page 103) does not provide an off-state for all termination switches. The structure must be improved to provide this capability. DCM is also associated with a change in the control scheme under action of a supervisor.

Moreover the redesign of the DC-DC converter must encompass the capability of operation in quiescent mode (regulated output voltage at no load

current). The bias current budget must be controlled to the lowest possible value. The proper wake-up of the converter is also a required functionality.

Finally there is a trend in multi-phase DC-DC converters to address transient performances with an additional energy path [Švi13]. The additional energy path approach faces the challenge of additional passive components that limits the power density. The 3D assembly approach discussed in this work provides a nice framework to embed any additional passive component at a limited penalty in term of footprint.

SoC demonstration is the other application goal of the DC-DC converter discussed in this work. A test-chip should then include a digital payload along with its power supply strategy. The DC-DC converter is the actuator in this strategy. Obviously the challenge will be more on the interposer than in the silicon test-chip because of the I/Os of the digital functions.

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FOLIO ADMINISTRATIF

THÈSE SOUTENUE DEVANT L'INSTITUT NATIONAL DES SCIENCES APPLIQUÉES DE LYON

NOM : NEVEU
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DATE de SOUTENANCE : 11/12/15

Prénoms : FLORIAN

TITRE : DESIGN AND IMPLEMENTATION OF HIGH FREQUENCY 3D DC-DC CONVERTER

NATURE : Doctorat

Numéro d'ordre : 2015ISAL0133

Ecole doctorale : ED EEA

Spécialité : Génie Electrique

RESUME :

L'intégration ultime de convertisseurs à découpage repose sur deux axes de recherche. Le premier axe est de développer les convertisseurs à capacités commutées. Cette approche est compatible avec une intégration totale sur silicium, mais reste limitée en terme de densité de puissance si la charge requiert une importante puissance. Le second axe est l'utilisation de convertisseurs à inductances, qui pâtissent d'imposants composants passifs. Une augmentation de la fréquence de découpage permet de réduire les valeurs des composants passifs requis. Cependant une augmentation de la fréquence implique de fait une augmentation des pertes par commutation, ce qui est contrebalancé par l'utilisation d'une technologie de fabrication plus avancée. Ces technologies plus avancées souffrent quant à elles de limitations au niveau de leur tension d'utilisation.

Convertir une tension de 3,3V vers une tension comprise entre 0,6V et 1,2V apparait donc comme un objectif ambitieux pour un convertisseur inductif, particulièrement dans le cas où les objectifs de taille minimale et de rendement supérieur à +90 % sont vises. Un assemblage 3D des composants actifs et passifs permet de minimiser la surface effective du convertisseur. Un fonctionnement à haute fréquence est aussi considéré, ce qui permet de réduire autant que possible les valeurs requises pour les composants passifs.

Dans le contexte de l'alimentation « on-chip », la technologie silicium est contrainte par la charge, c'est-à-dire les fonctions numériques. Une technologie 40 nm CMOS de type « bulk » est choisie comme cas d'étude pour une tension d'entrée de 3,3 V. Les transistors 3,3 V présentent une figure de mérite Q_G x R_{DSON} médiocre, les transistors 1,2 V sont donc sélectionnés. Ce choix permet en outre de présenter une meilleure compatibilité avec une future intégration sur puce. Une structure cascode utilisant trois transistors en série est étudiée est confrontée à une structure standard à travers des simulations et mesures.

Une fréquence de travail de +100MHz est choisie. La technologie 40nm propose des capacités MOM et MOS qui affichent des densités trop faibles pour assurer un découplage suffisant. Une technologie de capacités en tranchées est sélectionnée, et fabriquée sur une puce séparée qui servira d'interposeur et recevra la puce active ainsi de les inductances. Les inductances doivent être elles aussi fabriquées de manière intégrée afin de limiter leur impact sur la surface du convertisseur.

Ce travail fournit un objet contenant un convertisseur de type Buck à une phase, avec la puce active retournée (technique « flip-chip ») sur l'interposeur capacitif, sur lequel une petite inductance est rapportée. Le démonstrateur une phase est compatible pour une démonstration à phases couplées. Les configurations standard et cascode sont comparées expérimentalement aux fréquences de 100 MHz et 200 MHz.

La conception de la puce active est l'élément central de ce travail, l'interposeur capacitif étant fabriqué par IPDiA et les inductances par Tyndall National Institute. L'assemblage des différents sous-éléments est réalisé via des procédés industriels. Un important ensemble de mesures ont été réalisées, montrant les performances du convertisseur DC-DC délivré, ainsi que ses limitations. Un rendement pic de 91,5 % à la fréquence de 100 MHz a été démontré.

MOTS-CLÉS : Convertisseur DC-DC, haute-fréquence, circuit intégré, 3D, CMOS

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