A 6 GHz Digital Receiver Using COTS Prototyping Boards

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***Abstract*—We have designed and tested a digital receiver suitable for the reception of 6 GHz instantaneous baseband signals. It is based on a Tektronix TADC-1000 12.5-GS/s 8-bit digitiser module, a Tektronix TIPA-3100 HAPS Interposer board and a Synopsys HAPS62-Virtex6 Prototyping Motherboard. This motherboard is also employed for filtering and signal processing. The ADC module uses an external clock from the interposer board and can accept a range of input clock frequencies between 1.6 and 3.125 GHz, resulting in sample rates of between 8 and 12.5 GS/s in single-channel mode. The external clock and digital data are supplied to and processed via the HAPS62 board. A 2048-channel weighted overlap-add (WOLA) and FFT structure separate the input signal into approximately 5-MHz sub-bands to allow subsequent high-resolution processing to obtain continuous spectral information over the input bandwidth.**

This system meets present-day demands on high-resolution wideband digital back-ends for RF spectrum monitoring. This technology could be part of the next generation wideband signal intercept systems for the future detection, classification and location of modern complex RF signals.

Keywords— digital receiver, high-resolution wideband back-ends, high-speed ADC, FPGA, FFT

I. INTRODUCTION

Current digital back-ends for RF signal intercept systems are able to analyse wideband signals, typically at 500 MHz input bandwidth and as wide as 2 GHz while offering a flexible range of spectral resolutions and high-resolution signal analysis. These back-ends are based on high-speed analogue-to-digital converters (ADCs) and high density field-programmable gate array (FPGA) devices. The sampling rate of the ADCs and the computing power of the FPGAs make it possible to directly digitise analogue signals of a few GHz of instantaneous bandwidth, and later to analyse them at high spectral resolutions of a few tens of kHz.

In this paper, we describe the implementation of a digital spectrometer and high-resolution signal processing system that performs digitisation and analysis of 6 GHz bandwidth signals. This development addresses the problem of intercepting complex RF signals that have frequency bandwidths much greater than 500 MHz.

In Section 2 we describe the digital receiver hardware design including the data transfer setup between the FPGA, interposer and ADC boards. We outline in Section 3 the signal processing architecture and in Section 4 present recent measurement results.

II. DIGITAL RECEIVER HARDWARE DESIGN

The digital receiver is based on a Tektronix TADC-1000 12.5-GS/s 8-bit digitiser module [1], a Tektronix TIPA-3100 HAPS Interposer [2] and a Synopsys HAPS62-Virtex6 Prototyping Motherboard [3]. The ADC module requires an external clock from the interposer board and can accept a range of input clock frequencies between 1.6 and 3.125 GHz, resulting in sample rates of between 8 and 12.5 GS/s in single-channel mode. The Interposer and FPGA prototyping boards provide power, cooling, JTAG interfacing, a Starfabric cabled PCI interface, a serial RS232 control port and a high-speed parallel digital interface.

The ADC is constructed of four time-sequenced ADCs each pair of which transmit their 3.125 gigabyte/s data to one of two 1:4 Demux modules that produce 128 digital lines for 390 Mbps double data rate (DDR). These data are then filtered into 2048 overlapping sub-bands, using an FFT spectrum analyser engine in order to reach high spectral resolution. Figure 1 presents the system block diagram of this ADC [1].

The Tektronix TIPA-3100 HAPS Interposer board interfaces to the FPGA on the Synopsys HAPS62 board. The 128-bit data interface passes data unchanged through the interposer for maximum data integrity. A DDR reference clock from the digitiser is buffered and provides 10 clocks to the HAPS62 FPGA for input of high speed data into various clock domains. A 128-bit wide LVDS data bus, 10 LVDS clocks and a Serial Peripheral Interface (SPI) are also provided. An FPGA controller on the interposer provides a PCI interface from a host computer to the digitiser module and also an SPI interface to the hardware on the interposer board (clock and reference signal generation) for control of their operation. An additional 20 unused interconnect lines are provided from the HAPS FPGA to an FPGA controller on the Interposer for future use [2].

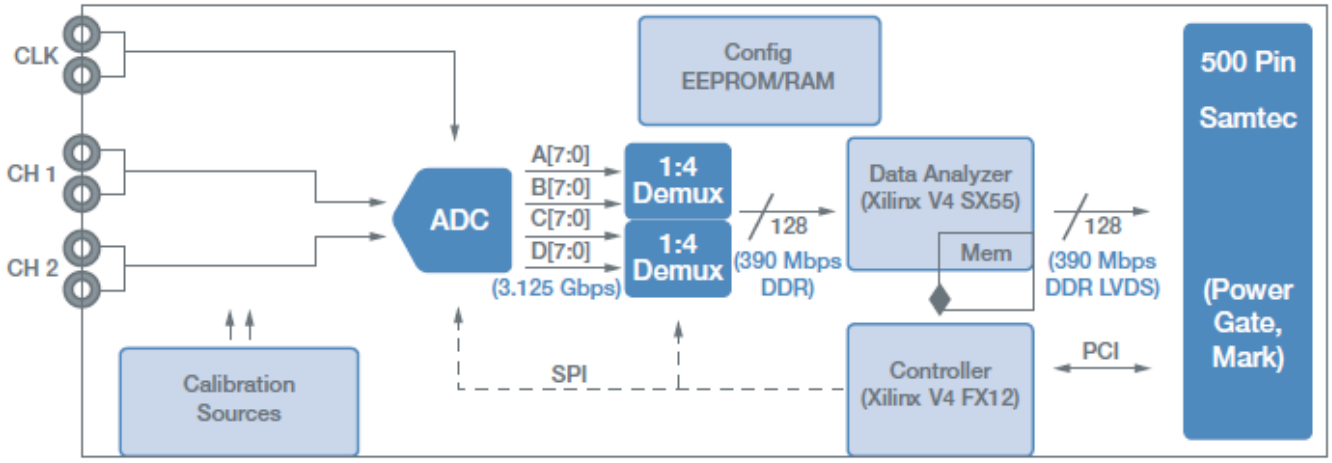

Figure 1. System block diagram [1].

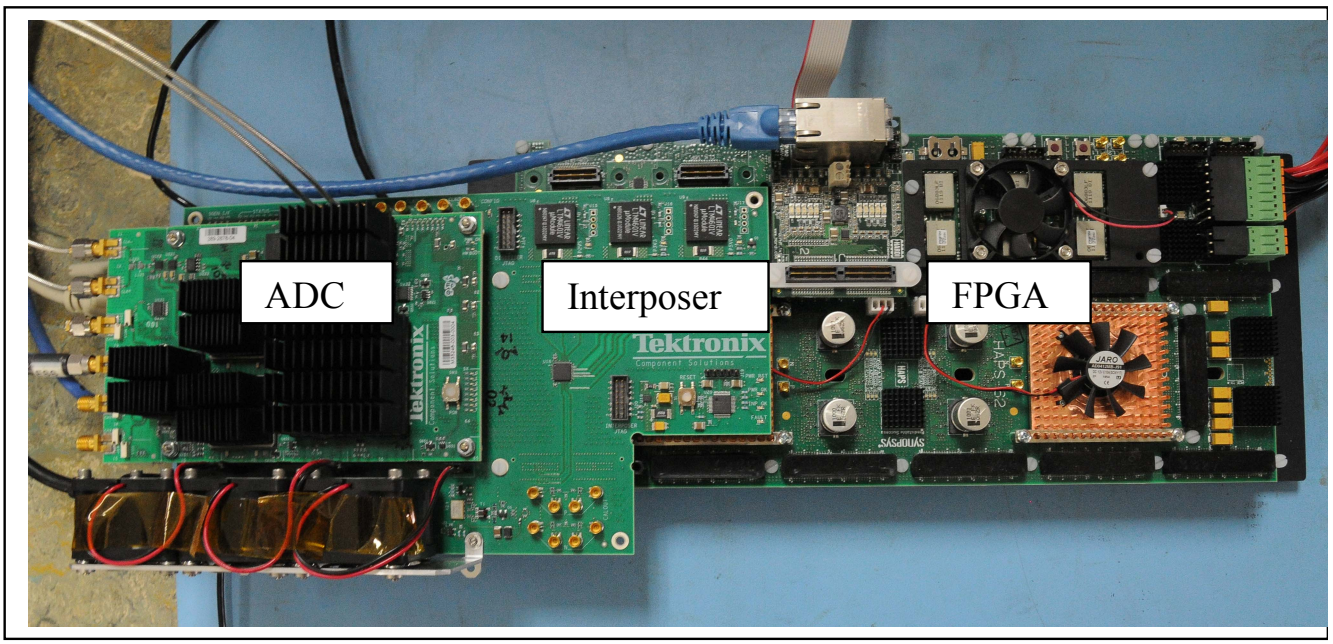

Figure 2. Picture of the digital receiver prototyping boards configuration.

The Synopsys HAPS62-Virtex6 Prototyping Motherboard is an FPGA-based prototyping system that allows ADC, FPGA and software integration and system-level validation at real-time run-rates using industry standard interfaces. The HAPS62 FPGA board contains two Xilinx Virtex-6 LX760 FPGAs, supports high performance digital signal processing and has high speed connectors with configurable I/O applications such as giga-bit Ethernet or PCI-express with power and cooling management.

Figure 2 shows a picture of the digital receiver boards. The ADC board can be seen sitting on the interposer board that connects to the FPGA board.

III. Digital Signal Processing

A WOLA-FFT or windowed pre-sum-FFT structure has been used to process digitised (real) RF signals in a DC to 6 GHz bandwidth into 2048 complex sub-bands. These output sub-bands are complex-valued baseband signals and have a bandwidth of approximately 5 MHz each. A WOLA-FFT structure was chosen instead of a straightforward application of the FFT on an input signal as the straight DFT approach suffers from two significant drawbacks, namely, leakage and scalloping loss. In the case of leakage, a strong RF interfering signal that is situated close to signals of interest in the nearby bins can suppress weak signals of interest. DFT scalloping loss is the loss in energy between frequency bin centres due to the non-flat nature of the single-bin frequency response.

A WOLA is a very efficient implementation of a uniform multi-rate filter bank using a DFT as described in [5], [6] and [7]. A classical uniform multi-rate filter bank is an array of digital baseband down converters with equally-spaced centre

frequencies and identical bandwidth. Each down converter performs a frequency down conversion, shifting a centre frequency of interest to baseband; low-pass filtering selects the bandwidth of the sub-band and down-sampling reduces the sampling frequency and maintains the Nyquist rate. The sampling frequency is reduced by a factor equal to the number of channels of the multi-rate filter bank.

Figure 3 shows an example of a standard 2048-channel filter bank. In our application the digitised input signal is placed into an array of digital filters, which are decimated-by-2048 versions of the original low-pass filter used in the equivalent classical uniform multi-rate filter bank. This means that the original FIR low-pass filter of N coefficients is partitioned into 2048 all-pass FIR poly-phase filters of N/2048 coefficients. Finally, the filtered signals are processed via a parallel FFT engine to obtain the output sub-bands.

This architecture offers increased efficiency in both speed and area, which are key aspects for programmable systems based on FPGAs. Note that there is a logic gate saving due to both the partition in the filtering stage and the computational efficiency of the FFT algorithm. In addition, all the data processing are performed at the reduced sampling rate. Because of all these benefits, digital filter banks are well suited for being the first processing stage of a digital receiver.

As the input digitised signal is real-valued, symmetry properties can be applied in order to use a single parallel FFT. This single FFT works on real or complex-valued input samples that are obtained via arithmetic operations over the real-valued samples coming from the filtering stage. For our design, the complex FFT is implemented using a radix-4 fully-parallel architecture. The FFT engine processes 2048 5-MHz complex-valued signals corresponding to an output sub-band of the WOLA.

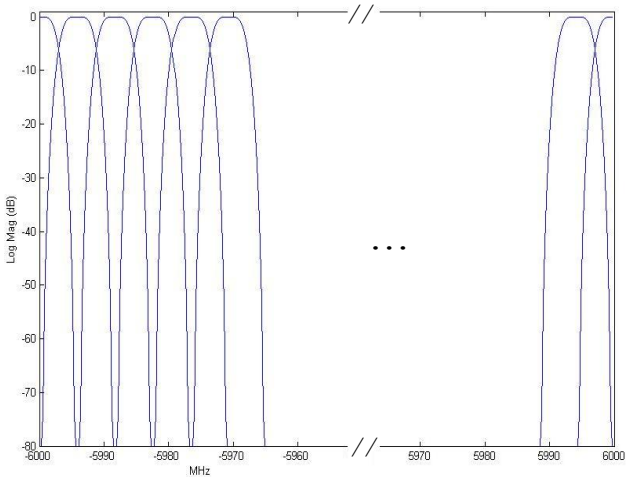

Figure 3. The 2048-channel WOLA plotted in MATLAB showing the channelised filter bank implemented to obtain continuous spectral information.

IV. RESULTS

The digital receiver was tested in the laboratory in order to evaluate its performance for spectrum monitoring and possible further digital processing. The results shown are from signals received from an omni-directional antenna with a pre-amplifier and band-pass filter. The spectrum and time-history waterfall display in Figure 5 has a frequency range of 0 to 6 GHz with its input derived from a 2-18 GHz band-pass filter. Figure 6 shows a screen capture of the spectrum displayed for the same 0 to 6 GHz frequency range but with the 2-18 GHz filter removed and shows the presence of signals in the 0 to 2 GHz band. The measured spectrum is displayed as a function of frequency and time which is updated continuously. Each figure displays approximately 17 seconds of measurements. The integration time is 12 μs with a frequency resolution of approximately 5 MHz which corresponds to 2048 FFTs accumulated for each sub-band. To cover the whole RF range from 2 to 18 GHz you could scan in three steps of 6 GHz or use 3 digitiser cards to cover the entire 2-18 GHz band.

This rapid prototyping implementation of the spectrometer uses an existing FFT core designed for a different ADC that requires data in blocks of 8 samples per clock. The Tektronix TADC-1000 provides data to the FPGA in blocks of 64 samples per clock so the FFT operates on 1/8th of the data. The current XC6VLX760 FPGA does not have a sufficient number of multipliers to implement 8 FFT cores each with 8 samples per clock.

A data buffering work-around allows us to still operate over the full 6 GHz bandwidth, but with some dead time. The project is scalable and work is underway to migrate to an FPGA with a greater number of multiplier resources. The spectrometer used 128 out of 864 DSP48E1 slices of the FPGA multiplier resources. A 100% duty cycle version of this spectrometer requires approximately 1024 DSP48E1 slices, easily supported by currently available devices.

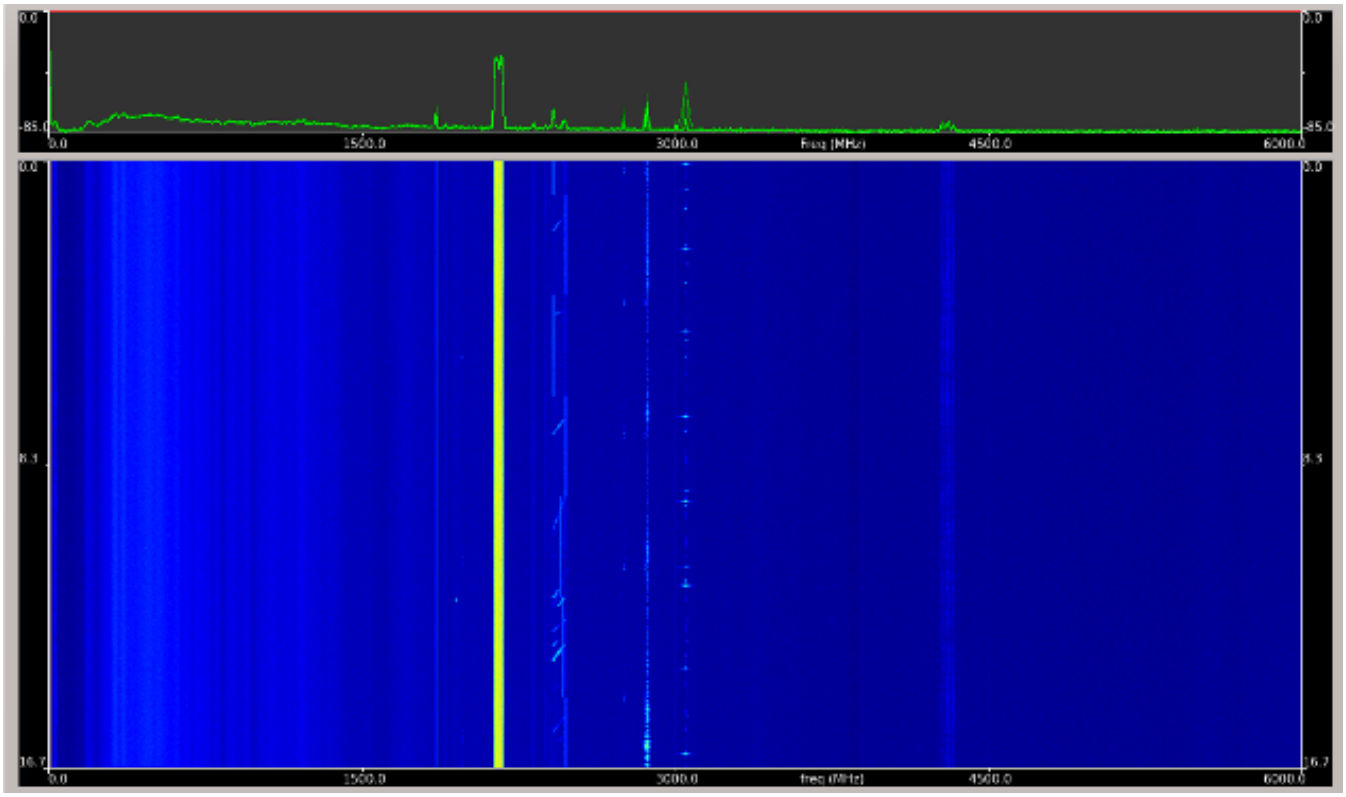

Figure 4. Measured spectra for the instantaneous frequency range of 0 to 6 GHz of a typical RF environment using a 2 - 18 GHz band-pass filter.

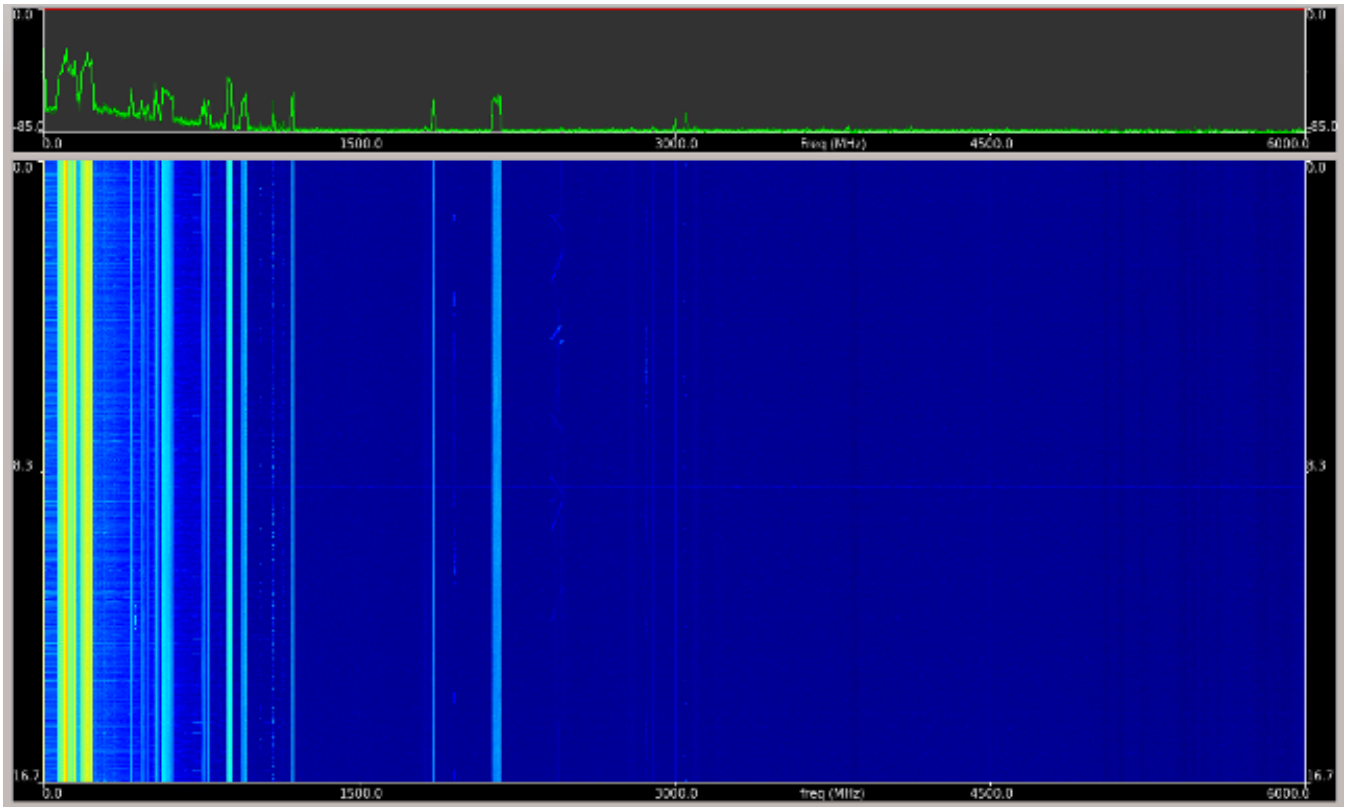

Figure 5. Measured spectra for the instantaneous frequency range of 0 to 6 GHz of a typical RF environment with the 2 - 18 GHz band-pass filter removed.

V. CONCLUSIONS

We have outlined the design and presented some results of a digital receiver that addresses the present-day demands for the detection and analysis of complex broadband RF signals that can occupy large instantaneous bandwidths. This receiver can digitise signals of an instantaneous bandwidth of up to 12 times wider than the current generation of digital receivers and RF intercept systems. It provides a uniform and continuous spectral response across the band and can also achieve high spectral resolutions. With a sampling speed of 12.5 GS/s, the design is a significant step forward in the development of digital receivers for RF signal intercept systems and RF spectrum monitoring.

This prototype digital receiver and high-resolution signal processing system can digitise and analyse, in real-time, up to 6 GHz bandwidth signals. The system appears to be capable of addressing the problem of receiving complex ultra-wideband RF signals that typically operate over frequency bandwidths much greater than 500 MHz. This digital receiver design could form the core of systems to monitor the activity of complex RF signals that occupy large frequency bandwidths as well as long range tactical data links that can use spread spectrum waveforms.

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