# An Accurate, Semiautomatic Technique of Measuring High Resistances

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*Abstract*—**An accurate, semiautomatic method of calibrating high-resistance standards is described. Measurements of resistances between $10^9$ and $10^{14}$ Ω at a minimum of 1 V or $10^{-12}$ A can be made with an accuracy better than 0.1 percent, each determination requiring typically from 0.5 to 50 s. The value of resistance is determined in terms of a fixed three-terminal capacitance, a resistance ratio, and a standard frequency, all being stable and accurately determinable quantities. The sources of errors and their minimization are discussed; the construction and operation of such a device are described.**

## Introduction

THE WHEATSTONE bridge has long been an accepted means of measuring and comparing two-terminal resistances. More recently, its emergence as an accurate instrument for high-resistance measurements up to the teraohm ($10^{12}$ Ω) range and beyond has been substantiated by improvements in the bridge design, and the advent of sensitive dc null detectors of high input impedance. Design improvements include any built-in flexibility with which various bridge configurations can be selected for optimum performance and for the accurate calibration of the ratio arms of the bridge, as well as the incorporation of shielding, guarding, laddering, and delta-wye transformation techniques[1]–[5]. As the resistance to be measured rises above $10^{10}$ Ω, however, the accuracy of the bridge suffers considerably from the accumulated errors in the scaling process, where intermediate high-resistance standards of limited stability, and significant temperature and voltage coefficients are involved, and from the diminution of effective sensitivity in the presence of increasing system noise and stray-capacitance effects in the bridge circuit. Commercial bridge units can typically achieve an accuracy of 0.25 percent at $10^{12}$ Ω.

Another method of calibrating resistances above $10^9$ and $10^{10}$ Ω involves charging or discharging resistor-capacitor networks. This constitutes a potentially powerful method, for high-resistance values can be established through other stable and accurately determinable quantities, and within certain practical limits, measuring time can sometimes be traded for increased precision. A particularly successful technique has been disclosed by Scott,[5] which has provided the most accurate means of calibrating multiteraohm resistors, with a typical accuracy figure of 0.1 percent.

At no sacrifice of overall accuracy, this established approach has been carried further by the technique to be presented here, so that semiautomatic operation and direct reading become possible, and with the value of the high resistance established through the values of a low-voltage *fixed* capacitor, a resistance ratio, and a standard frequency. A precision, prototype device based upon the active, analog integrator technique has been constructed to enable one to measure resistance standards between $10^9$ and $10^{14}$ Ω accurately and quickly (better than $\pm 0.1$ percent in typically 0.5 to 50 s), subject to a minimum test voltage of 1 $V$, and a minimum test current of 1 pA ($10^{-12}$A). Preliminary results obtained with the prototype unit and an estimation of the errors involved will also be given.

## The Integrator

The basic block diagram of the high-resistance measuring device is shown in Fig. 1, where $R_x$ denotes the high resistance under test. The operation of the device is based upon the analog integrator technique which utilizes in this case a high-gain operational amplifier with high input impedance $Z_{in}$, the input resistor $R_x$, and the feedback capacitor $C$. The performance of the integrator, noise and drift excluded, can be fairly accurately described, after the offset voltage of the amplifier has been set to zero (a practical proposition), by

$$\frac{V_i(s) - V_o(s)/A(s)}{Z_x(s)} = \frac{V_o(s)/A(s) - V_o(s)}{Z_f(s)} + \frac{V_o(s)}{AZ_{in}(s)} + I_{os}(s), \quad (1)$$

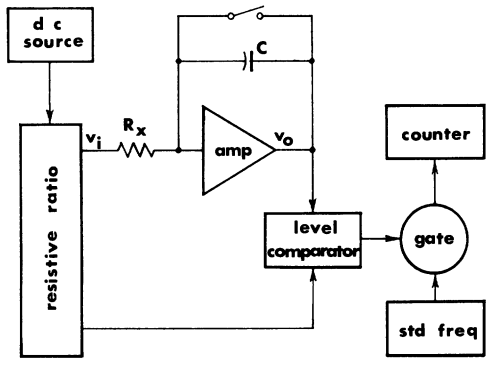


Fig. 1. Basic block diagram of high-resistance measuring device.

Manuscript received April 10, 1967. This paper was presented at the 1967 IEEE International Conference.

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where

$V_i(s)$ = transform of input voltage $v_i(t)$, assumed constant
$V_o(s)$ = transform of output voltage $v_0(t)$
$A(s)$ = open-loop voltage transfer function
$Z_x(s)$ = input network impedance (as shown, $Z_x = R_x$)
$Z_f(s)$ = feedback network impedance (as shown, $Z_f = 1/sC$)
$Z_{in}(s)$ = input impedance of amplifier, $Z_{in} > 10^{14}$ Ω in parallel with less than 30 pF
$I_{os}(s)$ = transform of offset current $i_{os}(t)$, assumed constant, flowing into the amplifier.

It is assumed that the integrator has reached its initial steady state of $v_o = 0$ with a constant voltage $v_i$ applied to $R_x$, before the initiation of the integration process at time $t = 0$ by the opening of the normally closed switch across $C$. Under these conditions, $Z_x(s)$ in (1) can be replaced simply by $R_x$, while the shunt capacitance across this resistor can be absorbed into the input capacitance $C_{in}$ of the amplifier. Furthermore, when a high-quality air-dielectric capacitor $C$, having a simple leakage resistance $r$, is used as the feedback element, (1) becomes

$$\frac{V_i(s)}{R_x} + V_o(s)\left[sC + \frac{1}{r}\right] = I_{os}(s) + \frac{V_o(s)}{A(s)}\left[s(C + C_{in}) + \frac{1}{R_x}\right]. \quad (2)$$

On the other hand, a perfect integrator would satisfy the following

$$\frac{V_i(s)}{R_x} + sCV_o = 0. \quad (3)$$

The discrepancy between (2) and (3) represents the error of the practical integrator. Under the assumed operating conditions that $|A(0)| \gg 1$ $(A(0) \approx -4000)$, $v_i \geq 1$ $V \geq v_o$, $C \geq 50$ pF $\geq C_{in}$, and that the test current through $R_x$, $i_R \geq 10^{-12}$ A, the error contribution of the last term on the right-hand side of (2) will be separately assessed as errors due to the finite gain, bandwidth, and input impedance of the integrating amplifier.

Ignoring this term for the moment, then

$$\frac{V_i(s)}{R_x} + V_o(s)\left[sC + \frac{1}{r}\right] = I_{os}(s). \quad (4)$$

Since it can be assumed that both $v_i(t)$ and $i_{os}(t)$ remain constant for the duration of the integration period $\Delta t$ of typically 0.5 to 50 s, and that $v_o(t)$ closely approximates a ramp, the increment in $v_o(t)$ during $\Delta t$ can now be expressed as

$$\Delta v_o = \frac{-v_i \Delta t}{CR_x}\left[1 - \frac{i_{os}R_x}{v_i} - \frac{\Delta t}{2Cr}\right]. \quad (5)$$

Hence, the unknown resistance is closely given by

$$R_x = \frac{\Delta t}{C}\,\frac{v_i}{-\Delta v_o}\,[1 + \eta], \quad (6)$$

where the correction term $\eta$ is taken as

$$\eta = -\left[\frac{i_{os}R_{x,\text{nominal}}}{v_i} + \frac{\Delta t}{2Cr}\right]. \quad (7)$$

It is observed that only $\Delta t$, $C$, and the ratio of voltages $(v_i/\Delta v_o)$ need be determined accurately.

## The Measuring Device

A complete high-resistance measuring device, as outlined in a more detailed form in Fig. 2, has been constructed and tested. (Two recent publications[7],[8] presenting a related method of measuring high resistances have since come to the author's attention but no information about performance is available.)

In order to achieve an overall accuracy of better than 0.1 percent, as well as for noise and stability considerations, the amplifier in Fig. 1 has been realized as a unity-gain electrometer amplifier $A_1$ of input impedance $Z_i > 10^{14}$ Ω in parallel with less than 30 pF, followed in cascade by a heavily damped feedback operational amplifier $A_2$ with an effective zero-frequency voltage gain of approximately −4000. The integrator, now consisting of amplifiers $A_1$ and $A_2$, the test resistor $R_x$, and the feedback capacitor $C$, functions as already described. In addition, the relay-operated normally closed switch $S_2$ resets the integrator output $v_o$ to zero after each determination of $R_x$.

The input circuit of the electrometer amplifier, as well as capacitor $C$ and switch $S_2$, are carefully insulated and shielded; input connections are kept short and rigid to minimize shunt capacitance to ground, and to eliminate any change in this capacitance during a measurement. Since any unwanted dc leakage into this input terminal introduces an error, it is highly desirable, if not essential, to guard the circuit at points where leakage is likely to occur across insulation (e.g., across $C$ and $S_2$). The

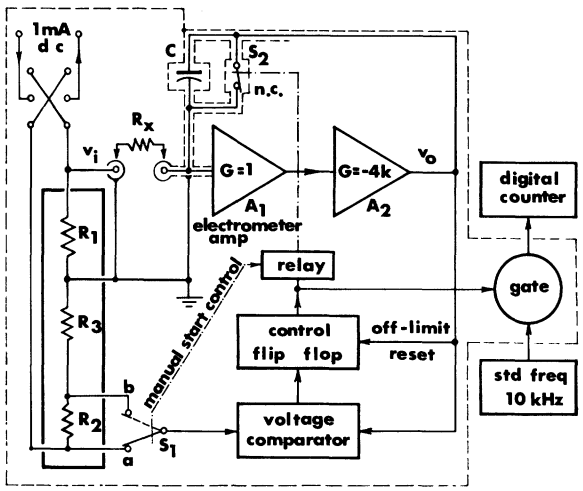


Fig. 2. Detailed block diagram of high-resistance measuring device.

input of an inverting operational amplifier being a "virtual ground," the guard circuit is conveniently at ground potential, a fact which simplifies the problem of practical implementation.

Since the voltage across $C$ need not exceed about 1 $V$ at any time, a high-voltage capacitor is not required. However, $C$ must have very low leakage and dielectric absorption. In these respects, small air-dielectric trimmer capacitors ($C \geq 50$ pF) on clean ceramic (steatite) bases offer a satisfactory solution, leakage resistance above $3 \times 10^{15}$ Ω being possible. For the most accurate work, however, modified units with guarded terminals are recommended. In order to establish accurately the capacitance value $C$ to within $\pm 0.01$ percent, it is measured as a three-terminal capacitor *in situ*, with $S_2$ open (but without the amplifiers turned on). This measurement is carried out at a number of frequencies down to at least 50 Hz to verify that the capacitance in question remains substantially unchanged with frequency.

The integration process is initiated manually through the action of a DPDT microswitch. This places $S_1$ (Fig. 2) in position $b$, and it also closes a circuit to energize the relay which opens $S_2$. As the output $v_o$ reaches the voltage $v_b$ at $b$, the voltage comparator sets the control flip flop (bistable multivibrator) which then keeps the relay energized through a parallel circuit. The starter switch is returned (manually or otherwise) to the original position, placing $S_1$ in position $a$, before $v_o$ crosses the voltage $v_a$ appearing at $a$, at which instant the same comparator resets the flip flop, de-energizing the relay to close $S_2$. The use of a single comparator has helped eliminate detection threshold problems. An electronic gate[9] controlled by the flip flop permits a precise determination of the elapsed time $\Delta t$, that $v_o$ takes to traverse from $v_b$ to $v_a$, in terms of standard frequency counts $N$, as registered by the digital counter. Fig. 3 (a) illustrates the sequence of operation of switch $S_1$, and Fig. 3 (c) the gating action of the flip flop in relation to Fig. 3 (b) the output $v_o$. It is clear that the gated period for the counter is essentially independent of the operate- and release-time delays, $d_1$ and $d_2$, of the relay, because the relay performs no timing functions.

Although in principle all the principal quantities in (6), viz., $\Delta t$, $C$, $v_i$, and $\Delta v_o = (v_a - v_b)$, can be measured and $R_x$ determined, it is definitely advantageous in practice to be able to obviate the need for measuring voltages absolutely. The quantity $(v_i/-\Delta v_o)$ in (6) can be replaced by the resistance ratio $(R_1/R_2)$, irrespective of the polarity of $v_i$, providing that 1) $R_x \gg R_1$, and 2) the input resistance of the comparator $R_i \gg R_2$, as the errors so introduced will be small (typically 0.005 percent). In practice, $R_1$ with a maximum of 110 $k\Omega$ is made up of two decades of 0.01-percent wire-wound resistors, and $R_2$ is a 1-$k\Omega$ resistor of similar quality and construction to obtain good tracking with $R_1$ over a small temperature range. By passing a constant 1 mA dc through these

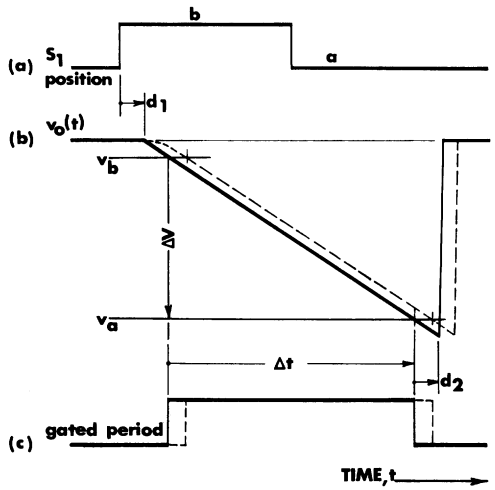


Fig. 3. (a) Position of switch $S_1$, (b) integrator output, $v_o$, and (c) gated period for counter.

resistors, and by varying $R_1$, $v_i$ can cover a working range of 1 to 110 $V$. The incremental output voltage $\Delta v_o$ is, therefore, very close to 1 $V$ in magnitude.

Due to the finite bandwidth of the integrating amplifier $A_2$, which has been purposely restricted to insure stability and reject noise, the output voltage, shown greatly exaggerated as the dotted curve in Fig. 3(b), will deviate from the ideal ramp. However, if enough time is allowed to elapse before incremental measurements of $v_o$ are made, errors due to transient at the onset and bandwidth limitations can be removed. This is achieved in practice by the introduction of another resistor $R_3 (\approx R_2/5)$, raising the magnitude of $v_b$ above zero.

The correction terms in (7) can now be examined. It is observed that considerable error will result if the effects of the small but finite offset current of the amplifier ($i_{os} \approx 10^{-14}$ $A$ or less) are not properly accounted for, as evidenced by the significance of the first correction term in (7) when the test current $i_R = v_i/R_x$ is low. Attempts to compensate physically for this offset current at the input of the amplifier will likely create more problems than they will solve; this approach has not been followed here. Instead, the feature of input polarity reversal, which is consistent with reversed dc measurement practice, is included in the design. The effects of $i_{os}$ can be averaged out by a polarity reversal of $v_i$, provided that $i_{os}$ remains constant in the short period of time required by this series of reversed dc measurements. The second term in (7) suggests the avoidance of unnecessarily long measurement time. However, a compromise must be made when timing accuracy and noise rejection requirements are taken into consideration. A practical measurement time from 0.5 to 50 s seems to be in order. Thus subject to a number of bounded errors, the device can be made direct reading, if necessary, with the value of the unknown resistance given by

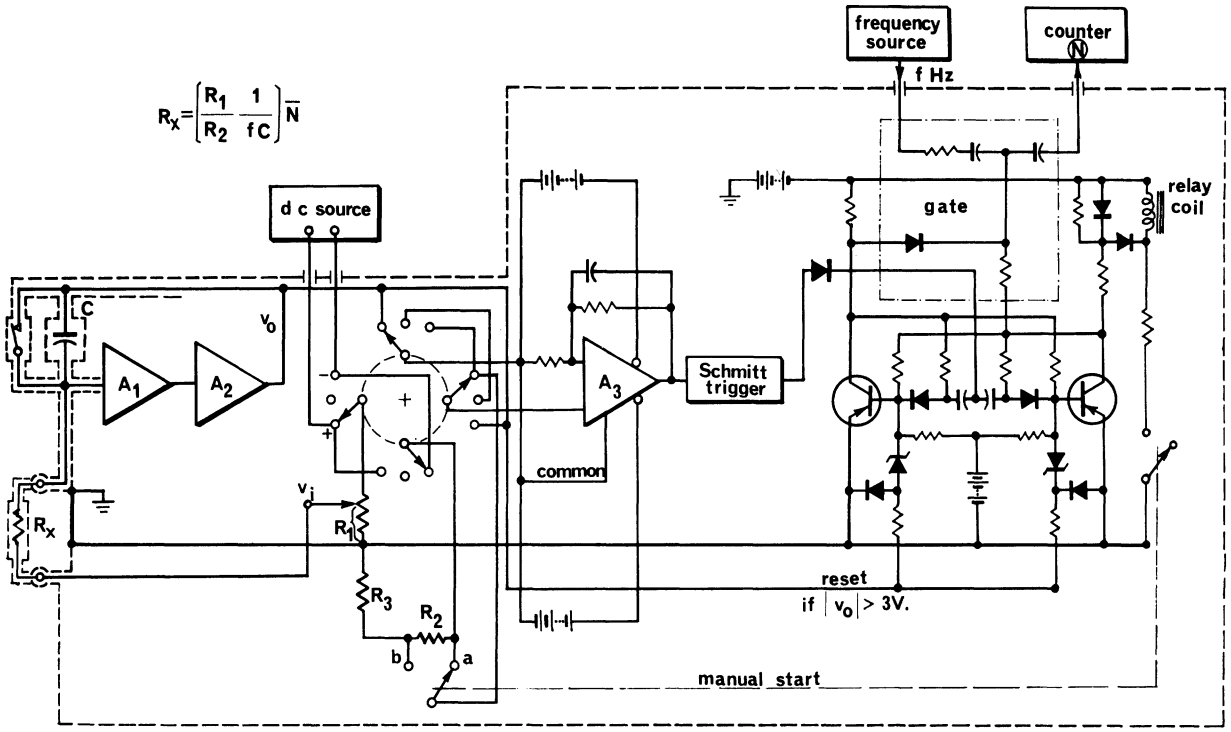


Fig. 4. Partial circuit diagram of high-resistance measuring device.

$$R_x = \left(\frac{R_1}{R_2}\cdot\frac{1}{fC}\right)\bar{N}, \tag{8}$$

where $\bar{N}$ = average of a number of registered counts in the digital counter, for reversed dc, and $f$ = signal frequency in Hz. For direct reading, the quantity $(R_1/R_2)$ $(1/fC)$ is adjusted to give powers of 10. Equation (8) clearly shows that the high-valued resistance can be established in terms of a fixed capacitance, a known frequency, and a ratio of two resistances of much lower values. These stable quantities can be measured by conventional techniques with an accuracy considerably higher than the final accuracy figure of the device.

Fig. 4 is a partial circuit diagram of the device. Attention is drawn to the input circuit of the comparator and the simple but effective circuitry which allows the control flip flop to perform its tasks. The comparator input amplifier $A_3$ connected as a noninverting high input-resistance amplifier of a moderate voltage gain of about 10, together with the Schmitt trigger, is powered from isolated power supplies which float at the potential of one of the inputs of $A_3$. Coupled reversals of input connections with reversed dc measurements keep the comparator working in identical conditions. These precautions greatly help eliminate common-mode, and sequential errors in the comparator circuit. The control flip flop fulfils the functions of 1) gating the frequency signal, 2) controlling the initiation and termination of the integration through the relay, and 3) resetting the integrator to zero either at the end of each determination of $R_x$, or whenever $|v_o| > 3V$.

## Performance and Errors of the Device

The operational aspects of the prototype device have been under continued development for some time. A new unit with improved guarding, component and supply stability, and added flexibility is under construction. The preliminary results or error estimates reported here are, however, essentially those obtained for the prototype unit.

Adequate stabilization of the particular electrometer amplifier used required over 48 hours of continuous operation, with an offset current of the order of $10^{-14}$ A. (Other electrometer amplifiers may give better performance in these respects.) Repeatability of digital-counter readings after stabilization was up to $\pm 0.02$ percent of reading over about 10 minutes. The value of $\bar{N}$ was generally obtained as a mean of four to ten reversed dc readings.

The accuracy of the device in measuring resistance standards from $10^9\Omega$ up to $10^{12}\Omega$ at 100 V has been verified by direct comparison of results (uncorrected for capacitor leakage, finite gain, and input impedance of the amplifier) with Wheatstone bridge determinations. Observed discrepancies ranged from $+0.02$ percent to $+0.06$ percent, the bridge determination consistently yielding the lower values. All experiments were carried out under standards laboratory conditions of $21 \pm 1$°C and $45 \pm 5$-percent relative humidity. Each of the resistors under test was placed inside an air-bath enclosure to ensure proper guarding, shielding, and temperature stability between determinations by the two methods.

TABLE I
ESTIMATED ERRORS OF HR MEASURING DEVICE

| Source | Expression | Typical Estimates in % | |
|---|---|---|---|
| | | 1) $\Delta t = 1$ s, $i_R = 10^{-10} A$ | 2) $\Delta t = 50$ s, $i_R = 10^{-12} A$ |
| Finite gain $\lvert A \rvert \approx 4000$ | $\frac{1}{\lvert A \rvert}\left(1 + \frac{\Delta t}{2CR_x}\right)$ | $+0.02 \pm 0.01$ | $+0.03 \pm 0.015$ |
| Finite input impedance $Z_{in} > 10^{14}\Omega // 50$ pF | $\frac{C_{in}}{\lvert A \rvert C}$ | $+0.01 \pm 0.01$ | $+0.02 \pm 0.01$ |
| Finite bandwidth | | negligible | negligible |
| Leakage resistance | | | |
| $r \approx 3 \times 10^{15}\Omega$ | $\frac{\Delta t}{2Cr}$ | negligible | |
| $r \approx 5 \times 10^{16}\Omega$ (guarded) | | — | $+0.001$ |
| Short-term Electrometer drift | $\frac{\Delta i_{os}}{i_R}$ | $\pm 0.01$ | $\pm 0.02$ |
| Ratio $(R_1/R_2)$ | | $\pm 0.01$ | $\pm 0.01$ |
| Capacitance $C$ | | $\pm 0.01$ | $\pm 0.01$ |
| Comparator and counter | | $\pm 0.01$ | $\pm 0.005$ |
| System noise | Noise $bw = \frac{1}{2\Delta t}$ | $\pm 0.001$ | $\pm 0.002$ |
| Algebraic sum | | $+0.03 \pm 0.06$ | $+0.05 \pm 0.07$ |

The high-resistance bridge employed was a specially designed one, featuring complete shielding, guarding, and demountable ratio arms with mercury contacts, in order to attain maximum accuracy through a series of calibration steps when using appropriate bridge connections. Accuracy of the bridge for $10^{12}$ Ω measurements at 100 V, referred to the 1 Ω standard, is estimated to be $\pm 0.05$ percent under optimum conditions. At reduced bridge voltages, however, its performance is curtailed by the limitation in system sensitivity.

Equation (2) forms the basis for assessing errors in the observed value of $R_x$, which arise from the finite gain, bandwidth and input impedance of the amplifier, the leakage resistance of the capacitor $C$, and the offset current $i_{os}$. As each of the errors is small, they may be considered singly. In addition, errors in $R_x$ arising from inaccuracies in the knowledge of $(R_1/R_2)$ and $C$, from the drift of the input voltages, etc., must also be assessed. These errors are summarized in Table I, for the two representative cases: 1) $\Delta t = 1$ s, $i_R = 10^{-10}$ $A$, and 2) $\Delta t = 50$ s, $i_R = 10^{-12}$ $A$. They are applicable, for instance, to the two cases of determining $10^{12}$ Ω at 100 $V$ and at 1 $V$, using a capacitance $C$ of 100 pF and 50 pF, respectively.

It should be pointed out that part of the errors due to the finite gain and input impedance of the amplifier can be estimated fairly accurately and corrections can be applied; the corrections for cases I and II will be $-0.03$ percent and $-0.05$ percent, respectively. These positive errors were also borne out by the observed discrepancies of results obtained by the two methods of determination cited above.

## CONCLUSIONS

A high-resistance measuring device, capable of rapid, semiautomatic operation with better than $\pm 0.1$ percent accuracy, has been constructed, demonstrating a further refinement in the RC time-constant technique of calibrating high resistances. Present limitations include amplifier drift and off-set current of the particular amplifier used, which restrict the measuring current to a minimum of $10^{-12}$ A. On the other hand, its advantages include high stability, direct-reading capability, high degree of freedom from pick-up, thermal electromotive force and stray-capacitance effects, and a wide choice of test voltages. Its semiautomatic operation has removed the complaint, usually directed at other time-constant methods, of being cumbersome in operation. It will be a useful tool in studying the effects of time, voltage, temperature, etc., on high-valued resistors.

When augmented by the more conventional Wheatstone bridge, this device will provide a complete and accurate coverage for the measurement of resistances from $10^5$ to $10^{14}$ or $10^{15}$ Ω.

ACKNOWLEDGMENT

The author is grateful to Dr. A. F. Dunn for many free and fruitful discussions during the course of this work, and for his valuable comments while preparing this paper.

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# Analysis of Rotationally Misaligned Stators in the Rotary-Vane Attenuator

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***Abstract*—Two types of errors are caused by misaligned stators in the rotary-vane attenuator. For each type of error the actual attenuation will differ from the indicated attenuation values throughout most of the usable range of the attenuator.**

**This analysis illustrates that these two types of errors are related to the technique of alignment used in establishing the zero reference of the rotating vane to the stator vanes. Equations pertaining to these errors are discussed and are solved with the aid of tables of attenuation error as a function of vane angle error for rotary-vane attenuators. Graphs of both types of errors are presented determining the parameters needed to establish limits of machining tolerances for each waveguide size.**

## I. INTRODUCTION

THE ROTARY-VANE attenuator is a resistive type of microwave attenuator and is very useful for the measurement of attenuation difference. The rotary-vane attenuator is considered to be the most suitable instrument for wideband application because theoretically it is independent of frequency, and the phase shift variations in the attenuator are small with changes of attenuation setting. It has been shown that a serious source of error in this type of attenuator is caused by misalignment between the vanes in the stators.[1] [2]

This paper analyzes two types of errors caused by misalignment between the stator vanes and the rotating vane at the zero setting. One type of error considered here occurs when the plane of the rotating vane is initially coincident with the plane of the vane in one stator only, and the other type of error considered occurs when the plane of the rotating vane is initially coincident with the average position of both stator vanes. The analysis shows that for each type of error the actual attenuation will differ from the indicated attenuation throughout the range of the attenuator.[5] Equations pertaining to these errors are discussed, and their solution is found with the aid of tables.[4] Graphs of both types of errors are presented for estimating the errors in attenuation at different dial settings with known machining tolerances for each of the waveguide sizes.

Manuscript received March 17, 1967.
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## II. ATTENUATOR CONSTRUCTION AND OPERATION

The rotary-vane attenuator consists principally of three sections of circular waveguide: a rotating section; and two stators. A thin resistive card (vane) is placed diametrically across each section. The resistive cards of the stators lie in the same plane, and the card of the rotating section rotates with the center section. These three sections of circular waveguide are placed in tandem on the same longitudinal axis, as shown in the pictorial diagram of Fig. 1. In the usual construction of the attenuator, the rotating section of waveguide is rotated by a concentrically mounted gear. Errors caused by this type of gear drive have been studied.[5],[6]

The attenuation produced in a rotary-vane attenuator, ideally, is a function of the angle, $\theta$, which is the angle between the rotating vane relative to the fixed vanes. The theoretical attenuation value, $A$, is given in decibels as a function of the angle $\theta$ by the expression[7]

$$A = -40 \log_{10} \cos \theta. \quad (1)$$