A 10-A High-Precision DC Current Source With Stability Better Than 0.1 ppm/h

Nong Wang, Zhengkun Li, Zhonghua Zhang, Qing He, Bing Han, and Yunfeng Lu

***Abstract*— The principle, design, and measurement of a 10-A highly stable dc current source is described. Based on a modified low-frequency equivalent model of the MOSFET, we obtain the strict current equation of the MOSFET-based voltage-controlled current source. Factors determining the current stability are investigated and reasonable selection criteria for the key components are discussed. Reasons for oscillation due to the high parasitic capacitance of the paralleled MOSFETs with low set of drain–source voltage are explained and a combined noise gain and lead compensation method is proposed. The best measurement results show that the relative standard deviation and relative drift of the current in 1 h are, respectively, 7.5×10^{-8} and 2.2×10^{-8}. The current source has been used in our high-current meter stability evaluation experiments and can be used for other cases with appropriate improvement, such as the Joule Balance Project to redefine the kilogram at National Institute of Metrology.**

***Index Terms*— Current source, current supply, joule balance, standard current, transconductance amplifier, voltage-controlled current source (VCCS).**

I. Introduction

TO EVALUATE the stability of the ultraprecision high-current meter being developed by our team at National Institute of Metrology (NIM), a 10-A dc current source with stability better than 1×10^{-6}/h is required. However, there is no commercial current source that can satisfy this requirement. A possible solution has been introduced in [1], but it is too complicated to be achieved within a short time. A relatively simple solution has been proposed by us on the CPEM 2014 [2], and as in [3]–[5], the key circuit is a MOSFET-based transconductance amplifier, as shown in Fig. 1. It is essentially a voltage-controlled current source (VCCS) and its operating principle can be found in [2].

Compared with published approaches [3]–[5], the main improvement made by us in [2] is the current stability. To that end, we applied almost the best commercial voltage reference and sample resistor. However, as in [3]–[5], the selection criteria for the key components are qualitative and the only theoretical basis is the ideal current equation, which is obtained under a series of assumptions [2]. To further improve the current stability, it is necessary to obtain the strict current equation containing the parameters ignored in [2], thus establishing a theoretical basis for the reasonable selection criteria of the key components.

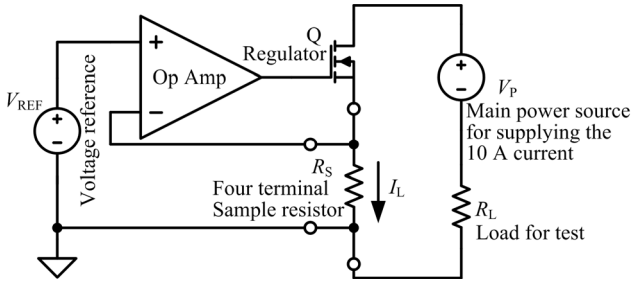

Fig. 1. Key circuit of the MOSFET-based 10-A VCCS used in [2] and in this paper.

Another improvement achieved in [2] is the extending of the output range and the reduction of power dissipation on the MOSFET. For that, five MOSFETs in parallel mode with low set of drain–source voltage were used. However, multi-MOSFETs in parallel mode with low drain–source voltage bring in high parasitic capacitance, thus leading to oscillation. To stabilize the loop, it is necessary to investigate the reasons for oscillation and seek for solutions.

In this paper, the strict current equation of the VCCS is derived on the basis of a modified low-frequency model of the MOSFET. Based on the strict equation, factors determining the current stability are analyzed and reasonable selection criteria for the key components are established. We have built the high-frequency equivalent circuit of the VCCS and found out that the oscillation is caused by the combination effect of the high parasitic capacitance of the multi-MOSFETs and the open-loop output impedance of the operational amplifier (op-amp). To eliminate the oscillation, a combined noise gain and lead compensation method is proposed. Finally, a 10-A dc current source with stability much better than 1×10^{-6} is realized and tested.

II. Principle

A. Strict Current Equation

To derive the strict current equation, we have established the low-frequency equivalent circuit of the VCCS. The dotted

Manuscript received August 25, 2014; revised October 24, 2014; accepted November 10, 2014. This work was supported in part by the National Natural Science Foundation of China under Grant 51077120 and in part by the National Key Scientific Instrument and Equipment Development Projects of China under Grant 2011YQ090004. The Associate Editor coordinating the review process was Dr. Lucas Di Lillo.

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Digital Object Identifier 10.1109/TIM.2014.2376114

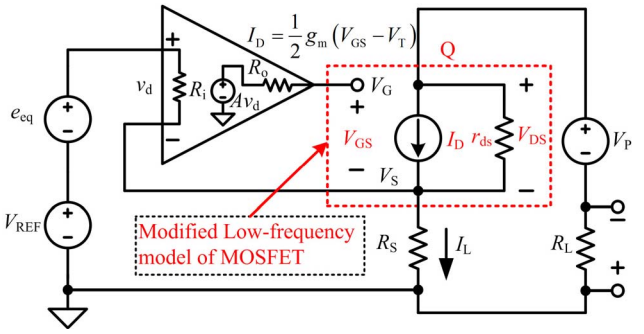

Fig. 2. Low-frequency equivalent circuit of the VCCS with one MOSFET to derive the strict current equation.

box in Fig. 2 shows the modified low-frequency model of the MOSFET.

For a MOSFET operating in the active region, the drain current equation can be written as

$$I_D = \frac{1}{2} g_m (V_{GS} - V_T) \tag{1}$$

where I_D is the drain current, g_m is the low-frequency transconductance, V_{GS} is the gate–source voltage, and V_T is the threshold voltage. Detailed derivation of this equation can be found in [6], where the relationship between this equation and the familiar square-law equation is described. Equation (1) implies that the drain current is independent of the drain–source voltage V_{DS}. However, this independence is true only when the channel-length modulation effect is ignored. For a real MOSFET device, this effect cannot be neglected because its output characteristic curve is not absolutely flat. In our modified model, this effect is approximately expressed by the output impedance r_{ds} of the MOSFET, as shown in Fig. 2.

In Fig. 2, by solving the circuit equations written on the basis of the Kirchhoff's law, we obtain the strict current equation as

$$I_L = \frac{\frac{1}{2} g_m A (V_{REF} + e_{eq}) - \frac{1}{2} g_m V_T + \frac{V_P}{r_{ds}}}{\frac{1}{2} g_m (A+1) R_S + \frac{(R_S + R_L)}{r_{ds}} + 1}, \tag{2}$$

where I_L is the stabilized load current, V_{REF} is the voltage reference, R_S is the sample resistor, A and e_{eq} are, respectively, the open-loop gain and the equivalent input noise voltage and drift of the op-amp, R_L is the load, and V_P is the main power supply. Note that the input and the output impedance (R_i and R_o in Fig. 2) of the op-amp are ignored, because R_o is usually much smaller than the input impedance of the MOSFET (infinite in this model), and for high current source R_S is usually much smaller than R_i.

To obtain the ideal current equation, some assumptions are made as follows. The A, r_{ds}, and g_m are large enough and e_{eq}, R_S, R_L, V_T, and V_P are small enough. Under these assumptions, the strict current equation can be simplified as

$$I_L = \frac{V_{REF}}{R_S} \tag{3}$$

which is the ideal current equation as described in [2]–[4].

By comparing (2) with (3), we can see that the strict current equation contains almost all the key parameters of the components used, while the ideal equation only contains two. Therefore, by analyzing (2), main factors determining the current stability can be found.

B. Factors Determining the Current Stability

By taking logarithm on both sides of (2), we obtain

$$\ln I_L = \ln\left[\frac{1}{2} g_m A (V_{REF} + e_{eq}) r_{ds} - \frac{1}{2} g_m V_T r_{ds} + V_P\right] - \ln\left[\frac{1}{2} g_m (A+1) R_S r_{ds} + r_{ds} + (R_S + R_L)\right]. \tag{4}$$

By taking total differential on both sides of (4) and based on the assumptions made when deriving the ideal current equation aforementioned, the following equation can be obtained as:

$$\frac{dI_L}{I_L} \approx \frac{dV_{REF}}{V_{REF}} + \frac{de_{eq}}{V_{REF}} - \frac{dR_S}{R_S} + \frac{1}{(1+A)} \frac{dA}{A}, \tag{5}$$

where it is assumed that $e_{eq} \ll V_{REF}$.

In (5), dI_L/I_L is the relative change of I_L, i.e., the current stability. Similarly, the items on the right side, including dV_{REF}/V_{REF}, de_{eq}/V_{REF}, dR_S/R_S and dA/A, are, respectively, the relative change of V_{REF}, e_{eq}, R_S, and A. Note that the signs in (5) only indicate the direction of change rather than magnitude. So, (5) implies that the stability of V_{REF}, R_S, and e_{eq} will directly determine the current stability, while that of A is attenuated $(1 + A)$ times. If A is large enough, effect from A can be ignored. Now, factors determining the current stability can be concluded as V_{REF}, R_S, and e_{eq}. Since no correlation exists between them, there should be the following relationship:

$$\frac{dI_L}{I_L} \le \sqrt{\left(\frac{dV_{REF}}{V_{REF}}\right)^2 + \left(\frac{de_{eq}}{V_{REF}}\right)^2 + \left(\frac{dR_S}{R_S}\right)^2}. \tag{6}$$

In our design, the requirement is $dI_L/I_L \le 1 \times 10^{-6}$. According to (6), there should be

$$\frac{dV_{REF}}{V_{REF}} = \frac{de_{eq}}{V_{REF}} = \frac{dR_S}{R_S} \le 5.8 \times 10^{-7}. \tag{7}$$

Equation (7) implies that the relative change of V_{REF}, R_S, and e_{eq} should be, respectively, smaller than 5.8×10^{-7}, which are the selection criteria for the three most crucial parameters.

III. Determining the Key Components

According to the analysis above, the key components in our design can be concluded as V_{REF}, R_S, op-amp, and MOSFET, and the selection criteria will be described in the following.

A. Voltage Reference and Sample Resistor

Equations (3) and (5) show that V_{REF} and R_S are two of the most important components. As shown in (3), I_L is theoretically determined only by the ratio of V_{REF} to R_S. However, value selection of the two key components is a tradeoff that requires comprehensive consideration. Higher V_{REF} will help to improve signal-to-noise ratio (SNR), but

more power will be consumed on R_S, thus deteriorates its stability. Besides, higher V_{REF} means higher common mode rejection ratio (CMRR) of the op-amp will be required.

In our design, the required stability of V_{REF} is better than 5.8×10^{-7}. As far as we know, voltage reference with stability better than 1 ppm can only be realized by very few ultraprecision zeners, such as LTZ1000 [1], [7]. Here, to test the performance of the VCCS, a commercial dc voltage standard named 732 B from Fluke is used. To reduce the power dissipation on R_S and to guarantee the SNR, the 1.018 V output is selected. Test results show that the stability of the 1.018 V output with a voltage buffer well designed is better than 0.1 ppm in 1 h, which is sufficient to our design.

Since the required current is 10 A, the value of R_S will be about 0.1 Ω, thus the power consumed on R_S will be about 10 W. Besides, the required stability of R_S is better than 5.8×10^{-7}. Resistors that can satisfy these requirements are difficult to achieve [1]. Here, a 0.1-Ω standard resistor with rated power 50 W from Tinsley Corporation is used. Test results show that its stability is better than 0.1 ppm after 2-h preheating and this performance is good enough for our design.

B. Error Amplifier

For the op-amp in our design, the most crucial parameters are dV_{OS}/dT (input offset voltage drift), e_n (low-frequency input noise voltage), A, CMRR, power supply rejection ratio (PSRR), gain bandwidth product (GBW), and R_o.

Since dV_{OS} and e_n are equivalent to superpose on the input of the op-amp and no correlation exists between them, there should be the following relationship:

$$de_{eq} \le \sqrt{e_n^2 + (dV_{OS})^2}. \tag{8}$$

According to (7), there is $de_{eq} \le 0.59\ \mu$V. So, there should be $e_n = dV_{OS} \le 0.42\ \mu$V, i.e., e_n should be $<0.42\ \mu V_{P\text{-}P}$, and dV_{OS}/dT should be better than 0.42 μV/°C.

According to (5), if effects from dA/A can be ignored, A should be greater than 120 dB, which can be easily achieved.

As shown in Fig. 2, the common-mode input voltage of the op-amp is about 1.018 V due to V_{REF} and V_S. To reduce this effect, the CMRR should be better than 120 dB.

To reduce the ripple and noise from the supply of the op-amp, lead-acid batteries are used in our design. To further reduce the effect from the supply, PSRR should be better than 120 dB.

In addition, the GBW and R_o should be as small as possible, because larger of them will increase the difficulty of stabilizing the feedback loop, which will be discussed in Section IV-A.

In our design, OPA227P from Texas Instruments is used. Its parameters satisfy all the requirements discussed above except that the GBW is little high for dc source.

C. MOSFET

For the MOSFET in our design, the most key parameters are r_{ds}, g_m, $R_{DS(ON)}$ (drain–source on-state resistance), C_{gs} (gate–source capacitance), and C_{gd} (gate–drain capacitance).

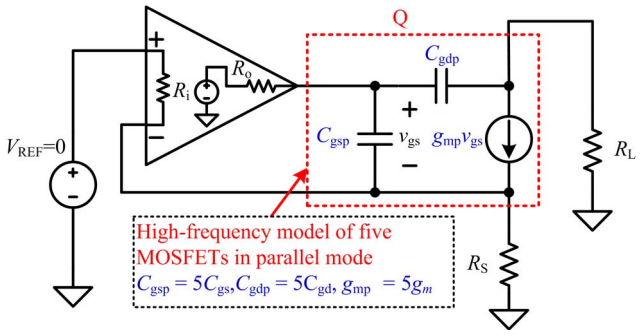

Fig. 3. High-frequency small-signal equivalent model of the 10-A VCCS to explain the reasons for oscillation.

As discussed in Section II, a larger r_{ds} is beneficial to the current stability. However, this parameter is always not given in the datasheet. Here, there is a rule of thumb that the higher $V_{DS(max)}$ (drain–source breakdown voltage) is, the more flat the output characteristic curve will be, i.e., the r_{ds} will be larger.

From the typical input characteristic curve of the MOSFET, one can see that with drain current increasing g_m will increase. So, for the same type of MOSFET, to achieve a larger g_m, drain current should be set higher. However, higher drain current means more power will be consumed, which will in turn deteriorate the stability of the MOSFET. Consequently, it is a tradeoff to set the drain current.

A larger $R_{DS(ON)}$ means more power will be consumed and more self-heat will be generated, thus will deteriorate the stability of the MOSFET and that of other components nearby. But on the other hand, from the typical on-resistance versus temperature characteristic curve in the datasheet one can see that along with temperature increasing $R_{DS(ON)}$ will increase. This is a beneficial feature when multi-MOSFETs are paralleled to use, because average-current resistors will not be necessary. Of course, all the MOSFETs should be installed in the same temperature environment.

Lower C_{gs} and C_{gd} are beneficial to the loop stabilization, thus avoid possible self-oscillation, which will be discussed in Section IV.

In our design, to reduce power consumption on each MOSFET, five IRFP460 from Vishay Group were used in a parallel mode. To further reduce power dissipation, the drain–source voltage on each MOSFET is set to 2 V. To ensure consistent temperature on each MOSFET, the five MOSFETs are fixed on a same heat sink with sufficient power.

However, multi-MOSFETs with lower drain–source voltage will bring in higher parasitic capacitance, which will deteriorate the loop stability, thus leading to oscillation.

IV. Reasons for Oscillation and Compensation

A. Reasons for Oscillation

To investigate the reasons for oscillation, the high-frequency small-signal equivalent model of the 10-A VCCS is established, as shown in Fig. 3. Shown the dotted box is the equivalent model of the five MOSFETs in parallel mode.

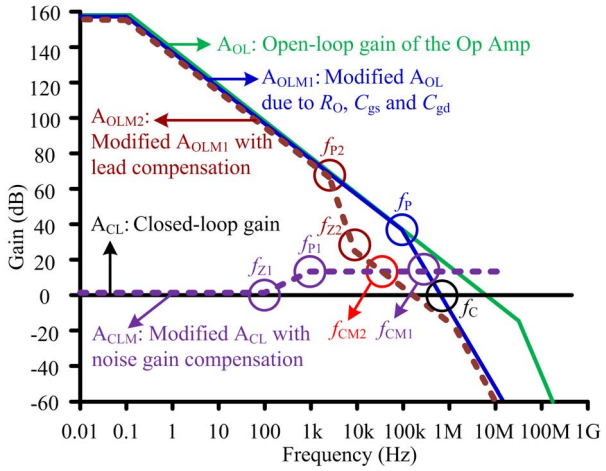

Fig. 4. Gain versus frequency plot to explain the reasons for oscillation and the method of the combined noise gain and lead compensation.

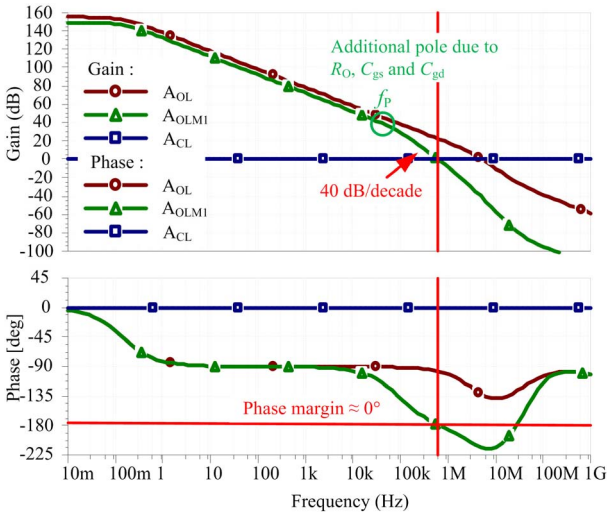

Fig. 5. Simulation plot of the gain and phase versus frequency of the 10-A VCCS without compensation to verify the explanation of the reasons for oscillation. In the simulation, op-amp = OPA227P, $C_{gs} = 4300$ pF, $C_{gd} = 3200$ pF, $R_o = 40\ \Omega$, $R_L = 0.2\ \Omega$, and $g_m = 2$.

C_{gsp}, C_{gdp}, and g_{mp} are, respectively, five C_{gs}, C_{gd}, and g_m in parallel mode. Since R_S and R_L are much smaller than r_{ds} in our design, effect from r_{ds} is ignored. For power MOSFETs, parasitic capacitances, such as C_{gs} and C_{gd}, are usually high, and they will increase with decrease of the drain–source voltage. Datasheet of IRFP460 shows that C_{gs} and C_{gd} are about 4300 and 3200 pF, respectively, when the drain–source voltage is 2 V. So, effects from C_{gs} and C_{gd} cannot be ignored.

According to Fig. 3, the β (feedback factor) of the circuit can be considered to be one, i.e., $\beta = 1$. So, the A_{CL} (closed-loop gain) of the circuit can be approximated to one, i.e., $A_{CL} \approx 1$. As shown in Fig. 4, A_{OL} is the open-loop gain of the op-amp. In high frequency, due to the effects of R_o, C_{gsp}, and C_{gdp}, there will be an additional pole at f_P with frequency about $1/2\pi R_o(C_{gsp} + C_{gdp})$, where it is assumed that R_S and R_L are so small that C_{gsp} and C_{gdp} are equivalent to grounding. Due to the additional pole, the A_{OL} curve will become A_{OLM1}. If the pole at f_P is above the A_{CL} curve, the rate-of-closure of the A_{OLM1} and A_{CL} curve will be 40 dB/decade at f_C and the circuit will be unstable.

In our design, R_o is about 40 Ω, which is the simulation vale using the method in [8]. As a result, the corner frequency at f_P will be about 106 KHz. The GBW of OPA227P given in the datasheet is 8 MHz, according to the analysis above, the circuit will be unstable.

Using the high-frequency model of the five MOSFETs in parallel mode and the method proposed in [8], we obtain the simulated gain and phase versus frequency plot of the circuit, as shown in Fig. 5. The simulation results are consistent with the approximate analysis shown in Fig. 4. The simulated corner frequency at f_P is about 93.2 kHz, which is very close to the analysis value of 106 kHz. Since the rate-of-closure of the A_{CL} and A_{OLM1} curve is about 40 dB/decade, the circuit is unstable. The figure also shows that when the loop gain (in this simulation, the loop gain curve is identical to the A_{OLM1} curve) is 0 dB, the phase margin is about 0°, which also confirms that the circuit will be unstable.

Note that the zero caused by the effects of C_{gs}, C_{gd}, R_S, and R_L are not considered, because its frequency is much higher than the unity gain frequency of the op-amp and it will be under the A_{CL} curve. Besides, the frequency prediction of f_P is under the assumption that R_S and R_L are so small that C_{gsp} and C_{gdp} are equivalent to grounding. If beyond this hypothesis, the accuracy of the estimation will be poor. To predict the accurate frequency of the corner frequency of the pole and zero, strict transfer function should be established. However, it is usually not necessary in engineering applications.

B. Compensation

According to the reasons for oscillation aforementioned, solutions can be concluded as how the op-amp driving high capacitive loads. Several methods have been proposed in [8] and a noise gain compensation method (or lag compensation) to stabilize the MOSFET-based VCCS has been proposed in [9]. However, these methods cannot be directly applied in our design. Fig. 5 shows that the gain at the additional pole f_P is about 40 dB. If only the noise gain method is used, for the A_{CL} curve, it is a long way to go from 0 to 40 dB, so more than one pole and zero will be required. As a result, the method in [9] will not be competent.

In our design, a combined noise gain and lead compensation method is used. As shown in Fig. 6, R_F, R_2, and C_2 are the components to constitute the noise gain compensation, while R_1 and C_1 form the lead compensation.

The idea of this method is using the lead compensation to modify the A_{OLM1} curve and the noise gain compensation to change the A_{CL} curve. As shown in Fig. 4, before compensation, the intersection of the A_{CL} and A_{OLM1} curve will be at f_C. By adding the noise gain compensation, there will be a zero at f_{Z1} and a pole at f_{P1}. According to Fig. 6, the corner frequency of f_{Z1} will be $1/2\pi(R_F + R_2)C_2$ and that of f_{P1} will be $1/2\pi R_2 C_2$. Since the gain at f_P is about 40 dB, at f_{CM1}, i.e., the intersection of the A_{OLM1} and

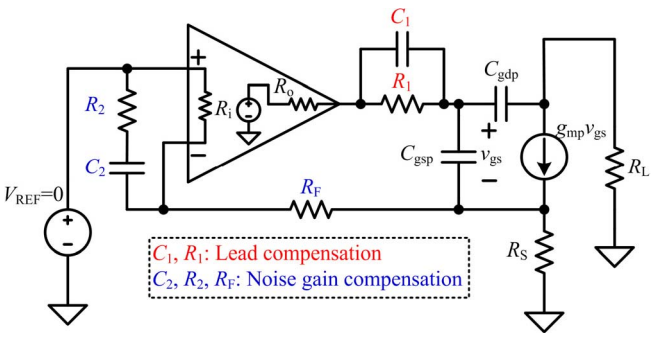

Fig. 6. Combined noise gain and lead compensation method to eliminate oscillation.

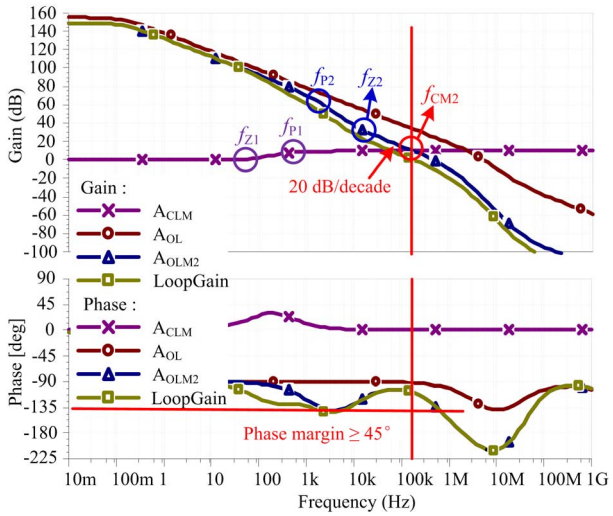

Fig. 7. Simulation plot of the gain and phase versus frequency of the 10-A VCCS with compensation to verify the proposed compensation method. In the simulation, op-amp = OPA227P, C_{gs} = 4300 pF, C_{gd} = 3200 pF, R_o = 40 Ω, R_L = 0.2 Ω, g_m = 2, R_1 = 2.4 kΩ, C_1 = 6.6 nF, R_2 = 5 kΩ, R_F = 10 kΩ, and C_2 = 100 nF.

A_{CLM} (the modified A_{CL} curve) curve, the rate-of-closure is still about 40 dB/decade. So, the circuit is still unstable. By adding the lead compensation, there will be a pole at f_{P2} and a zero at f_{Z2}. According to Fig. 6, the corner frequency of f_{P2} is approximately $1/2\pi\, R_1(C_{gs} + C_{gd})$ with an assumption of $R_1 \gg R_o$, and that of f_{Z2} is approximately $1/2\pi\, R_1 C_1$. Now, the crossover frequency will move from f_{CM1} to f_{CM2}. At f_{CM2}, the rate-of-closure will be about 20 dB/decade. So, the circuit will be stable.

To demonstrate our first-order analysis above, the circuit in Fig. 6 is simulated and shown in Fig. 7. The simulation results agree very well with our first-order analysis. The loop gain and phase plots confirm a stable circuit with phase margin of about 71° at f_{CM2}. There is a slight dip of phase to under 45° between 1 and 8 kHz but not enough to cause concern.

Note that the real values of the passive components used for compensation are different from that used for simulation because the actual C_{gsp}, C_{gdp} of the MOSFETs and R_o of the op-amp may be different from the simulation value. Besides, other parasitic effects, for example, the lead inductance and capacitance are not considered in the simulation.

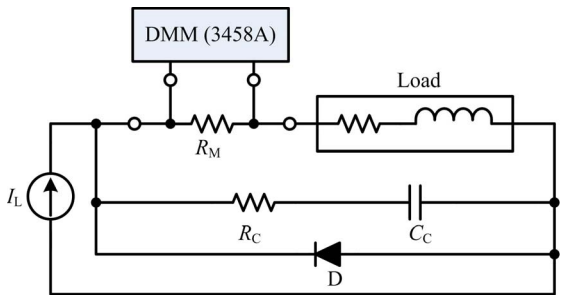

Fig. 8. Test circuit of the introduced 10-A VCCS with a practical load.

V. Measurement and Results

A design of the introduced 10-A VCCS has been constructed and experiments have also been performed. The test circuit is shown in Fig. 8.

The load is the input of a high-current meter to be evaluated, which can be equivalent to a 0.1 Ω resistor in series with a 5 mH inductor. R_C and C_C constitute the compensation net to eliminate self-oscillation caused by the inductive load. A high-speed diode with low leakage current is added to protect the source when the load current has a sudden change, which will generate a high induced voltage due to the inductor. R_M is the measuring resistor, whose characteristic is identical to R_S. Both the two resistors are calibrated under 10 A by the Guildline 6622A dc comparator resistance bridge combined with the 6623A high current range extender with transformation 100:1 and ratio accuracy ±0.4 ppm. The values of the two resistors are traceable to a 10 Ω standard resistor, which has been calibrated by the Quantum Hall Resistance standard at NIM. To guarantee the stability of the two precision resistors, a thermostatic oil bath with temperature stability of ±2 mK was used. Measurements were performed using the Agilent 3458A [8(1/2) digital multimeter] with 1 V range and a long integration time (NPLC = 100) to measure the voltage on the potential terminal of R_M. The accuracy of the multimeter, which has been calibrated by the Josephson voltage standard at NIM, is better than 0.5 ppm.

After 1-h preheating, measurements were performed in continuous 10 h and the results are shown in Fig. 9(a). In the first 5 h, the relative standard deviation (RSD) and relative current drift (RCD) are, respectively, 3×10^{-7}/5 h and 1×10^{-6}/5 h, while in the latter five hours, the RSD and RCD are, respectively, 1.2×10^{-7}/5 h and 2.6×10^{-7}/5 h. The obvious drift in the first 5 h is mainly due to the drift of the sample resistor and the measuring resistor, whose thermal equilibrium require a long time due to their large size. In the first 2 h, the RSD and RCD in 1 h are, respectively, better than 1.3×10^{-7}/h and 3.7×10^{-7}/h while in the latter 8 h, the RSD and RCD in 1 h are, respectively, better than 1×10^{-7}/h and 1.7×10^{-7}/h. In the continuous 10 h, the best result in 1 h [as shown in Fig. 9(b)] shows that the RSD and RCD are, respectively, 7.5×10^{-8}/h and 2.2×10^{-8}/h.

Although the stability of the source is better than 0.1 ppm/h, its short term (1 h) accuracy that can be guaranteed is only about 0.5 ppm, which is mainly determined by the measuring accuracy of the measuring resistor R_M and the multimeter.

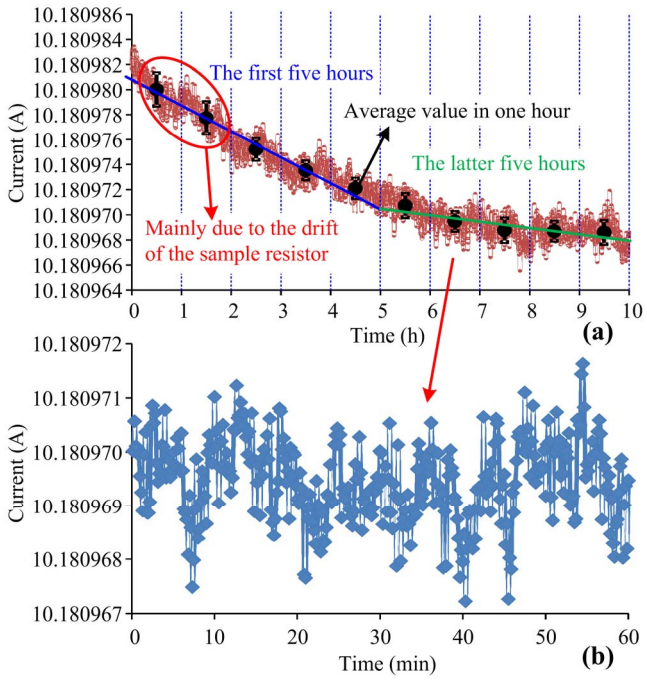

Fig. 9. Measurement results (a) in continuous 10 h and (b) in 1 h.

The repeatability of the source in 24 days is about 1 ppm, which is mainly determined by the long-term stability of the sample resistor R_S and the reference voltage V_{REF}. The relative change of R_S in a month is about 1 ppm, which is also measured by the Guildline 6623A system under 10 A. The long term stability of the V_{REF} (1.018 V output of the Fluke 732B) given in the datasheet is 0.8 ppm in a month. So determined by the two key components, the repeatability of the source is only about 1 ppm in 24 days.

VI. Conclusion

A relatively simple solution for a 10-A dc current source with stability better than 0.1 ppm/h has been introduced. Some key issues, including deviation of the strict current equation, factors determining the current stability, reasons for oscillation, as well as the compensation method of the source, have been discussed.

Test results in the latter 5 h are satisfactory, but the current in the first 5 h shows obvious drift. The drift is mainly due to the long thermal equilibrium time of the cumbersome sample resistor and the measuring resistor, which is the main problem in this design. In addition, the long-term stability and the repeatability of the source are poor and remained to improve in the future. Besides used for evaluating high-current meters, the source may be applied to estimate the stability of small resistors in the range of 0.1 mΩ to 10 Ω as described in [5]. By proper improvement, this source can be used for other cases, such as the Joule Balance Project to redefine the kilogram at NIM.

Acknowledgment

The authors would like to thank Dr. Shisong Li and Mr. Kunli Zhou from Tsinghua University for their valuable discussions. They would also like to thank the reviewers and the editors for their constructive suggestions to improve this paper.

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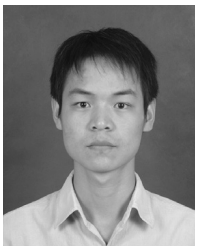

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