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Demonstration of a 10 V programmable Josephson voltage standard system based on a multi-chip technique

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Abstract

We have demonstrated a programmable Josephson voltage standard (PJVS) operation up to 10.84 V using a multi-chip technique. We combined two PJVS chips fabricated using $NbN/(TiN_x/NbN)_2$ junction technology. Each PJVS chip was mounted on a single chip carrier using bonding wire, and the two chip carriers were connected by a simple Cu lead wire, and mounted on a cryocooler. High-precision measurements confirmed flat voltage steps for all 22 cells, with a peak-to-peak variation of 100 nV and wide margins of at least 0.35 mA. We also confirmed the stability of the voltage steps in spite of a temperature and RF frequency variation of ± 0.1 K and ± 0.1 GHz, respectively.

1. Introduction

A programmable Josephson voltage standard (PJVS) [1] is more practical than a conventional Josephson voltage standard based on a superconductor–insulator–superconductor Josephson junction (JJ): its advantages include short voltage-setting time and high immunity to noise. These merits also enable its flexible use as a digital-to-analog converter (DAC). PJVS systems with a practical voltage amplitude of about 1 V have been developed [2–6].

PJVSs with a much higher voltage amplitude of 10 V are also being studied. This is a very challenging subject, since highly advanced fabrication technology is needed to integrate the huge number of JJs used. So far, the Physikalisch-Technische Bundesanstalt (PTB) has obtained 10 V by using an array of $Nb/AlO_x/Al/AlO_x/Nb$ junction technologies [7] (the number of JJs is 69 120, and the RF frequency is about 70 GHz). The National Institute of Advanced Industrial Science and Technology (AIST) has also obtained 10 V using an array based on $NbN/(TiN_x/NbN)_2$ double-barrier junction technology [8, 9] (327 680 JJs, RF frequency about 16 GHz). The National Institute of Standards and Technology (NIST) has obtained 3.9 V using $Nb/(MoSi_2/Nb)_3$ triple-barrier junction technology [10] (101 115 JJs, RF frequency about 18.5 GHz): about 300 000 JJs will be necessary to obtain 10 V if using the same fabrication technology. However, it is still difficult to obtain 10 V PJVS chips with a high fabrication yield, since numerous JJs are required; this remains the most significant problem.

To overcome this problem, we have applied a multi-chip technique to create a 10 V PJVS. In this paper, we first explain the need for a multi-chip technique, then describe the cryopackaging and construction of the 10 V multi-chip PJVS system, and finally report the results of high-precision voltage measurement results for the system.

2. Need for a multi-chip technique

In the 10 V PJVS chip fabricated using the AIST $NbN/(TiN_x/NbN)_2$ process [8, 9], the PJVS array contains 327 680 JJs and the RF frequency is 16 GHz, which *corresponds* to 10.84 V. The array is divided into 16 equal cells with 20 480 JJs in each. To operate it as an 11-bit DAC, one of these cells is further divided into 7 sub-cells containing a smaller number of JJs: 320, 320, 640, 1280, 2560, 5120, and 10 240 in each. (The total number of cells is 22 per chip.) Because the voltage of each of 16 larger cells is about 677 mV, at least 15 of the larger cells are required to reach a total voltage of 10 V.

Table 1 shows the bias margins of $n = +1$ voltage steps for two 10 V PJVS chips fabricated using the above-mentioned AIST process. In both chips, there are two or more defective

Table 1. Bias margins of voltage steps for PJVS cells in two chips. The defect cells are denoted by 'N/A'. By using all correct cells, chip #1 and chip #2 can generate the maximum voltage of 9.48 V and 4.74 V, respectively. In combining these two chips, we chose the 22 cells having the widest margins (marked with '∗') among those correct cells.

Cell # (# of JJs)	Chip#1 margin (mA)	Chip#2 margin (mA)
1 (320)	∗0.80	N/A
2 (320)	∗1.08	N/A
3 (640)	∗0.66	N/A
4 (1280)	∗0.78	N/A
5 (2560)	∗0.58	N/A
6 (5120)	∗1.28	N/A
7 (10 240)	∗0.58	N/A
8 (20 480)	N/A	0.42
9 (20 480)	N/A	N/A
10 (20 480)	0.78	∗0.80
11 (20 480)	0.84	∗0.82
12 (20 480)	0.22	∗0.60
13 (20 480)	∗0.96	N/A
14 (20 480)	∗0.84	N/A
15 (20 480)	∗0.78	∗0.78
16 (20 480)	∗0.76	∗0.74
17 (20 480)	∗0.84	∗0.86
18 (20 480)	∗0.94	N/A
19 (20 480)	∗0.90	N/A
20 (20 480)	0.52	N/A
21 (20 480)	∗0.80	N/A
22 (20 480)	∗0.88	N/A

cells that do not have the $n = +1$ correct voltage steps (denoted by 'N/A' in the table). So both chips cannot generate 10 V independently, due to lack of voltage: the maximum voltages is 9.48 V in chip #1 and 4.74 V in chip #2. This is the reason why a 10 V system using a single chip only is difficult to obtain, making it necessary to employ a multi-chip technique. By combining those two PJVS chips, we will be able to obtain a voltage that exceeds 10 V. Therefore, in this research, we combined those two PJVS chips and developed a 10 V PJVS system by multi-chip (dual-chip) packaging.

3. Connection of PJVS chips

3.1. Voltage drop at the chip-to-chip connection

In a dual-chip PJVS, two PJVS arrays (chips) need to be connected to each other. The key problem is the voltage drop at the chip-to-chip connection, which leads to a decrease in voltage accuracy. This occurs because a small part of the bias current undesirably flows along the chip-to-chip connection which would generally be a normal conductor with a finite resistance. If a floating current source is used, as shown in figure 1(a), the bias current will ideally flow in each cell only and does not flow out along the connection. For noise immunity, however, we employed pairs of grounded current sources that are of opposite sign, and equal in magnitude (supplying source: I_+, return source: I_-) as shown in figure 1(b). (Even if the noise of floating source may not be so large as to disturb the measurement it will be costly, both economically and in terms of hardware, to get 22 floating sources for realizing a 11-bit DAC.) Each cell is biased

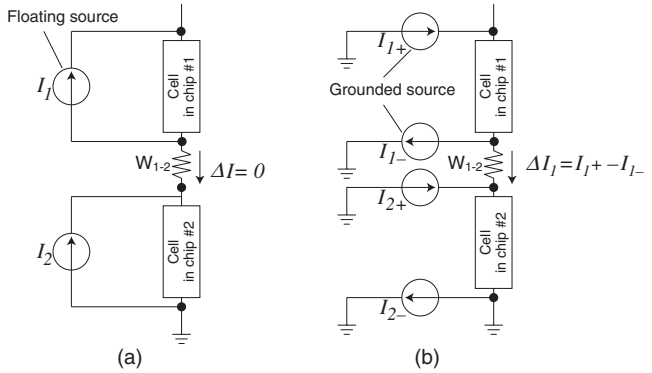

Figure 1. Circuit diagram of bias current sources supplying to the PJVS cells. (a) Bias supplying using a floating current source to each cell. Since the chip-to-chip connection 'W_{1-2}' is out of the loops of the current sources, no current will flow along the connection. (b) Bias supplying using pairs of grounded current sources (I_{1+}, I_{1-}). Generally, I_{1+} and I_{1-} are not perfectly equal to each other because of the variation of resistors in the current sources. Therefore, the unbalanced current from the chip #1 ($\Delta I_1 = I_{1+} - I_{1-}$) will flow to the chip #2 along the connection.

differentially by this pair of sources. However, there is generally a little difference in magnitude between those two current sources ($\Delta I = I_+ - I_- \neq 0$), caused by variations in the resistors used in the current sources. Here we will use the term 'unbalanced current' to refer to the difference in the currents of the pair. Unbalanced current will flow out of the connected cell and to an adjacent cell along the connection between cells. We estimated that the unbalanced current per cell was about 10 μA (this is because the supplied bias current to each cell is about 10 mA, and the variation in resistance in the current source is about 0.1%). In our dual-chip PJVS, an unbalanced current will flow through the chip-to-chip connection (W_{1-2} in figure 1(b)). Since each chip has an average of 11 cells (half the total number of cells), about 110 μA($= 10\ \mu\text{A} \times 11$) will accumulate as the total unbalanced current along the chip-to-chip connection.

3.2. Chip-to-chip configurations and cryopackaging

The most direct way to reduce the voltage drop is to employ a superconductor for the chip-to-chip connection because it has zero resistance. This can be achieved by using a multi-chip module based on flip-chip bonding with superconducting wires and superconducting solder bumps (figure 2(a)). However, the critical temperature of the superconducting solder bumps is lower (even InSn solder is 5 K) than the operating temperature of our NbN-based PJVS (10 K). Furthermore, flip-chip bonding sometimes causes a deterioration of the electrical characteristics of the chips.

For these reasons, we employed a structure shown in figure 2(b), in which two carriers are connected using a simple Cu lead wire. Although the chip-to-chip connection has a finite resistance, packaging is easy. We therefore connected two chips (the previously mentioned chip #1 and chip #2) in the configuration shown in figure 2(b). Each chip was independently mounted on a single chip carrier and connected to it using bonding wire instead of flip-chip bonding. To

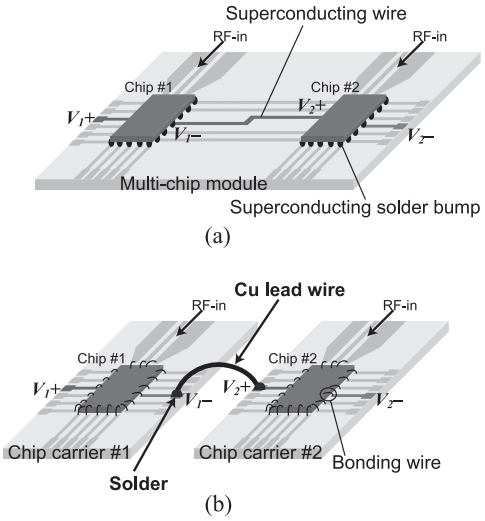

Figure 2. Configurations of a chip-to-chip connection. (a) The most direct way to connect chips is using a multi-chip module based on a superconducting flip-chip bonding. In this method, however, the critical temperature of solder bump is at most 5 K and is lower than the operating temperature of the PJVS chip. In addition to this, flip-chip bonding causes deterioration of chips. (b) Each chip is mounted on a single carrier independently. Two carriers are simply connected by a Cu lead wire.

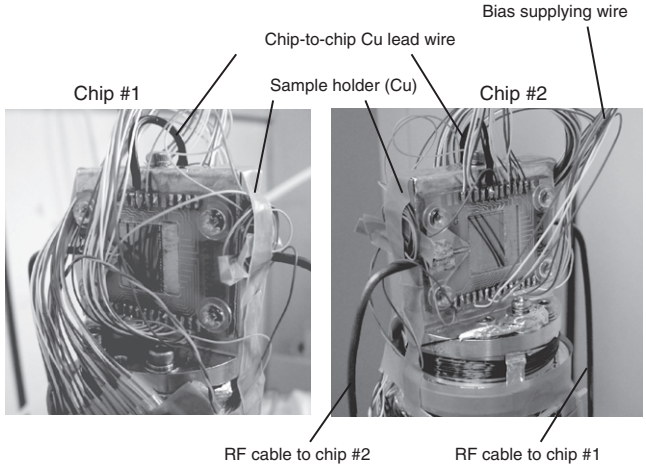

Figure 3. A photograph of the dual chip mounted on the sample holder of a cryocooler. For a simple and compact packaging, we designed the sample holder as the standing Cu board where two chip carriers are mounted back-to-back with the chips facing each other.

reduce the resistance, we placed three bonding wires (diameter 10 μm) in parallel. To achieve simple and more compact packaging, we designed the sample holder as a standing Cu board with two chip carriers facing each other back-to-back. We used a short (about 5 cm long) Cu lead wire with a cross section of 0.5 mm^2, and connected it to the chip carriers using solder. Figure 3 is a photograph of the two chips mounted on the sample holder on a Gifford–McMahon (GM) cryocooler.

We measured the resistances of each section of the chip-to-chip connection (Cu lead wire, wire on chip carrier, and bonding wire) individually using the four-terminal method at an operating temperature of 10 K. The results are shown in table 2. The total resistance of the interconnection was 2.24 mΩ. It is clear that the bonding wire has by far the highest resistance (2.30 mΩ per wire), but it can be drastically reduced by using ribbon bonding instead. The resistance of the chip carrier is not low because we simply used the conventional chip carriers designed for single-chip packaging (the wire is narrow, at 200 μm width). We plan to redesign the chip carrier and increase the wire width to 500 μm.

Table 2. Resistances of the chip-to-chip connection at 10 K. We measured the resistance at each section of the connection (bonding wire, wire on chip carrier, and Cu lead wire) by using the four-terminal method. The reason why we should multiply the resistance of bonding wire by two and divide by three is that it includes two connecting points of bonding between the chip and the carrier, and that we placed three wires in parallel to reduce the resistance. The reason for multiplying the resistance of the carrier by two is that it includes two carriers.

Type of wiring	Resistance @10 K (mΩ)
Cu lead wire (A)	0.05 ($L = 50$ mm, $S = 0.5$ mm^2)
Al bonding wire (B)	2.30 (per wire)
Cu chip-carrier wire (C)	0.33 ($L = 5$ mm, $W = 200$ μm)
Total ($A + B/3 \times 2 + C \times 2$)	2.24

From the estimated unbalanced current and measured resistance above, we estimated the voltage drop to be about 250 nV (= 2.24 m$\Omega \times 110$ μA). This corresponds to 0.03 ppm for 10 V. This may be practical as a secondary standard, but is not small enough for a primary standard. The voltage drop can be reduced further by replacing the bonding wire with ribbons and increasing the width of the wires on the chip carrier.

4. High-precision measurement of voltage steps

4.1. System configuration

For operation as a 10 V 11-bit DAC, 22 cells including 7 smaller cells are necessary. In this experiment, among the 44 cells in chip #1 and chip #2, we chose 22 working cells with wide bias margins (marked by '$*$' in the table 1). In this combination, we can obtain the maximum voltage of 10.84 V, whereas the voltages of chip #1 and chip #2 are 6.77 V and 4.06 V, respectively. We connected 22-channel bias current sources to those chosen cells. The remaining 22 cells are defect or small-margin cells, and bias sources were not connected (the bias currents were zero). Since these defective cells have $n = 0$ steps of about 4 mA width, they will not have an unfavorable influence on the voltage steps of the correct cells. We connected two RF sources, a digital voltmeter (DVM: Agilent 3458A), and a temperature controller (Lakeshore Model 331) to the 10 V PJVS system. We also developed software for automatic measurement.

4.2. High-precision measurement

We evaluated constant voltage steps for 22 cells individually. If used as the primary standard, voltage steps should be measured with a resolution of 10 nV. To measure voltages at such high resolution, we adopted a null method in which the voltage sensitivity of the DVM is maximized and reading errors of

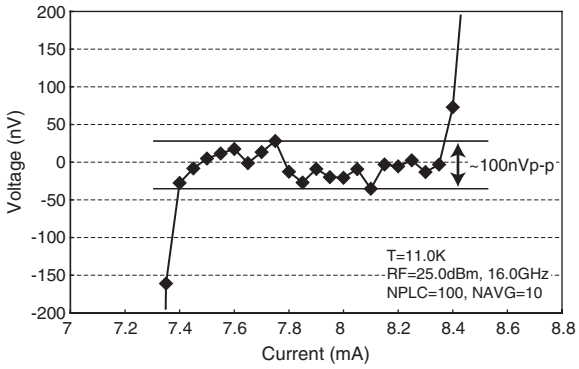

Figure 4. I–V curves of voltage steps using the null method for cell #1 as a typical curve in the dual-chip PJVS array. The peak-to-peak variation of the voltage steps was about 100 nV.

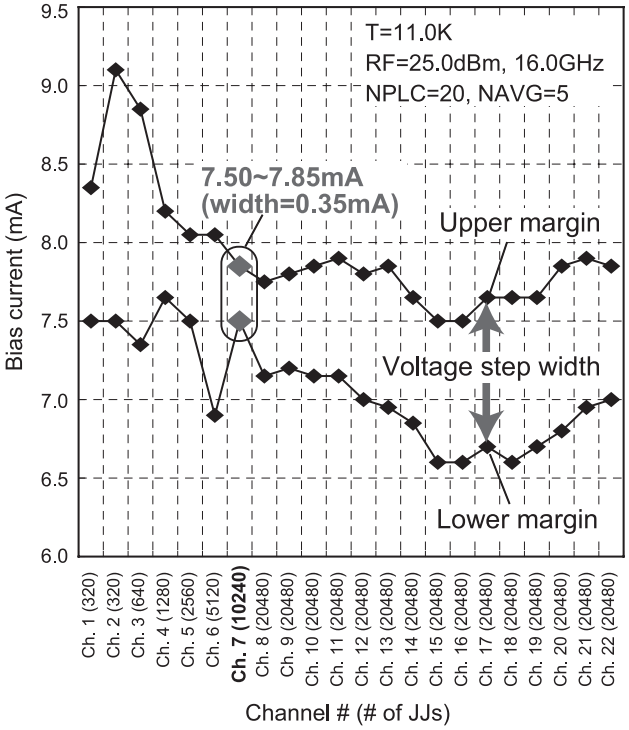

Figure 5. Bias margins of the $n = +1$ step for all 22 cells. The lower and upper limits of current margins are shown. Cell #7 has the minimum bias margin of 0.35 mA.

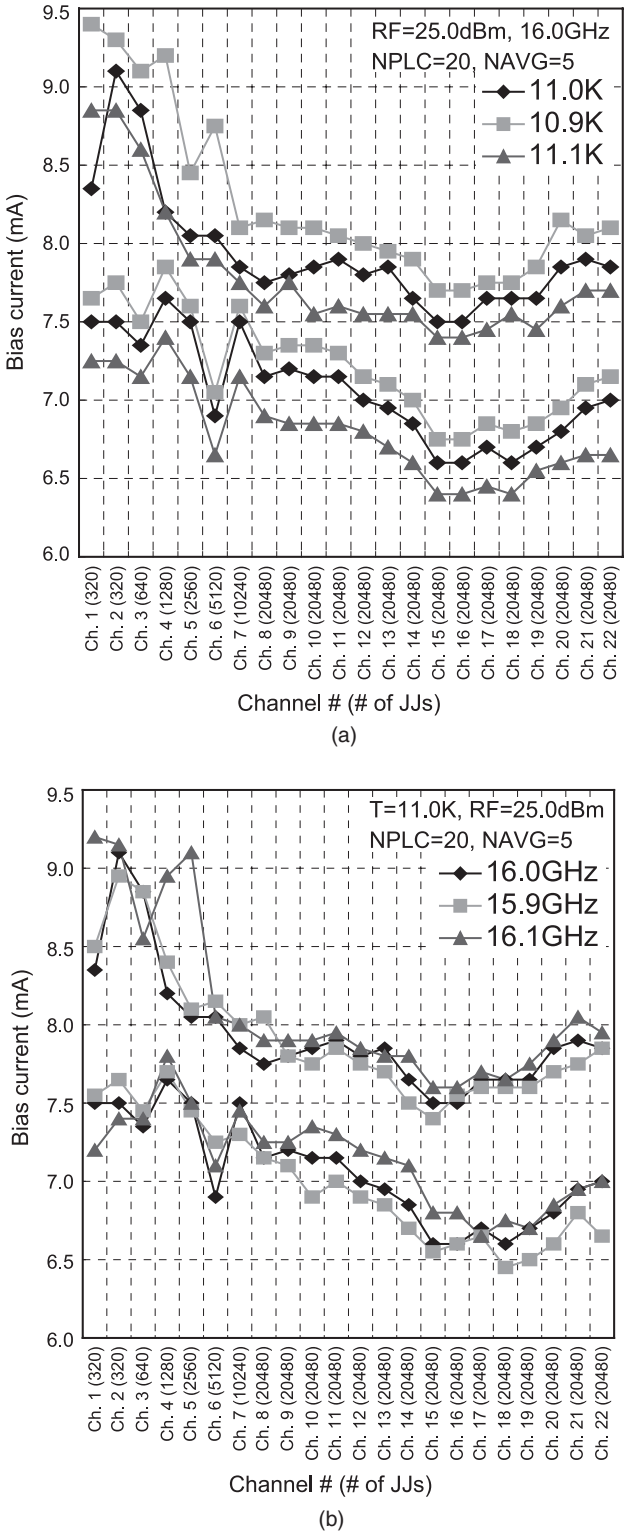

Figure 6. Measurement results of the voltage steps with parameter deviations. The lower and upper limits of current margins are shown. (a) The temperature is changed by ±0.1 K from the optimum value of 11.0 K. (b) The RF frequency is changed by ±0.1 GHz from the optimum value of 16.0 GHz.

the DVM are avoided. In this method, two cells with the same number of JJs are employed in the following way: the bias current to one cell is swept around the $n = +1$ step and the voltage is measured while the other is fixed on the center of the $n = -1$ step. Moreover, in this method, the voltage of the PJVS array in the zero-voltage state (the zero-biased state) was subtracted to avoid offset voltages such as the thermo-electromotive force on the output voltage lead wire and zero error of the DVM. Figure 4 shows the results of the $n = +1$ voltage steps for cell #1 as a typical curve. During this measurement, all parameters were controlled at the optimum points: the microwave power and frequency were 25.0 dBm and 16.0 GHz, respectively, for both chips, and the temperature was 11.0 K. At this temperature, the $I_c R_n$ product is equal to about 33 μV where the characteristic frequency is nearly equal to the RF frequency of 16 GHz. In this condition, the

nominal critical current is about 5.5 mA. As seen in the graph, a flat voltage step was obtained with a peak-to-peak variation of about 100 nV. We also confirmed the flat voltage steps of the remaining 21 cells. This is the same level as the maximum sensitivity of the DVM, which means that all 22 cells have perfectly flat voltage steps, indicating that the total voltage of 10.84 V is obtained by supplying bias currents to all 22 cells. Comparison of our developed 10 V PJVS system with the 10 V primary voltage standard of NMIJ/AIST is now under way.

We also show the bias margin of the $n = +1$ steps of the 22 cells in figure 5. As seen in the figure, cell #7 has the narrowest bias margin of 0.35 mA: its main cause is likely to be flux trapping in the chip. Actually, we measured cell #7 several times, warming the chips to 20 K and then recooling to 11 K. The margin had strong probabilistic variations. But we do not know why cell #7 is easy to have flux trapping. On the other hand, the remaining 21 cells have sufficiently large margins of at least 0.5 mA (averaging 1.0 mA).

Under more realistic conditions, the temperature varies due to the cycle of the GM cooler. The RF frequency is also changed to adjust the voltage precisely. The voltage steps need to be tolerant of parameter variations such as these. We therefore evaluated the voltage steps at a temperature and RF frequency variation of ± 0.1 K and ± 0.1 GHz, respectively. The results of the current position of the $n = +1$ step are summarized in figures 6(a) and (b). Figure 6(a) shows that the voltage steps are stable even when the temperature varies by ± 0.1 K, which is larger than the actual variation of ± 0.05 K. We also obtained a wide step width through the frequency range of 16 ± 0.1 GHz, as shown in figure 6(b). Our PJVS can therefore be used not only for a 10 V system, but also for a 1 V system. This is because the resolution of the DAC is 11 mV, and the voltage around 1 V is covered continuously by adjusting the frequency within the 16 ± 0.1 GHz range. These results indicate that our dual-chip technique is sufficiently reliable and effective for use as a 10 V PJVS.

5. Conclusion

We have demonstrated the PJVS operation up to 10.84 V using a dual-chip technique. Each PJVS chip was mounted on a single carrier using bonding wire, and the two carriers were connected by a simple Cu lead wire, and mounted on a cryocooler. High-precision measurements confirmed flat voltage steps for all 22 cells, with a peak-to-peak variation of 100 nV and wide margins of at least 0.35 mA. We also confirmed the stability of the voltage steps in spite of a temperature and RF frequency variation of ± 0.1 K and ± 0.1 GHz, respectively. The voltage drop at the chip-to-chip connection was estimated to be about 250 nV, corresponding to 0.03 ppm for 10 V. However, it will also be useful for the primary standard by reducing the chip-to-chip resistance: replacing the bonding wire with ribbons and increasing the width of the wires on the chip carrier.

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