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A novel low-voltage high precision current reference based on subthreshold MOSFETs

YU Guo-yi†, ZOU Xue-cheng

(*Department of Electronic Science & Technology, Huazhong University of Science and Technology, Wuhan 430074, China*)

†E-mail: ymancheng@yahoo.com.cn

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Abstract: A novel topology low-voltage high precision current reference based on subthreshold Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) is presented. The circuit achieves a temperature-independent reference current by a proper combination current of two first-order temperature-compensation current references, which exploit the temperature characteristics of integrated poly2 resistors and the *I-V* transconductance characteristics of MOSFET operating in the subthreshold region. The circuit, designed with the 1st silicon 0.35 μm standard CMOS logic process technology, exhibits a stable current of about 2.25 μA with much low temperature coefficient of 3×10^{-4} μA/°C in the temperature range of −40~150 °C at 1 V supply voltage, and also achieves a better power supply rejection ratio (PSRR) over a broad frequency. The PSRR is about −78 dB at DC and remains −42 dB at the frequency higher than 10 MHz. The maximal process error is about 6.7% based on the Monte Carlo simulation. So it has good process compatibility.

Key words: Current reference, Curvature-compensation, Low voltage, Subthreshold, CMOS integrated circuit
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INTRODUCTION

With the development of modern electronics, there is a growing trend of designing a low-voltage high precision current reference in many mixed-signal and analog circuits such as data converters (Mehr and Singer, 2000; Oh *et al*., 2004), oscillators and PLLs (Razavi, 2001; Banba and Shiga, 1999). Low-cost reasons need the reference to be realized in simple standard CMOS logic process technology, without resorting to the use of BiCMOS process and special devices such as floating-gate device (Ahuja *et al*., 2005; Chen and Shi, 2003). Since the current of a MOSFET operating in subthreshold region is very small and the current-mode circuit exhibits better performance than voltage-mode circuit in low-voltage conditions, a few researchers are focusing on using MOSFETs operating in subthreshold region to design the low-voltage low-power current reference with high precision (Huang *et al*., 2006; Liu and Kursun, 2006; Giustolisi and Palumbo, 2003).

Filanovsky and Allam (2001) studied the temperature characteristic of MOSFET biased in saturation region and pointed out clearly that below a certain bias point, which depends on the technology adopted, the gate-source voltage of a MOSFET biased with a fixed drain current decreases with the temperature in a quasi-linear fashion. As a result from this observation, a gate-source voltage can be used instead of a base-emitter voltage to design a current or voltage reference independent of temperature.

This work designs a first-order pure MOSFETs current reference, which exploits the temperature characteristic of the integrated poly2 resistor and the *I-V* transconductance characteristic of a MOSFET operating in subthreshold region. To improve the temperature characteristic of the current reference, a high-order temperature compensation approach based on a novel topology structure is described in this paper. The basic principle is to sum up two first-order weighted current references. One is scaled curvature-down and other is scaled curvature-up.

GATE-SOURCE VOLTAGE TEMPERATURE BEHAVIOR IN SUBTHRESHOLD MOSFET

In subthreshold region, a MOSFET can be used as a bipolar transistor whose current I_{ds} changes exponentially with variations in V_{gs}. The *I-V* transconductance characteristic of the MOSFET operating in subthreshold region is given by Taur and Ning (1998)

$$I_{ds}=n\mu C_{ox}\left(\frac{W}{L}\right)V_T^2\exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right)\left[1-\exp\left(-\frac{V_{ds}}{nT}\right)\right], \quad (1)$$

where C_{ox}, W/L, V_{ds}, V_{th}, $V_T=KT/q$, n and μ being respectively the gate-oxide capacitor per unit area, the width and length ratio of MOSFET, the drain-source voltage, the threshold voltage, the thermal voltage, the slope factor and the mobility. The slope factor n can be expressed as (Tsividis, 1999)

$$n=1+C_{dep}/C_{ox}\approx 1.5, \quad (2)$$

where C_{dep} is the surface depletion capacitor. And the mobility μ is dependent on the temperature and is given by Sze (2002)

$$\mu(T)=\mu(T_0)(T/T_0)^{-m}, \quad (3)$$

where $\mu(T_0)$ is the mobility at the reference temperature T_0, and $1\leq m\leq 2$.

When the MOSFET is used as diode-connected structure, the drain-voltage V_{ds} is much greater than the thermal voltage V_T. So the last term in Eq.(1) can be eliminated. Substitute Eq.(3) into Eq.(1) to get the gate-voltage V_{gs}

$$V_{gs}=V_{th}+nV_T\ln\left[\frac{I_{ds}L}{n\mu(T_0)(T/T_0)^{-m}C_{ox}WV_T^2}\right]. \quad (4)$$

Assuming m=2 for estimation and keeping I_{ds} constant, differentiate Eq.(4) with respect to temperature to get

$$\frac{\partial V_{gs}}{\partial T}=\frac{\partial V_{th}}{\partial T}+\frac{nK}{q}\ln\left[\frac{I_{ds}LT_0^2}{n\mu(T_0)C_{ox}WV_T^2}\right]. \quad (5)$$

Eq.(5) shows that the term within the "ln" function is much smaller than 1, which means the second term in Eq.(5) is negative. Together with the negative temperature coefficient of the threshold voltage, the gate-source voltage of MOSFET has a negative temperature coefficient and can be expressed as the equation below with the first order equivalence

$$V_{gs}=A-BT, \quad (6)$$

where $A>0$, $B>0$, V_{gs} decreases with temperature.

FIRST-ORDER PURE MOSFETS CURRENT REFERENCE

The proposed first-order pure MOSFETs reference current circuit is shown in Fig.1. The circuit includes two symmetric subcircuits. One is a scaled curvature-down reference current and the other is a scaled-up reference current. The following circuit analysis is based on the left part. The diode-connected M_1 and M_2 operate in subthreshold region instead of the base-emitter junction in the conventional bandgap reference. The Op-AMP forces the voltage of R_1 and R_2 to be equal so the currents are equal in the resistance of R_1 and R_2.

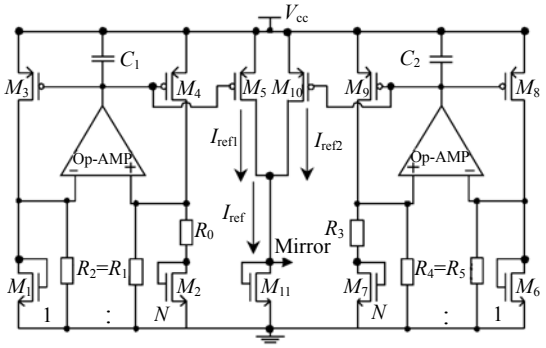

Fig.1 Proposed reference current circuit

Assuming $(W/L)_2/(W/L)_1=N=6$, $(W/L)_3/(W/L)_4=1$, according to Eq.(4), the current in the resistance R_0 can be given by

$$I_{R_0}(T)=\frac{V_T\ln N}{R_0(T)}. \quad (7)$$

Thus the reference current I_{ref1} can be obtained as

$$I_{ref1}(T)=I_{R_1}(T)+I_{R_0}(T)=\frac{V_{gs}(T)}{R_2(T)}+\frac{V_T\ln N}{R_0(T)}. \quad (8)$$

According to the 1st silicon 0.35 μm standard CMOS logic process technology, the high resistive poly2 resistance is negative temperature coefficient for the first order and the low resistive poly resistance is positive temperature coefficient for the first order. They can be written as

$$\left.\begin{aligned} R_{\mathrm{hr}}(T) &= R_{\mathrm{hr0}}(T_0)[1-\lambda_1(T-T_0)],\\ R_{\mathrm{lr}}(T) &= R_{\mathrm{lr0}}(T_0)[1+\lambda_0(T-T_0)],\end{aligned}\right\} \tag{9}$$

where λ_1=5.03×10^{-4} and λ_0=4.74×10^{-3}. If R_1 and R_2 are implemented by the high resistive poly2 and R_0 is implemented by the low resistive poly2, Eq.(8) can be expressed as (omitting the high-order terms)

$$I_{\mathrm{ref1}} = \frac{A-BT}{R_1(T_0)}[1+\lambda_1(T-T_0)]+\frac{V_{\mathrm{T}}\ln N}{R_0(T_0)}[1-\lambda_0(T-T_0)]. \tag{10}$$

The first-order temperature compensation current I_{ref1} is achieved, then the ratio m_1 of $R_1(T_0)/R_0(T_0)$ should satisfy

$$m_1 = \frac{R_1(T_0)}{R_0(T_0)} = \frac{B(1+\lambda_0 T_0)-A\lambda_1}{(1-\lambda_0 T_0)(K/q)\ln N}. \tag{11}$$

Two-order differentiating Eq.(10) with respect to temperature to get

$$\frac{\mathrm{d}^2 T_{\mathrm{ref1}}}{\mathrm{d}T^2} = -2[B\lambda_1 + m_1\lambda_0(K/q)\ln N]. \tag{12}$$

The values of B, λ_0, λ_1 and m_1 are positive, so $\mathrm{d}^2 I_{\mathrm{ref1}}/\mathrm{d}T^2<0$. That is, the first-order temperature compensation current I_{ref1} is scaled curvature-down. To the right part, if R_4 and R_5 are implemented by the low resistive poly1 and R_3 is implemented by the high resistive poly2, based on the same deductive method, the scaled curvature-up current I_{ref2} can be obtained and the first-order temperature compensation condition is given by

$$m_2 = \frac{R_4(T_0)}{R_3(T_0)} = \frac{B(1-\lambda_1 T_0)-A\lambda_0}{(1+\lambda_1 T_0)(K/q)\ln N}. \tag{13}$$

As a result from the above observation, the high-order temperature compensation current I_{ref} can be achieved by the combination of the appropriate scaled curvature-down I_{ref1} and the scaled curvature-up I_{ref2}, that is

$$I_{\mathrm{ref}} = CI_{\mathrm{ref1}} + DI_{\mathrm{ref2}}, \quad C/D = m_2/m_1. \tag{14}$$

According to the implementation circuit in Fig.1, the design should satisfy

$$\frac{(W/L)_5/(W/L)_4}{(W/L)_9/(W/L)_{10}} = \frac{C}{D} = \frac{m_2}{m_1}. \tag{15}$$

The bypass capacitors C_1 and C_2 in Fig.1 are the high frequency compensation capacitors. Designing the proper value of the capacitors C_1 and C_2 would enhance the power supply rejection ratio (PSRR) of the output reference current too much.

According to Eq.(12), the poly sheet resistivity variation does not change the convex curvature of I_{ref1}. Based on the same analysis, the poly sheet resistivity variation also does not change the concave curvature of I_{ref2}. In Eq.(8), the poly sheet resistivity variation only makes a weighted difference of the current I_{ref}. So the temperature coefficient of the reference current I_{ref} is independent of the poly sheet resistivity variation. Correcting of the current I_{ref} value is only to trim the number of the mirror NMOS, M_{11}. In this case, the mirror NMOS number is 24 besides 8 for laser trimming. It can correct the ±20% error of the reference current.

LOW-VOLTAGE OP-AMP DESIGN

Because a pMOS differential pair Op-AMP has lower input common-mode voltage than an nMOS differential pair Op-AMP, the Op-AMP in conventional reference circuit often employs the pMOS differential pair Op-AMP. However the minimum supply voltage is about 1.5 V due to the pMOS differential pair for the Op-AMP. When the supply voltage is lower than 1.5 V, it will force the tail MOSFET into triode region and causes a decrease of the bias current and then degrades the performance of the common-mode rejection ratio. Consequently, the pMOS differential arrangement Op-AMP is not suitable for the low supply reference circuit.

The problem described above can be eliminated by using a two-stage folded nMOS differential pair

configuration Op-AMP as shown in Fig.2. It is composed of a soft-start circuit, a self-bias circuit, two-stage folded nMOS differential pair Op-AMP and an R-C compensation network for achieving a sufficient stability margin. The soft-start circuit and self-bias circuit are jointly-owned by the two Op-AMPs. To analyze the circuit conveniently, they are drawn into one Op-AMP circuit. In this configuration, the gate-voltage of the differential nMOS is biased by the drain-source voltage of diode-connected subthreshold M_1 and M_2. The bias current of M_{A4} and M_{A5} of the fold Op-AMP is larger than the tail current to avoid the current of the fold current mirror decreasing down to zero, while one of the two input differential nMOSFETs has zero current and the other one has the whole tail current. By means of studying the proposed Op-AMP circuit using small-signal analysis, the total voltage gain A_V is approximately expressed as

$$\left.\begin{aligned} A_V &= g_{m1}g_{m11}(r \,\|\, r_{o9})(r_{o10} \,\|\, r_{o11}),\\ r &= r_{o7} + (r_{o2} \,\|\, r_{o5})(1 + g_{m7}r_{o7}),\end{aligned}\right\} \tag{16}$$

where g_{mj} and r_{oj} respectively indicate the transconductance and the output resistance of M_{Aj}, and j is the footnote. The small frequency voltage V_s of the supply will couple into the Op-AMP output through the frequency compensation capacitor C_C. So the PSRR of the Op-AMP is not very high in the high frequency conditions, but this is useful for enhancing the PSRR of the output reference current. The PSRR can be expressed by

$$\left.\begin{aligned} PSRR(s) &= \frac{s+\omega_{p1}}{s+\omega_T}, \quad \omega_T = \frac{g_{m1}}{C_C},\\ \omega_{p1} &= [g_{m11}(r \,\|\, r_{o9})(r_{o10} \,\|\, r_{o11})C_C]^{-1}.\end{aligned}\right\} \tag{17}$$

In Eq.(17), ω_{p1} and ω_T respectively indicate the dominant pole and the unit gain bandwidth (GB). To improve the Op-AMP's precision, we would design its open-loop gain to be as high as possible. As result from Eq.(17), the Op-AMP's PSRR is increased, but the PSRR of the output reference current is decreased. So it is necessary to add the high frequency compensation capacitors C_1 and C_2 (that is, bypass capacitor, C_{bypass}) as shown in Fig.1.

Unfortunately, there are two equilibrium points: one at the desired operation point and another at zero point. To ensure the current reference always ends up smoothly to the correct operation point, a practical soft-start circuit shown in Fig.2 is designed. The soft-start circuit includes a self-bias peaking current mirror. During power up, the M_{B1} operates in triode region and produces a current I_b to startup itself. Due to the voltage-drop on the resistance R_s, M_{B2} operates in saturation region but M_{B3} operates in subthreshold region. Because the current I_0 produced by M_{B3} charges the MOSFET capacitor C_{MS6}, the startup current produced by the M_{B4} increases smoothly until the whole circuit operates on the correct point. Then the startup current would be turned off by M_{S5}. It is important to design a proper value of the width and length ratio of M_{S2} and M_{S3}, which determines the

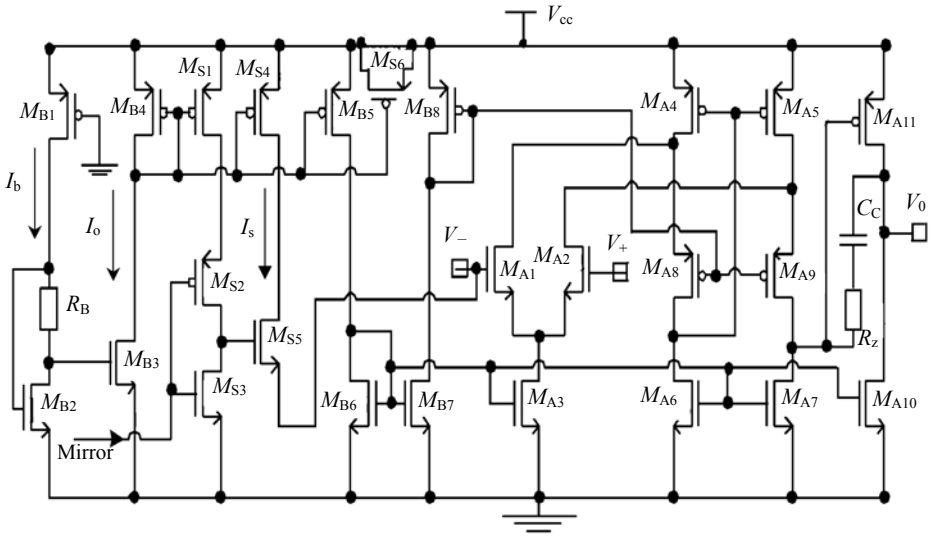

Fig.2 Low-voltage nMOSFETs Op-AMP circuit

startup circuit's end-point. The current I_0 and I_b are given by

$$\left.\begin{aligned} I_0 &= I_b\left(\frac{W}{L}\right)_{M_{B3}}\left(\frac{L}{W}\right)_{M_{B2}}\exp\left(-\frac{I_b R_s}{nV_T}\right), \\ I_b &= \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{M_{B1}}(V_{cc}-|V_{tp}|)(V_{cc}-V_{tn}), \end{aligned}\right\} \quad (18)$$

where μ_p, V_{tp} and V_{tn} are the mobility, and threshold voltage of pMOSFET and nMOSFET, and V_{cc} is the supply voltage. When I_b equals nV_T/R_s, I_0 reaches its maximal current value.

SIMULATION RESULTS

The performance of the proposed reference current circuit is verified by Hspice simulation. The simulation was carried out with 1st silicon 0.35 μm standard CMOS logic process technology.

The temperature dependence characteristic of I_{ref1} through M_5, I_{ref2} through M_{10} and their combined current I_{ref} through M_{11} are shown in Fig.3. The temperature coefficient of I_{ref1}, I_{ref2} and I_{ref} are respectively 4.355×10^{-3} μA/°C, 3.955×10^{-3} μA/°C and 3×10^{-4} μA/°C. So the novel temperature compensation approach is a very effective measure to improve the temperature performance.

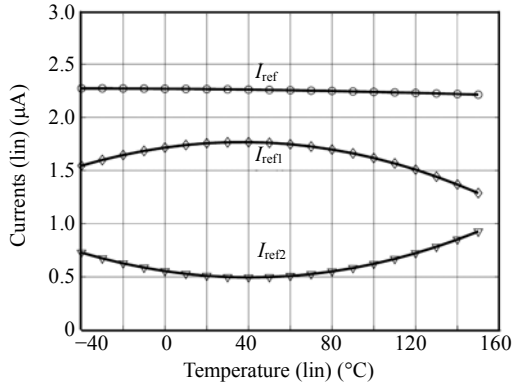

Fig.3 Temperature dependence characteristic of I_{ref1}, I_{ref2} and I_{ref} at 1 V supply voltage

The output reference current as a function of the supply voltage at room temperature is shown in Fig.4. The proposed current reference operates properly with supply voltage higher than 0.65 V and starts up smoothly.

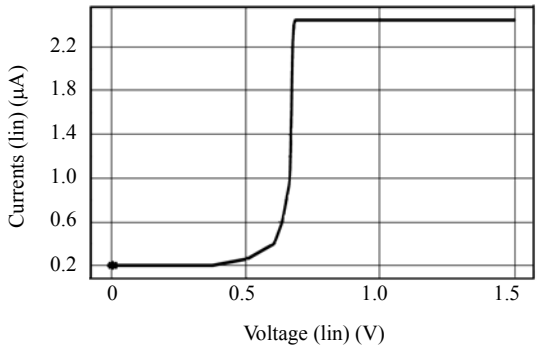

Fig.4 Output reference current as a function of the supply voltage at room temperature

The PSRR with and without bypass high frequency compensation capacitor at 1 V supply voltage is shown in Fig.5. The bypass compensation capacitor greatly improves the output current PSRR. It is about −78 dB at the frequency lower than 100 Hz and remains −40 dB at frequency higher than 10 MHz.

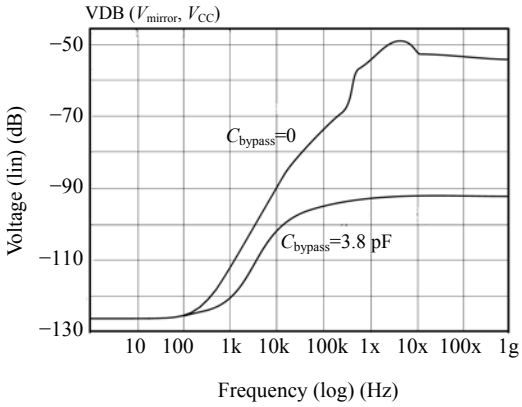

Fig.5 PSRR of the current reference with and without bypass compensation capacitor

Monte Carlo simulation with the poly sheet resistivity Gaussian distribution variation ±20% was carried out with the number of the Monte Carlo simulations being 30. The total variation of the current I_{ref} is shown in Fig.6. The maximal positive error is about +6.7%, and the maximal negative error is about −5.8%. The error can be cancelled by the trimming.

CONCLUSION

This paper describes a low-voltage high precision current reference based on subthreshold MOSFETs

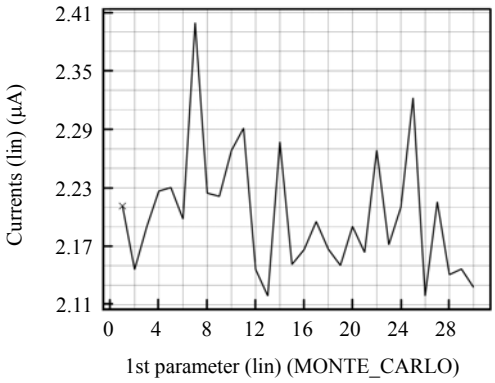

Fig.6 Monte Carlo simulation on the total variation of the current I_{ref} with the poly sheet resistivity Gaussian distribution variation ±20%

(instead of the base-emitter junction) with a novel temperature compensation topology structure to achieve a much low temperature coefficient of 3×10^{-4} μA/°C. The novel approach is to combine properly a scaled curvature-down current and a scaled curvature-up current. The output reference current is 2.25±0.02 μA at temperature range of −40~150 °C with 1 V supply voltage. The bypass high frequency compensation capacitor is used properly to enhance the reference PSRR. The PSRR remains −40 dB with the bypass capacitor for the frequency higher than 10 MHz. The low-voltage Op-AMP is designed with nMOS differential pair configuration to overcome the problem that the conventional pMOS differential pair Op-AMP must be stable above 1.5 V supply voltage. The proposed reference current circuit can operate well at supply voltage higher than 0.65 V. Moreover, the circuit is designed by the pure CMOS logic process technology and the maximal process error is about 6.7% based on the Monte Carlo simulation. So it has good process compatibility.

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