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Design and metrological applications of a low noise, high electrical isolation measurement unit

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Abstract: A digitally controlled voltage generation and measurement unit optimised for high-precision electrical metrology is described. It is optically isolated from the controlling computer and contains specially constructed isolated power supplies allowing continuous operation without the need to recharge batteries. The source has a simple microcontroller that is pre-programmed with firmware to control operation and to carry out simple repetitive measurement tasks, such as generation and quantisation of signals using uniform sampling. The merits of the developed unit are demonstrated by three example applications: (i) the application of the unit to control a Josephson voltage standard, (ii) the implementation of a transfer standard for the calibration of the electronic instrumentation of fatigue testing machines traceable to the primary electrical standards and (iii) the force measurement of an ion thruster traceable to the primary electrical standards at the industrial user level.

1 Introduction

Successful exploitation of the Josephson effect in superconductors and the quantised Hall effect in semiconductors as electrical primary standards of voltage and resistance [1] demands measurement systems with very good electrical isolation as well as low noise and high stability. Since 1990, these quantum electrical standards, by virtue of internationally agreed values of the Josephson and von Klitzing constants [2], have been established as the top level maintained SI representations of the volt and the ohm in many national standards laboratories. Thus, routine measurements of these two effects need to be made, so the availability of automated measurement systems capable of long periods of operation is desirable. Indeed, at the National Physical Laboratory (NPL), all measurements of voltage standards for industrial customers are now carried out directly against the UK primary standard of voltage based on the Josephson effect.

This paper describes a precision voltage generation and measurement unit that is digitally controlled and electrically isolated from both the controlling computer and the mains-power supply. To the authors' knowledge, it achieves a higher level of electrical isolation than any commercially available data acquisition system, having an injected common-mode alternating current (AC) over a hundred times smaller than the best digital voltmeters. To quantify this, a measurement of the common-mode AC from a mains powered digital voltmeter input, using an 1 MΩ oscilloscope, typically shows voltage levels of 50 mV and above, mostly at power line frequencies, corresponding to a current of at least 50 nA. The system described here has an injected AC below 0.5 nA and has been designed for use in high-precision electrical

metrology applications where leakage currents, AC or direct current (DC), of <1 nA and isolation resistances of >10 GΩ are required. As will be illustrated in the applications section of this paper, such leakage currents can flow along paths in measurement circuits with the result that the operation of sensitive devices is disturbed and incorrect results obtained as a result of extra currents and voltages in measurement networks. The unit has become the essential component of several measurement systems for electrical quantum standards at NPL and has also found other applications in high accuracy electrical metrology. A number of units have also been supplied to other national measurement institutes for use in applications where the isolation of commercial data acquisition systems has been found to be inadequate.

The isolated measurement unit consists of (i) a main board, containing the digital control system, optical interface and analogue to digital converters (ADCs), digital to analogue converters (DACs) and a precision voltage reference, (ii) two high isolation DC–DC converters, one for digital logic power and one for analogue power and (iii) an application board that is chosen according to the intended use for the unit. In this paper, the unit is described in detail together with its use in three applications: (i) DC voltage measurements at the national standards laboratory level, (ii) the calibration of the electronic instrumentation used for the characterisation of fatigue testing machines at the measurement standards laboratory level and (iii) the force measurement of an ion thruster as an industrial application are given.

2 Main board

A block diagram of the main board is shown in Fig. 1. The board is physically divided into two separate areas, one for digital electronics and one for analogue circuits. A four-layer printed circuit board is used so that both analogue and digital ground planes can be employed in addition to the connection tracks. The analogue and digital circuits have separate lidded screening cans mounted on the component side of the board and the ground planes provide screening on the solder side of the board.

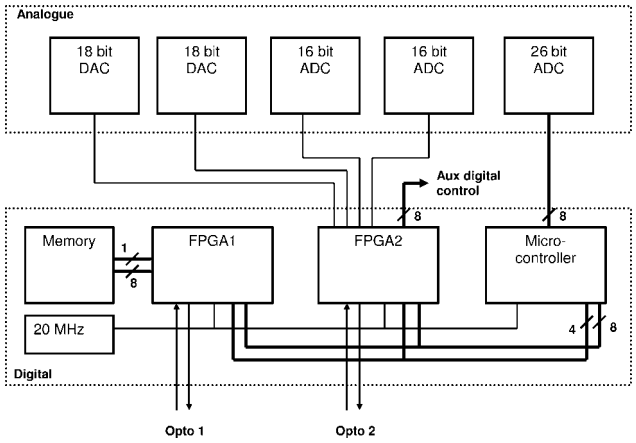

Figure 1 *Block diagram of main digital control board*

The digital electronics consists of an 8-bit microcontroller employing RISC architecture, two field programmable gate arrays (FPGAs), a 512 KB memory device and a 20 MHz oscillator which provides the master clock for the unit. The two FPGAs and the microcontroller communicate with each other through an 8-bit data bus and 4-bit address bus. FPGA1 is responsible for bus and memory control, and FPGA2 provides the interface to the DACs and ADCs as well as a simple 8-bit digital interface for controlling functions on the application board. In addition, each FPGA provides a serial optically isolated interface to external devices that can be a controlling computer or more boards of the same design. This serial interface, in which devices are connected in a ring configuration with a single controller and one or more 'outstations', is based on an original design [3] that has been updated here to be compatible with National Instruments LabVIEW® and a National Instruments digital data acquisition card. Device FPGA1 is configured to perform the outstation function only, whereas device FPGA2 can be either an outstation or a controller so that a set of boards can be configured communicate with each other without the services of an external computer. The microcontroller is pre-loaded with firmware so the unit is always ready to operate as soon as power is supplied. The firmware is stored in an EEPROM built in the microcontroller so that the microcontroller can easily be reprogrammed for the application of interest if it is required.

The firmware consists of a basic service loop that inspects the two FPGAs for data packets arriving over either optical ring interface. A total of 38 different operations or instructions are provided, which include writing to the DACs, reading from the ADCs and setting various parameters. The microcontroller can also carry out a number of operations such as programming a voltage sequence from data stored in memory to the DACs, taking regular ADC readings and storing them in the memory and running a simple servo control loop. The firmware is designed so that the microcontroller carries out all actions with a basic cycle time of 0.8192 ms corresponding to a maximum sampling frequency of 1.2207 kHz. The data memory is organised as eight 64 KB pages so that different pages can be used for different data tables. The address pointer wraps around within each page so that there is no danger of writing to one page corrupting another.

The analogue electronics comprises (i) two 16/18 bit DACs, (ii) two 16-bit ADCs, (iii) a 26-bit ADC and (iv) a precision voltage reference. All are standard commercial devices. The (i) DACs and (ii) ADCs have an in-built calibration function that ensures they are linear to the least significant bit. The DACs can be operated in either a 16 bit or 18 bit mode but in both cases, the accuracy of the output is 18 bits. The 26-bit ADC is a hybrid device and can be operated with a range of

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integration times ranging from 3 ms to 3 s with a corresponding resolution of 16–26 bits. The precision 10 V reference has a temperature coefficient of <2 ppm/°C and is used to provide a reference to all the DACs and ADCs with the exception of the 26-bit ADC, which has its own internal reference. In addition, the unit can be configured so that the DACs and the ADCs can take an external reference for applications where ratiometric measurements are required.

3 Isolated DC–DC converters

The isolated DC–DC converter (ISOP) was designed specifically for measurement applications where excellent electrical isolation of circuits is essential. Prior methods include the use of replaceable or rechargeable batteries, guarded line frequency transformers which are bulky and often have a high unguarded capacitance, or specially constructed toroidal double-screened transformers [4]. The ISOP gets close to the capacitance, isolation and noise performance of batteries without the inconvenience of having to interrupt experiments to recharge or refit battery cells or having experiments fail as batteries run low. Its compact design also lends itself to small scale production. In measurement instrumentation, the main problem experienced with conventional power supplies is that significant alternating current is injected into the measurement circuit from the transformer through coupling capacitances between windings or between windings and the safety screen if present. Furthermore, with the move to the higher frequencies now commonly used in modern switching designs, the AC coupled through the supply can reach the milliampere level, a magnitude quite common in commercial DC–DC converters. The ISOP achieves its performance through three major design advances of equal importance to the success of the supply.

First, the isolation transformer utilises near perfect Faraday screens placed independently around the primary and secondary windings on two toroidal cores as illustrated in Fig. 2. This is achieved through the use of conductive injection moulded plastic screens of high enough resistivity

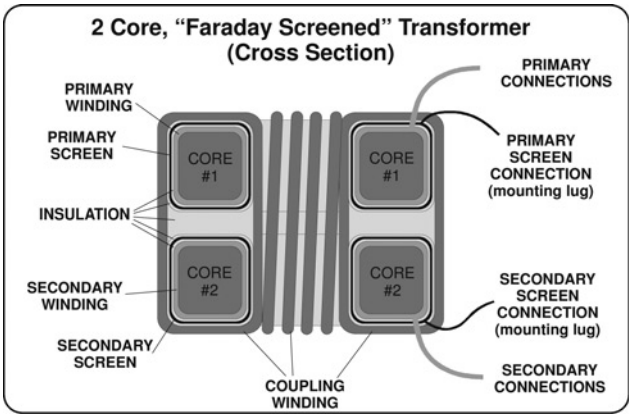

Figure 2 *Construction of screened transformer*

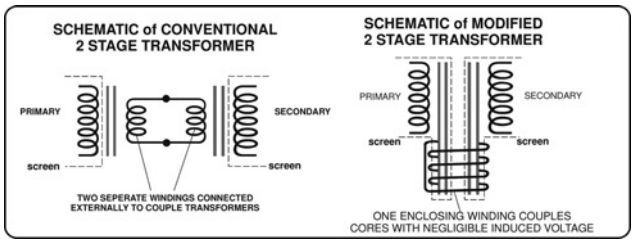

Figure 3 *Explanation of how windings are coupled*

to prevent a shorted turn of significant load but low enough to screen efficiently. The magnetic coupling of the isolated and individually screened primary and secondary is then made possible by a shorted turn, polytetraflurorethane (PTFE) sheathed, coupling winding arrangement around both wound cores, the shorted turn giving virtually zero potential in its winding (actually a series of $\pm 1/4$ turn potentials), but magnetically coupling the cores to better than 99.7%. The operation of this coupling winding is illustrated in Fig. 3.

Secondly, the drive and load waveforms implemented are slew controlled to prevent very fast edges and are made as symmetrical as possible so that within the primary screen, for example, positive and negative going edges are fully balanced differentially. Thirdly, the use of high permeability, high saturation density, 'nano crystalline' cores allows relatively low-frequency operation, ~7 kHz, which enables reasonably high power density compared with 50/60 Hz and further allows more aggressive slew rate limiting.

The isolation performance of an example converter was tested by measuring the leakage current using an oscilloscope fitted with a $\times 10$ probe to provide a high input impedance of 10 MΩ in parallel with ~10 pF. The resulting trace is shown in Fig. 4. The signal has a period of 170 μs corresponding to the drive oscillator frequency of 6 kHz. The peak-to-peak amplitude is ~500 μV that corresponds to a current of 200 pA peak-to-peak taking the impedance of the probe to be 2.7 MΩ at 6 kHz. In addition, the capacitance measured from screened winding to alternate screen is 0.02 pF and the input to output

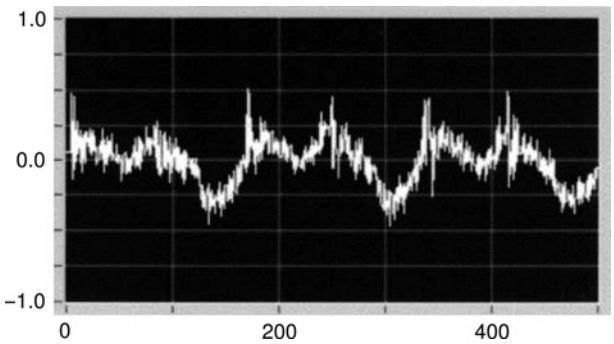

Figure 4 *Time domain representation of the leakage current measured using an oscilloscope probe (y axis in mV and x axis in μs)*

leakage impedance is >10 GΩ in parallel with a capacitance of <22 pF. The ISOP units are commercially available in small quantities and are of two design types: 12 V nominal input (11–15 V), 15 W and 24 V nominal input (23–28 V), 25 W. In both cases, two output voltage options are available: ±15 V and ±6.3 V with a typical conversion efficiency of 65–70%.

4 Application boards

4.1 Current source

Most DC measurements employ a periodic reversal of the voltage or current being measured to remove the static value, drift and low-frequency components of various offsets arising from input bias currents, input offset voltages and thermal emfs. In particular, precision resistance ratio measurements with DC are almost always conducted with a current reversal as this conveniently removes unwanted offsets while maintaining a constant power dissipation in the resistors being measured.

In some measurement systems, current sources are employed to energise the measurement circuit and each particular application imposes specific technical requirements for the source. One of the most demanding applications is the cryogenic current comparator (CCC) resistance ratio bridge [5], where it is important to have one or more current sources, which can be smoothly reversed through zero current without any discontinuities, for energising the resistors under test. To meet this requirement, a low noise voltage to current converter described here was designed that is able to deliver a bipolar current into a load connected on one side to the 0 V supply of the source. Although various operational amplifier circuits in principle achieve this, the load is actually part of the feedback network of the amplifier so non-ideal loads can lead to circuit instabilities. In the circuit presented here, the circuit feedback is independent of the load resistor so a wide range of load impedances can be tolerated and at the same time, a high output impedance from the source is maintained.

Fig. 5 illustrates the basic principle of the developed voltage to current converter. The circuit consists of two independent current sources whose currents are combined at the output terminal. The output current of each source is determined by the voltage across the current control resistors R_{10} and R_{11} so is directly dependent on the power supply voltages. This would lead to unacceptable drift unless the supply rails were highly stabilised. However, this problem can be completely avoided by linking the two sources by the input bias divider R_1 to R_4 and connecting the voltage input through resistor R_5. It can be shown that a value of R_5 exists such that the output of the complete source is independent of either supply voltage. With the simplifying assumptions that $R_1 = R_3$, $R_2 = R_4$ and so on for corresponding pairs of resistors in the two halves of the

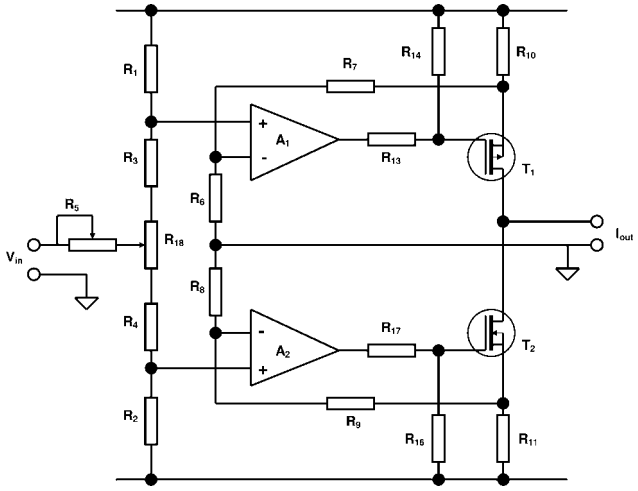

Figure 5 *Schematic diagram of voltage to current converter*

circuit, this value is given by

$$R_5 = \frac{R_1 - (G-1)(R_3 + (R_{18}/2))}{2(G-1)} \quad \text{where} \quad G = \frac{R_6 + R_7}{R_6} \tag{1}$$

Note that this result does not depend on the current control resistors R_{10} and R_{11}. The transconductance is given by

$$\frac{I_{\text{out}}}{V_{\text{in}}} = -\frac{2(G-1)}{R} \tag{2}$$

where

$$\frac{1}{R} = \frac{1}{R_{10}} + \frac{1}{(R_6 + R_7)}$$

so different values can simply be obtained by switching pairs of resistors at R_{10} and R_{11}. The compensation effect can be understood intuitively by considering the quiescent currents flowing in the output stages. The circuit operates in Class A mode so that at zero output current, the two stages carry equal and opposite currents with a magnitude slightly larger than half the maximum output of the source. If, for example, the positive power supply voltage is increased, then the quiescent current of the top half of the circuit increases. The input divider ensures that this increase is exactly compensated by an identical increase in the quiescent current of the lower stage so that the output current remains at zero. The output current noise of the circuit is a combination of operational amplifier noise and Johnson noise in the circuit resistors. Most resistors can be low in value, of the order of a few kΩ but the feedback resistors R_7 and R_9 have to be typically ten times the largest value chosen for R_{10} and R_{11}. The output noise scales directly with the values of R_{10} and R_{11} so for this reason and to make best use of the DAC providing the

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input voltage, it is desirable to have a number of output current ranges.

Most precision DC resistance standards are in decade values (e.g. 1, 10, 100 Ω) and are normally measured at the same nominal power, typically 1 mW. It is therefore convenient to have a current source with full scale outputs that scale as $\sqrt{10}$, such as 30, 10 and 3 mA, so that an optimum range can be chosen for a given standard resistor value. For the latest design of CCC bridge at NPL that covers the resistance range 1 Ω to 10 kΩ, a current source circuit board has been designed with a total of six output ranges with full scale values from 0.1 to 30 mA. A typical value for the gain, G (1), is 1.25 and with this value, the ratio $R_3 = 2R_1$ gives good DC bias conditions. With these values, the transconductance (2) is $0.5/R$ so that a ± 1 mA output for a ± 10 V input is achieved with $R = 2.5$ kΩ.

The sensitivity of the CCC, which is used to detect deviation of the current ratio in the resistance bridge from the required ratio, sets the specification for the current source. The main constraint is that the flux detector attached to a CCC, known as a superconducting quantum interference device (SQUID), has a periodic output response to input flux, normally denoted ϕ_0. For correct operation of a resistance bridge based on a CCC, the flux imbalance (both static value and peak-to-peak noise) in the CCC has to be kept below one ϕ_0. For a typical CCC used in the most recent design of resistance bridges at NPL [6], the CCC sensitivity is such that 20 μA in a single turn corresponds to one ϕ_0 in the SQUID. The current linkage in the CCC (for example, 2000 turns for the 100 μA measurement current range) is of the order of 200 mA·turns. Thus, one ϕ_0 corresponds to 10^{-4} of the full-scale current. The linearity and peak-to-peak noise (in the bandwidth seen by the CCC) of the current source ranges therefore need to be better than 50 ppm of the full scale.

To avoid any problems with contact noise and reliability, current range switching is achieved using field effect transistors (FET) rather than relays. However, the channel resistance of an FET when biased to be conducting can still be significant in relation to the value of the current setting resistors for the higher current ranges. This can lead to gain errors and non-linearity in the current output. A two-wire connection is therefore made for the range resistors relating to the three highest current ranges to give separate current and voltage connections as illustrated in Fig. 6. An additional problem is created by the capacitance across the FETs when they are biased to a non-conducting state. This has the largest effect on the lowest current ranges where the de-selected resistors all appear in parallel with the selected resistor through the capacitance of the switching FETs. This causes an undesirable increase in the voltage-to-current transfer function at higher frequencies. To reduce the effect of this stray capacitance to an acceptable level, two FETs are used in switch locations

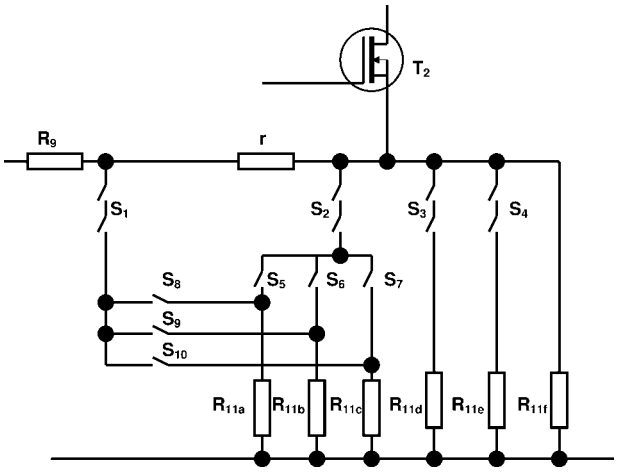

Figure 6 *Detail of current source range switching*

S_1–S_4 and the central source-drain connection and gate connections are driven with an AC-coupled guard signal.

In operation, the input voltage is supplied by the two DACs on the main board, their outputs combined in a summing amplifier so as to provide coarse and fine control of the generated current. The output current from the source is sensed with a 50 Ω resistor and the voltage developed across this resistor is scaled with a programmable gain amplifier (PGA) and then digitised using one of the ADCs on the main board to provide a current monitor. The linearity of all ranges is typically better than 20 ppm of full scale which is about a factor of two worse than the 18-bit DAC integral linearity of 10 ppm of full scale. Although the current source has been developed primarily for DC measurements, it has been designed to have a bandwidth of 100 kHz so as to obtain a good closed loop performance in feedback circuits. It therefore also has application in AC metrology. The accuracy of the output current clearly depends on component values used in the circuit but these errors can easily be corrected by maintaining calibration constants in the computer software which calculates the DAC values. The use of high-stability components ensures that these correction values only need occasional updating.

4.2 Totem-pole filter

The effective use of ADCs to acquire an analogue signal and DACs to generate an analogue signal requires the signals to be bandlimited. This is normally achieved using a low pass filter. Usually, the filter used to bandlimit the signal applied to an ADC is called an anti-aliasing filter and the purpose of such a filter is to attenuate signal frequencies above half the sampling frequency. The filter used after a DAC is usually called an anti-imaging filter and is used to attenuate harmonics of the generated waveform due to the step-wise approximation of the DAC. Many designs of such filters exist and component values can be chosen to give particular frequency response characteristics such as Butterworth or

Bessel [7, 8]. It is important to note that the frequency response of the filter is crucial to the performance of the measurement system and a discussion on choosing an appropriate filter for a given application can be found elsewhere [9].

The filter presented here, shown schematically in Fig. 7, has been optimised for low-frequency electrical metrology with the particular advantage that the main signal path does not include any operational amplifiers. This has the benefit that the noise and drift associated with these devices does not degrade the filtered signal in the passband. The term 'totem-pole' has been chosen to reflect how the filter consists of multiple stages stacked one upon another. Fig. 7 shows just one element but the design is general and can be extended to many stages using a recursive formula. Each stage consists of an operational amplifier with two resistors and two capacitors as indicated by the components within the dashed box. As will be shown, it is the *conductance* of this circuit element which is important and the conductance of all subsequent stages together is indicated by the component G_{n-1}. The overall attenuation of the filter is given by the simple expression

$$\frac{V_n}{V_s} = \frac{1}{1 + G_n R_0}$$

where G_n is the conductance at the output node to analogue ground given by $I_A + I_B = G_n V_n$. A full circuit analysis, which includes the operational amplifier characteristics, is complex but an effective insight into the operation of the circuit can be gained by considering the amplifier to be 'ideal' with infinite gain, infinite input impedance and zero output impedance. The inverting input then becomes a 'virtual earth' so that voltage V_A can be considered to be zero. This defines I_A:

$$I_A = sC_n V_n = \frac{-V_{n-1}}{R_n} \quad \text{and so} \quad V_{n-1} = -sC_n R_n V_n$$

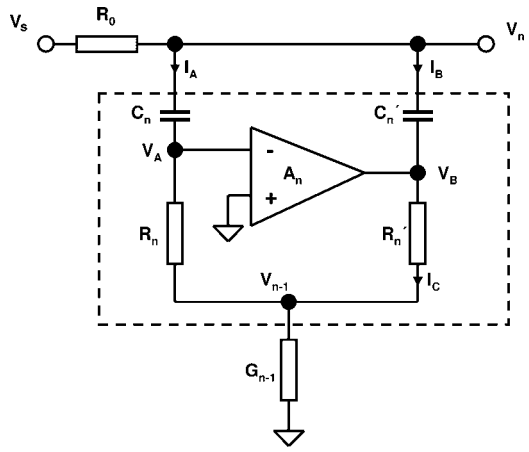

Figure 7 *Totem-pole filter showing basic building block (within the dashed line)*

However, it is still necessary to know the current into the next segment to define V_{n-1}. Summing currents flowing in R_n, R_n' and G_{n-1} gives

$$\frac{V_{n-1}}{R_n} + \frac{V_{n-1} - V_B}{R_n'} + G_{n-1} V_{n-1} = 0$$

thus

$$V_B = \frac{V_{n-1}(R_n + R_n' + G_{n-1} R_n R_n')}{R_n}$$
$$= -sC_n(R_n + R_n' + G_{n-1} R_n R_n') V_n$$

and the total current entering at the top of the totem-pole stack is

$$I_A + I_B = sC_n V_n + sC_n'(V_n - V_B) = (sC_n + sC_n'(1 + sC_n \times (R_n + R_n' + G_{n-1} R_n R_n')))V_n = G_n V_n$$

Using this expression for G_n, the filter transfer function can finally be deduced:

$$\frac{V_n}{V_s} = \frac{1}{1 + sR_0(C_n + C_n') + s^2 C_n C_n' R_0 \times (R_n + R_n' + G_{n-1} R_n R_n')}$$

Note that the expression is completely symmetrical to the exchange of the resistors or capacitors in a given block and that the formula is recursive. Table 1 lists the terms for a five-pole filter together with the corresponding coefficients to three decimal places for a Butterworth or Bessel response function. For low pass applications, the Butterworth is well known for its frequency flatness and lack of passband ripple but the Bessel gives a much better settling time for a given stopband rejection. The final stage in the five-pole filter is just a capacitor, represented here by two capacitors C_{n-2} and C_{n-2}' to preserve the symmetry of the series. There are more unknowns in the filter components than equations so the capacitors in each block can be chosen to be equal and the same value throughout such that $C_n = C_n' = C_0$ etc. This allows a simple algebraic solution of the equations and is also convenient as resistors can generally be obtained with a greater range of values than capacitors. The substitutions

$$\tau_1 = R_0 C_0, \quad \tau_2 = R_n C_0, \quad \tau_3 = R_n' C_0,$$
$$\tau_4 = R_{n-1} C_0, \quad \tau_5 = R_{n-1}' C_0$$

and expressions for the polynomial coefficients, $\alpha_1 - \alpha_5$, given in Table 1 lead to the following solution:

$$\tau_1 \omega_0 = \frac{\alpha_1}{2} \quad (\tau_2, \tau_3)\omega_0 = \frac{\alpha_2}{\alpha_1}\left[1 \pm \sqrt{1 - \frac{\alpha_1 \alpha_3}{\alpha_2^2}}\right]$$

$$(\tau_4, \tau_5)\omega_0 = \frac{\alpha_4}{\alpha_3}\left[1 \pm \sqrt{1 - \frac{\alpha_3 \alpha_5}{\alpha_4^2}}\right]$$

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Table 1 Polynomial coefficients α_i and constants for Butterworth and Bessel response functions

Power	Coefficient	Butterworth coefficient/ω_0	Bessel coefficient/ω_0	Expressions for α_i in terms of τ_i
s^0	—	1.000	1	
s^1	$\alpha_1 = (C_n + C_n{}') R_0$	3.236	1	$2\tau_1$
s^2	$\alpha_2 = C_n C_n{}' (R_n + R_n{}')R_0$	5.236	420/945	$\tau_1(\tau_2 + \tau_3)$
s^3	$\alpha_3 = (C_{n-1} + C_{n-1}{}') C_n C_n{}' R_n R_n{}' R_0$	5.236	105/945	$2\tau_1\tau_2\tau_3$
s^4	$\alpha_4 = C_n C_n{}' R_n R_n{}' C_{n-1} C_{n-1}{}' (R_{n-1} + R_{n-1}{}') R_0$	3.236	15/945	$\tau_1\tau_2\tau_3(\tau_4 + \tau_5)$
s^5	$\alpha_5 = (C_{n-2} + C_{n-2}{}') C_n C_n{}' R_n R_n{}' C_{n-1} C_{n-1}{}' R_{n-1} R_{n-1}{}' R_0$	1.000	1/945	$\tau_1\tau_2\tau_3\tau_4\tau_5$

Also given are expressions for α_i in terms of τ_i

where ω_0 sets the frequency response of the filter (in the case of a Butterworth filter, the −3 dB point) and the pairs of time constants such as τ_2, τ_3 are obtained from the positive and negative roots using the values for α_i in Table 1. Constants for fifth order Butterworth [7, 8] and Bessel [10] filters calculated using the above expressions are given in Table 2 and a drawing of the complete circuit for this case with component values normalised to $\omega_0 = C_0 = 1$ is given in Fig. 8.

The performance of the filter depends on the accuracy of the components. Typical factors to consider are the flatness of the passband, the accuracy of the −3 dB frequency and the attenuation of the stop band. The effect of component tolerances can easily be simulated using the circuit equations above and the important tolerances will depend on which filter aspects are of most importance to the user. However, as a general guide, for the Butterworth implementation of this design, a 10% variation in individual resistor and capacitor component values gives up to a 10% change in the stop band attenuation and −3 dB frequency plus a deviation in the passband gain of up to 10% in the final decade before the −3 dB point. It is worth noting that changes in the values of capacitors C and C' in a given segment have approximately equal and opposite effect. When assembling a circuit, therefore if a given capacitor is known to be above nominal, then it should be matched with one below nominal in the same filter stage to minimise the effect on the response function.

Table 2 Numerical values for timeconstants in terms of ω_0 for the Butterworth and Bessel response functions

Term	Butterworth	Bessel
$\tau_1\omega_0$	1.618	0.500
$\tau_2\omega_0$	2.618	0.738
$\tau_3\omega_0$	0.618	0.150
$\tau_4\omega_0$	1.055	0.247
$\tau_5\omega_0$	0.181	0.039

The above analysis assumes that the filter is driven from a low impedance and that the output is connected to a high impedance load. However, non-ideal impedances can be accommodated by simple corrections. For example, if the output is connected to a resistive load, R_L, then in the passband $V_n/V_s = R_L/(R_0 + R_L)$ and for calculating the −3 dB frequency, R_0 becomes the parallel combination of R_0 and R_L.

5 Example systems

To illustrate the use of the isolated voltage generation and measurement unit, three applications are described ranging from the application of the unit to control a Josephson voltage standard, a transfer standard for the calibration of the electronic instrumentation used in the calibration of fatigue testing machines at the calibration laboratory level and finally the measurement of force of an ion thrusters engine at the industrial user level.

5.1 Josephson bias unit

Top level voltage standards based on Zener reference diodes and Weston cells are now routinely calibrated by national laboratories against the voltage generated by an array of Josephson junctions [11]. To obtain the required voltage, the array of junctions needs to be biased by an adjustable low noise voltage source. Initially, battery powered, manually operated sources were used but these have been superseded by automated ones [12]. At NPL, all voltage reference standards submitted for calibration are measured directly against an array of junctions using an automated system. The majority of these have a mains power supply and it is more convenient to be able to measure the standards with continuous external power rather than rely on the internal battery power which might only last for a few hours. Although most standards have screened power transformers with some kind of guard screen, the residual

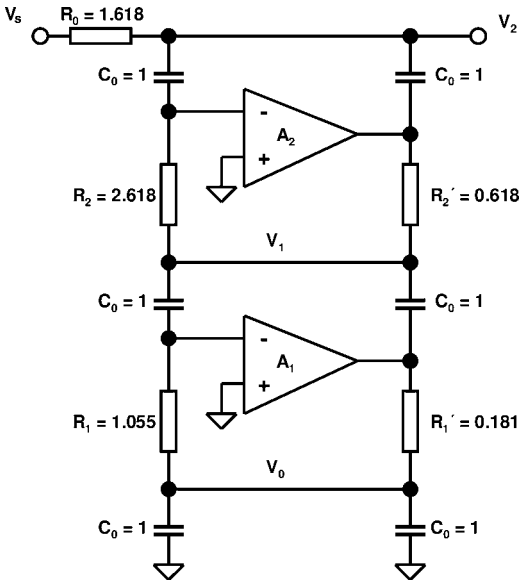

Figure 8 *Five-pole implementation of the filter design with component values for a Butterworth response*

mains frequency leakage current, up to 4 μA peak-to-peak, can cause instability in the Josephson array where the operating margins on the quantised voltage levels can be as low as a few microampere. To overcome this problem, the measurement circuit is connected to the measurement screen at the output terminals of the device under test (Fig. 9) and the single connection to mains earth is also made at this point. In this way, all leakage currents flowing through the transformer in the device under test are returned to their source and do not affect the array.

This connection scheme, however, places more stringent requirements on the array bias source because any leakage currents flowing through its power supply would now also flow in the measurement circuit. A low leakage bias system has therefore been produced, which combines the digital DAC/ADC board, isolated DC–DC converter and a Josephson junction array bias board to achieve the required specification. The two DACs are used to give coarse and fine control of the array bias voltage and one of the ADCs is used to monitor the array bias current and the other the array output voltage. Current–voltage curves are plotted using one of the repetitive sweep routines in the microcontroller. A four-wire connection to the array, as shown in Fig. 9, are used to sense the array voltage so that cable resistances are eliminated and the 26-bit ADC can be used to make array voltage measurements with a resolution of a few tens of microvolt in 10 V. For forward and reverse voltage measurements, a mechanical reversing switch is included in the circuit and a digital voltmetre (DVM) is used to measure the difference between the array and the voltage standard in both polarities. Note that the action of this reversing switch changes the position of the DVM in the circuit and therefore also the paths for leakage currents in the system. The leakage currents from the bias source are sufficiently low that they do not cause any difficulty in either switch position, making this measurement strategy possible. The requirements placed on the DVM in terms of common-mode rejection and leakage currents are stringent and this device gives rise to the dominant uncertainty component in the NPL system. The effect of leakage currents from the DVM on the array is minimised by connecting the 'Lo' terminal to the device under test since the DVM is asymmetrical and the currents generated at the 'Hi' terminal are generally lower than at the 'Lo' terminal.

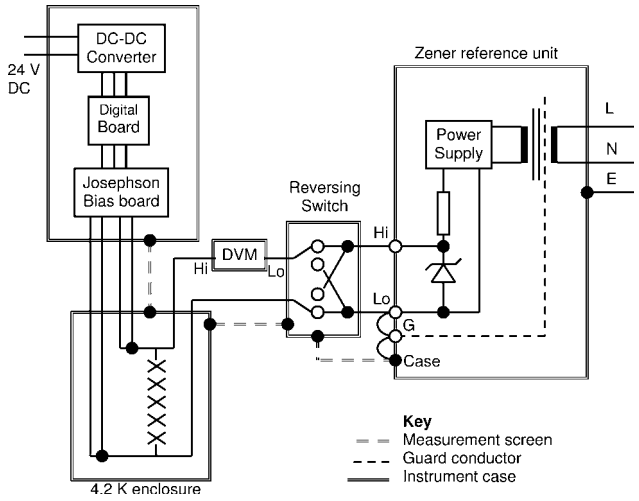

Figure 9 *Diagram of measurement system for Zener references against Josephson junction array*

5.2 Dynamic force standard

The measurement of dynamic forces using strain gauges and associated measurement electronics is set out in the British Standard BS 7935 [13]. Knowledge of the ability of the measurement electronics to measure the dynamic signals with sufficient accuracy is an important part of the traceability chain. To support this, a dynamic force standard was developed which simulates a strain gauge sensor, including

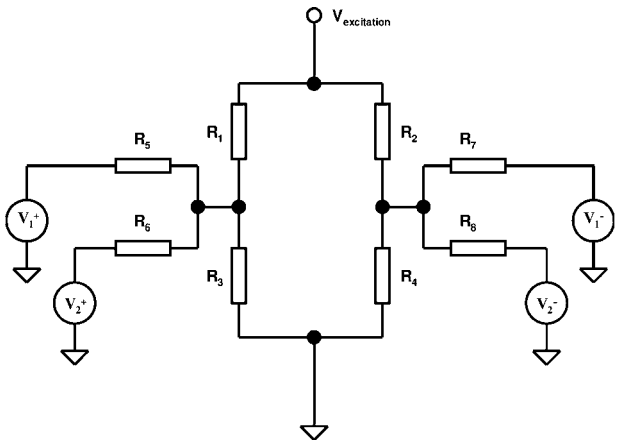

Figure 10 *Schematic of strain gauge simulator showing bridge components R_1 to R_4 and connection of drive signals via attenuator resistors R_5 to R_8*

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the dynamic changes, electrically. A schematic diagram of the sensor simulator is shown in Fig. 10.

The simulator is implemented by high stability metal film resistors with a low temperature coefficient. The two branches of the strain gauge emulator were matched to better than 0.05% of their nominal value. The low values of these resistors (e.g. 350 Ω) combined with the relatively high-voltage value of the bridge excitation (e.g. 10 V) imposes strict self-heating effect requirements. The network was designed to have temperature drift due to self-heating effects of better than 5 ppm/FS.

The two DACs on the main board produce one DC and one AC signal according to the requirements of BS 7935. At this stage, the AC signal is a staircase sinewave having high-order harmonics. The output of each DAC is passed through a PGA and a fifth order anti-imaging low-pass filter with Bessel frequency response using the totem-pole design. The filter removes the higher order harmonics of the AC staircase sinewave signal produced by the DAC. The output of the filter for each channel is applied to a bridge amplifier, which generates a differential output for connection to the strain gauge simulator (V_1^+, V_1^-, V_2^+, V_2^-, Fig. 10). The attenuator resistors are used to sum the DC and AC signals produced by the DAC and scale the output signals to the appropriate levels.

The excitation voltage of the strain gauge bridge (which is provided by the electronics unit under test) is used as reference voltage for the DACs so that the DFS operates in a ratiometric mode. This arrangement does not require long-term stability of the excitation voltage of the bridge which is provided by the measurement electronics. However, such an arrangement can introduce high common-mode signals so the isolated DC–DC converter is used to power the system to provide isolation from the screen of the electronics and a minimum common-mode interference current. Test waveforms as defined in BS 7935 are programmed into the memory on the main board. The accuracy of these waveforms was tested using precision AC measurement equipment and shown to be better than 0.1% for simulated strain gauge outputs in the range 10–40 mV and waveform frequencies in the range 17–100 Hz [14].

5.3 Current and voltage monitor for ion engine testing

Ion engines are used for positioning satellites in space and generate a small thrust using an accelerated beam of xenon ions. To support the development of a particular ion engine for the GOCE satellite, a special version of the measurement unit was developed to measure the current and voltage supplied to the engine during ground-based testing. Measurement of the current and voltage supplied to the engine gives a direct indication of the stability of the force generated through the relation

$$F = kI_B\sqrt{V_B}$$

where $k = 1.649\ \text{mN A}^{-1}\ \text{V}^{-1/2}$ for this particular design. The nominal operating voltage of the engine is 1176 V and the current is 0.4 A. The specification for the measurement unit was to be able to resolve a force of 0.001 mN/√Hz which translates into a current resolution of 17 μA/√Hz and voltage resolution of 0.1 V/√Hz. A further requirement was that the current be measured at the high terminal of the power supply to the engine. The necessary high voltage isolation was achieved using the DC–DC converter and optical fibre interface so that the measurement unit, consisting of a main board, two totem-pole filters for anti-aliasing and a transducer unit, was operating at the common-mode voltage of 1176 V. The transducer consisted of a 30 MΩ:18 kΩ divider for the voltage channel and a 0.25 Ω resistor followed by a ×10 amplifier for the current channel to give two nominal 1 V input signals to the filter stages.

To achieve the required voltage and current resolution at the operating point, the two DACs on the main board were used to offset the measured voltages and the difference voltages were further amplified by a PGA with ×1, ×10 and ×100 ranges. This technique works because the short-term noise from the DACs is much <1 least significant bit. Fig. 11 shows test data taken on the unit and the noise performance achieved was 0.001 V/√Hz and 1 μA/√Hz.

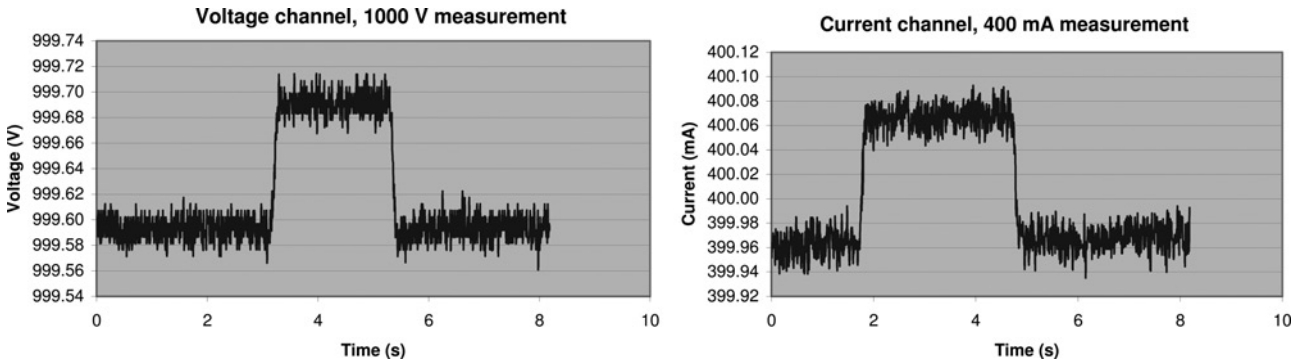

Figure 11 *Voltage and current channel test results showing a calibration step of 100 mV and 100 μA, respectively*

6 Conclusion

A design of precision voltage generation and measurement unit which is digitally controlled and electrically isolated from both the controlling computer and the mains power supply has been described. Through the use of specialised DC–DC converters and an optical fibre interface, the electrical isolation achieved is a hundred times better than is routinely obtained when using commercially available measurement equipment. The detailed design of two application boards to complement the main measurement board has also been presented. Three examples of the use of the measurement system in precision electrical metrology have been given which demonstrate the effective use of its versatility and electrical isolation.

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