HPM7177 – An Open Hardware Metrology-Grade Digitizer

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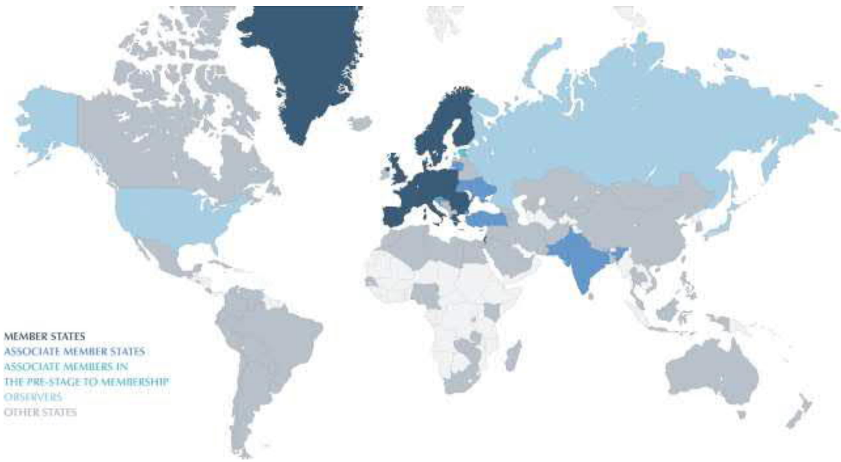
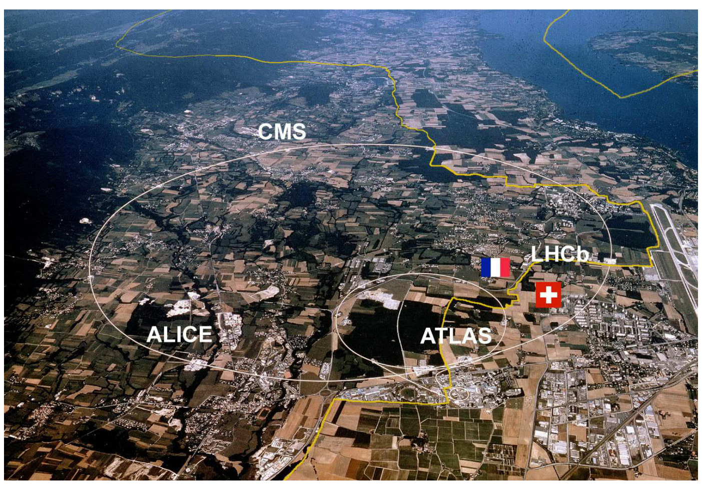
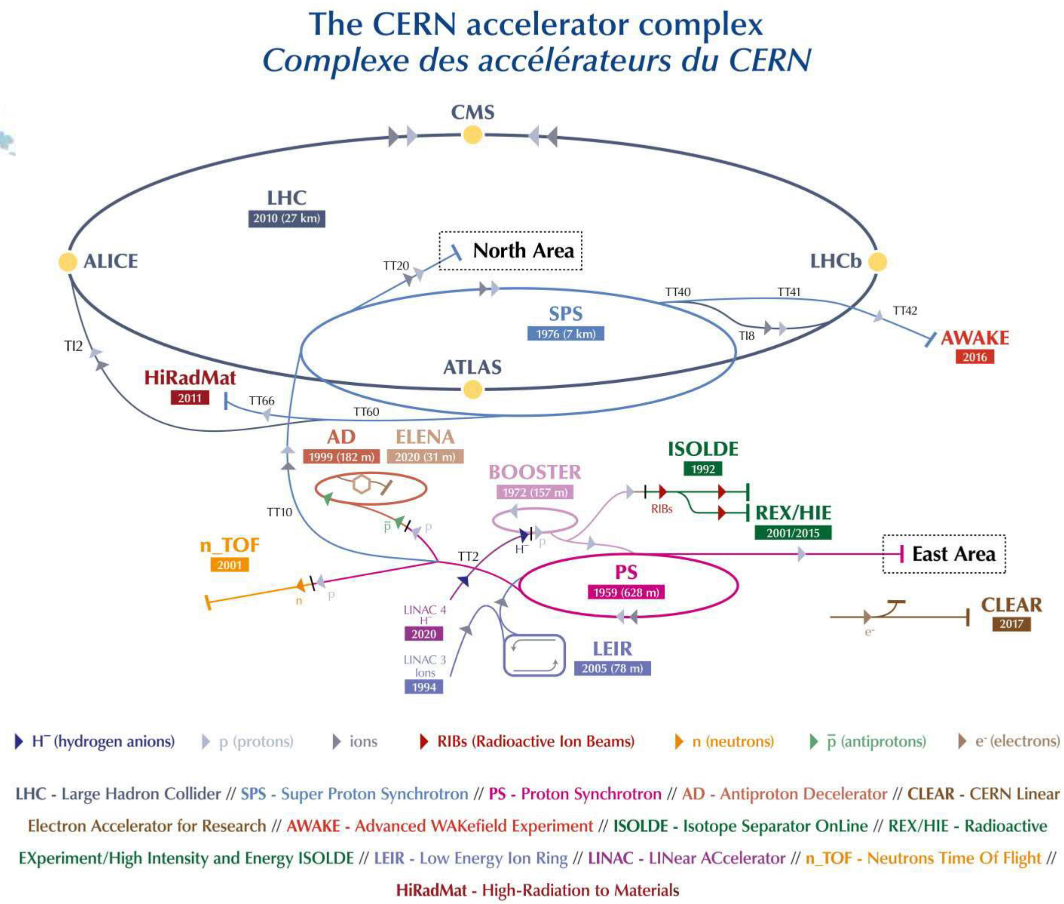
Presentation Outline

- Introduction
  - CERN, precision powering of magnets, HL-LHC, requirements, digitizers and more
- HPM7177
  - Starting points and evolution of prototypes
  - Present-day design
  - Testing and characterization
  - Next steps
- Excess noise in precision resistor networks

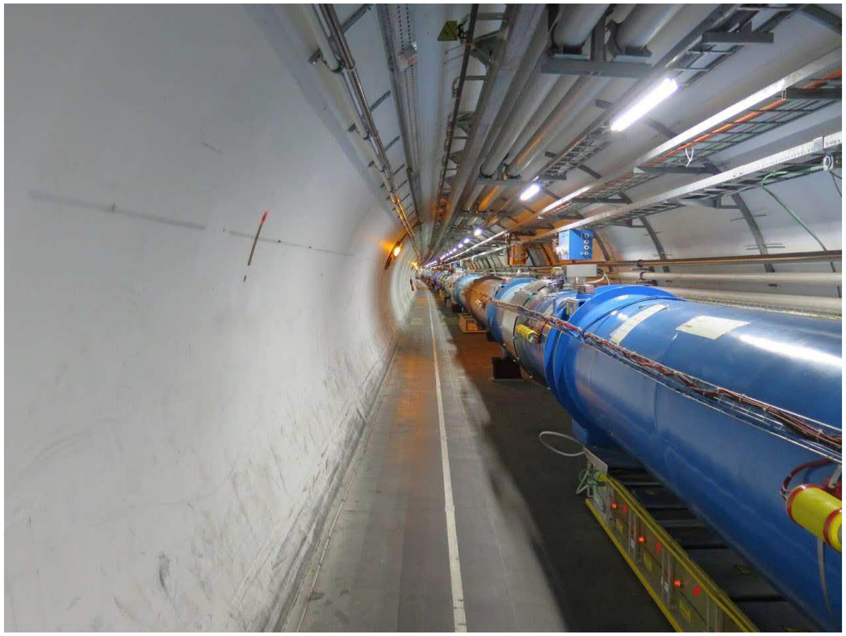
Introduction to CERN

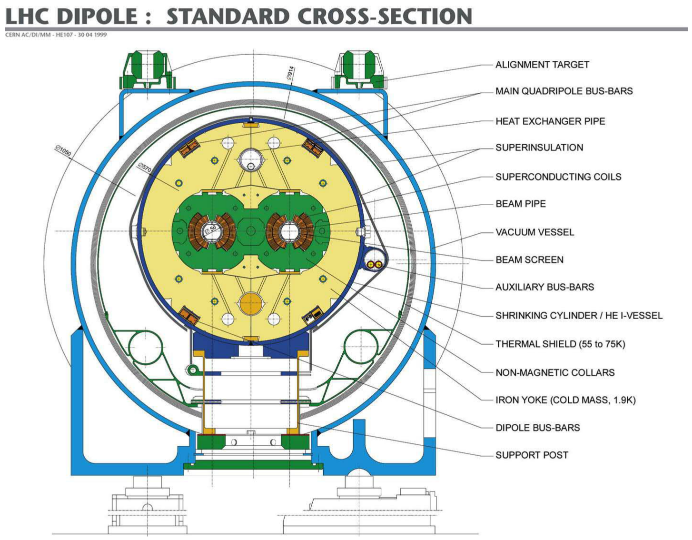






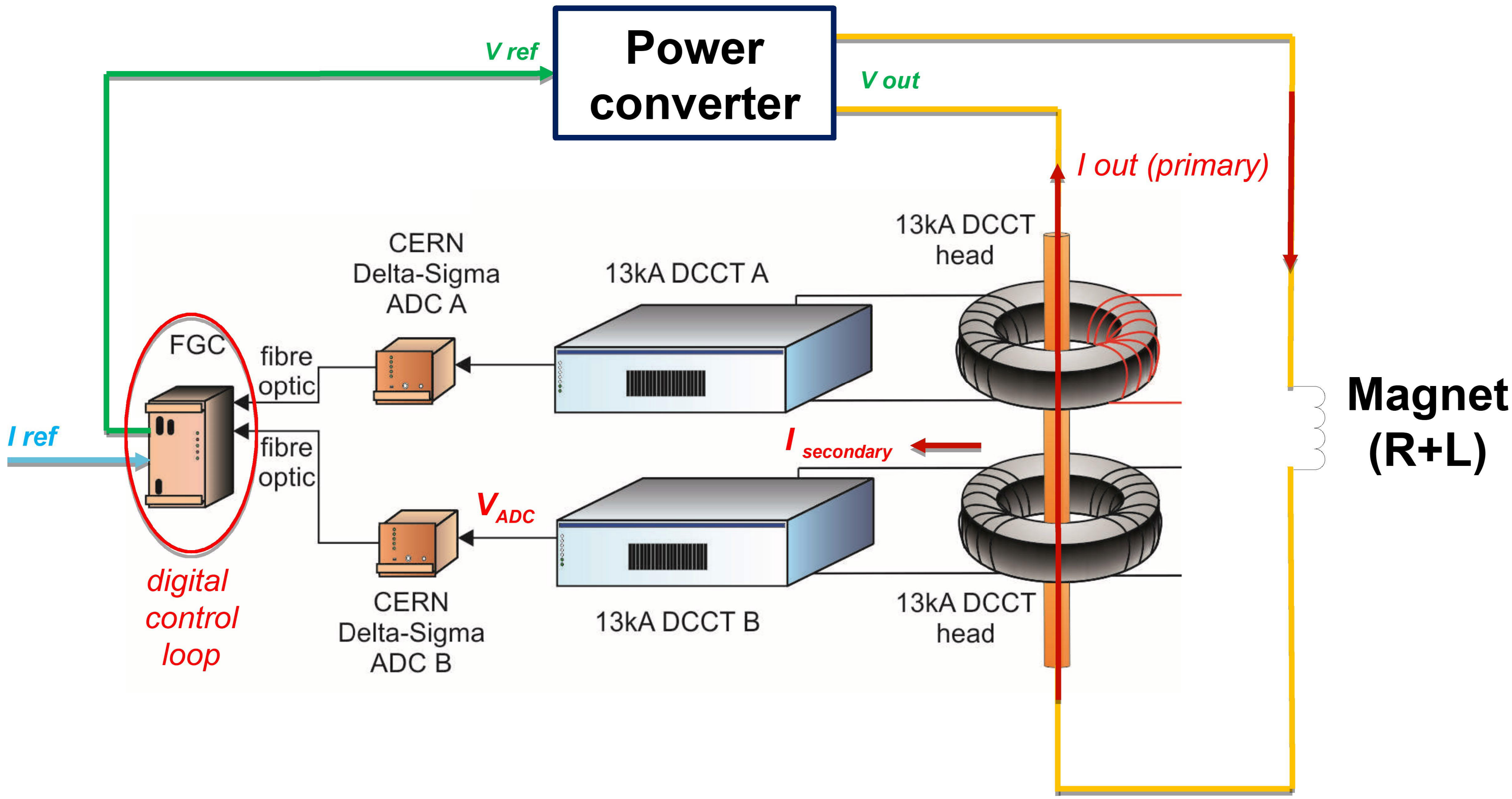
Power Converters and Magnets





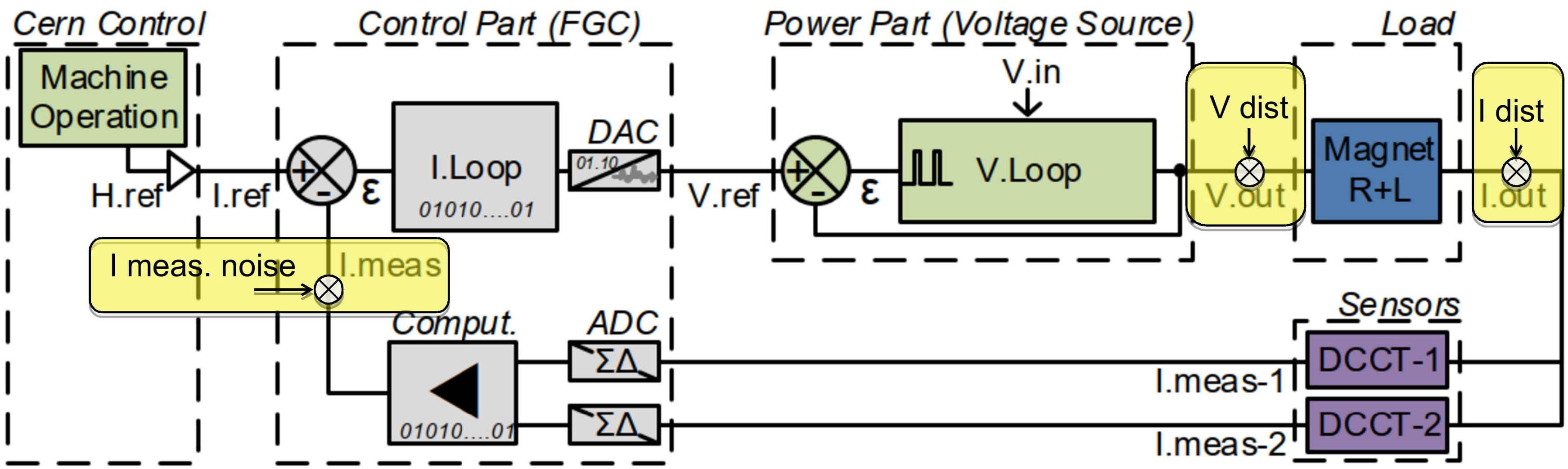
Electrical Power Converters Group
https://sy-dep.web.cern.ch/epc

High Precision Powering in LHC

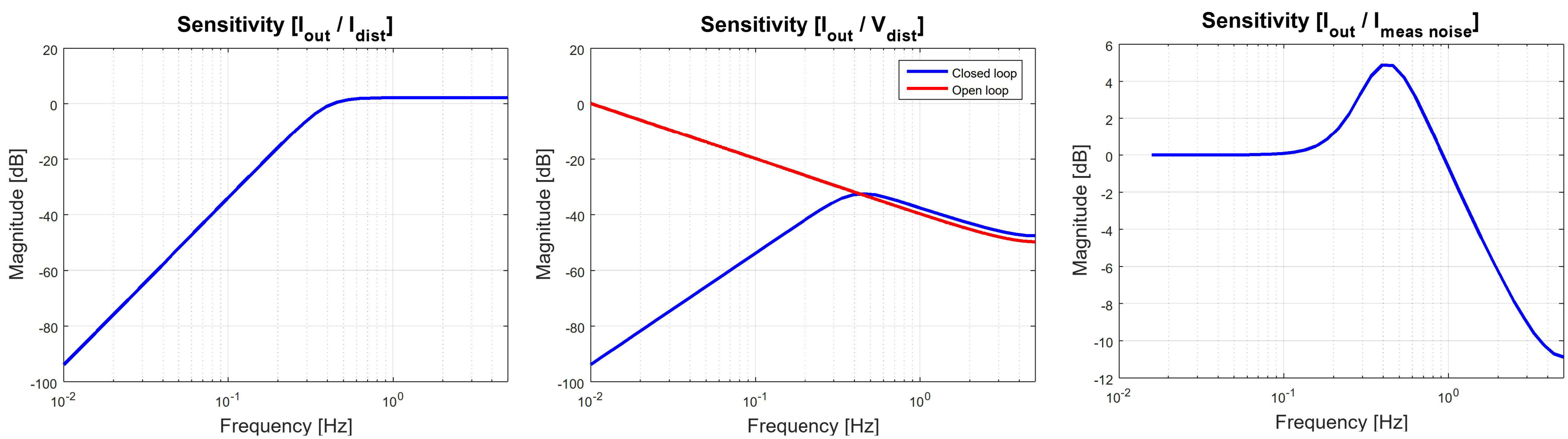


[1] M. C. Bastos *et al*. **High accuracy current measurement in the main power converters of the large hadron collider: tutorial 53**. *IEEE Instrumentation & Measurement Magazine*, vol. 17, no. 1, pp. 66-73 (2014)

Current Regulation: Closed loop performance



RPTE.UA83.RB.A78 – LHC 13 kA



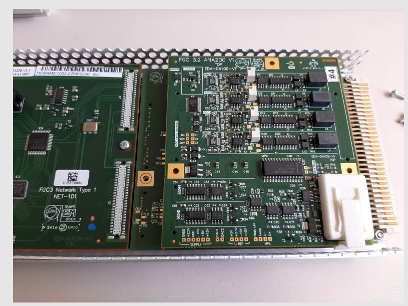
High Luminosity LHC

- Upgrade of the LHC to achieve >5x higher instantaneous luminosity and extend the life of LHC till 2040
- New magnets, crab cavities, superconducting links, etc.

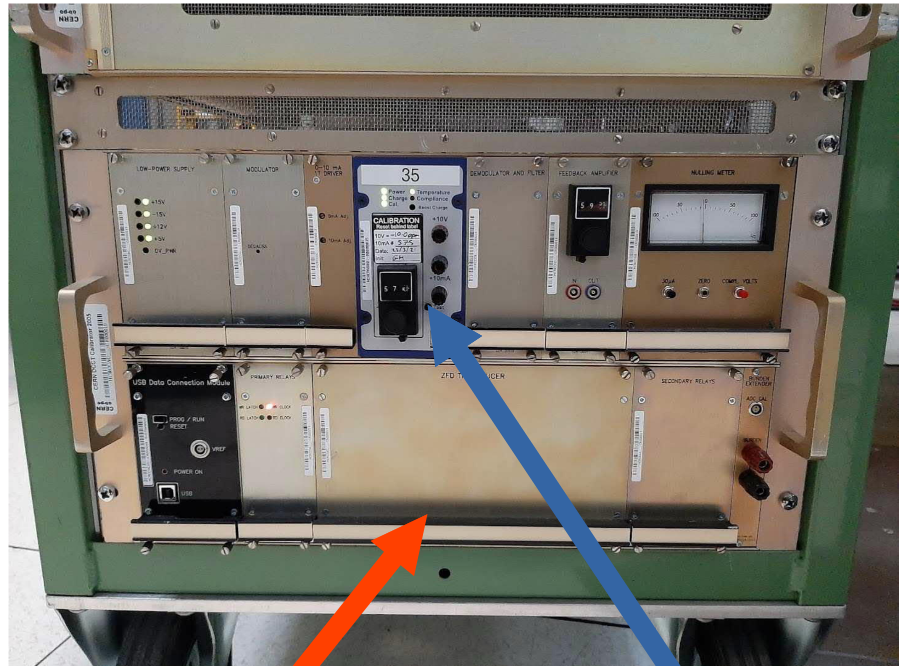
  https://hilumilhc.web.cern.ch/

- Some of our section's HL-LHC activities:
  - **Digitizers** – improvement / development, external production, testing
  - **DCCTs** – specification, procurement, testing, R&D on burden resistors
  - **Test infrastructure** – improvement for Class 0 DCCT testing

Digitizers for HL-LHC

Accuracy class	Digitizer	Controller	
0 and 2	HPM7177 **new development**	FGC3	
0.5	DS24 **improvement**	FGC2	
1	DS22	FGC2	
3 and >3	ANA104 **improvement**	FGC3	

HL-LHC – Class 0 Test Infrastructure



0-10 A current calibrator ($I_{nominal}$ = 5A) [3]

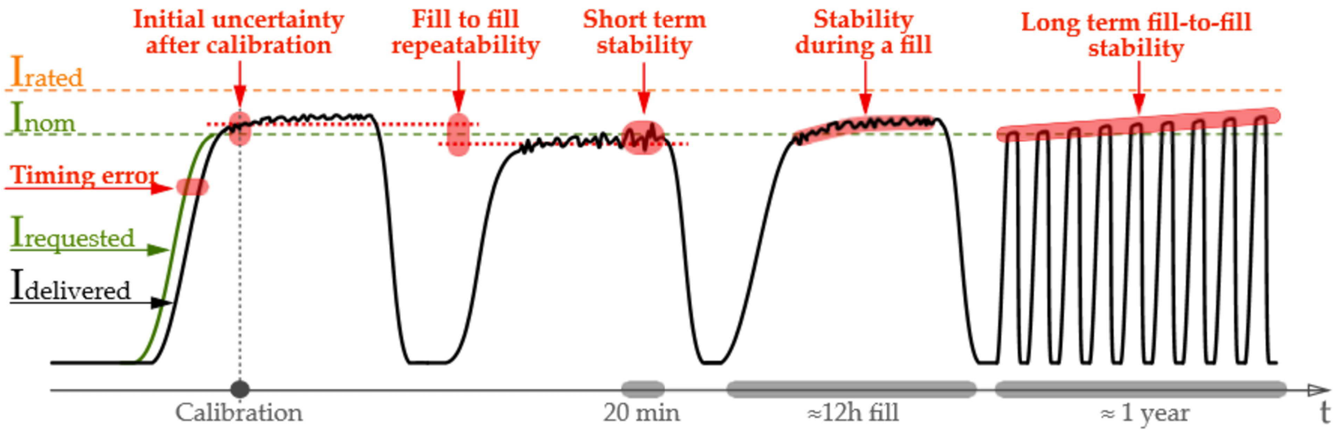
10 mA/10 V standard (“PBC”) [4]

presently working on improved versions

[2] *Fernqvist, G, Halvarsson, B., Pett, J.* **The CERN current calibrator-a new type of instrument**. CPEM-2002 (Ottawa, CA)

[3] *Fernqvist, G, Hudson, G., Pickering,* J. *Power, F.* **Design and evaluation of a 10-mA DC current reference standard**. IEEE TIM 52:2 (2003)

HL-LHC Class 0 Requirements

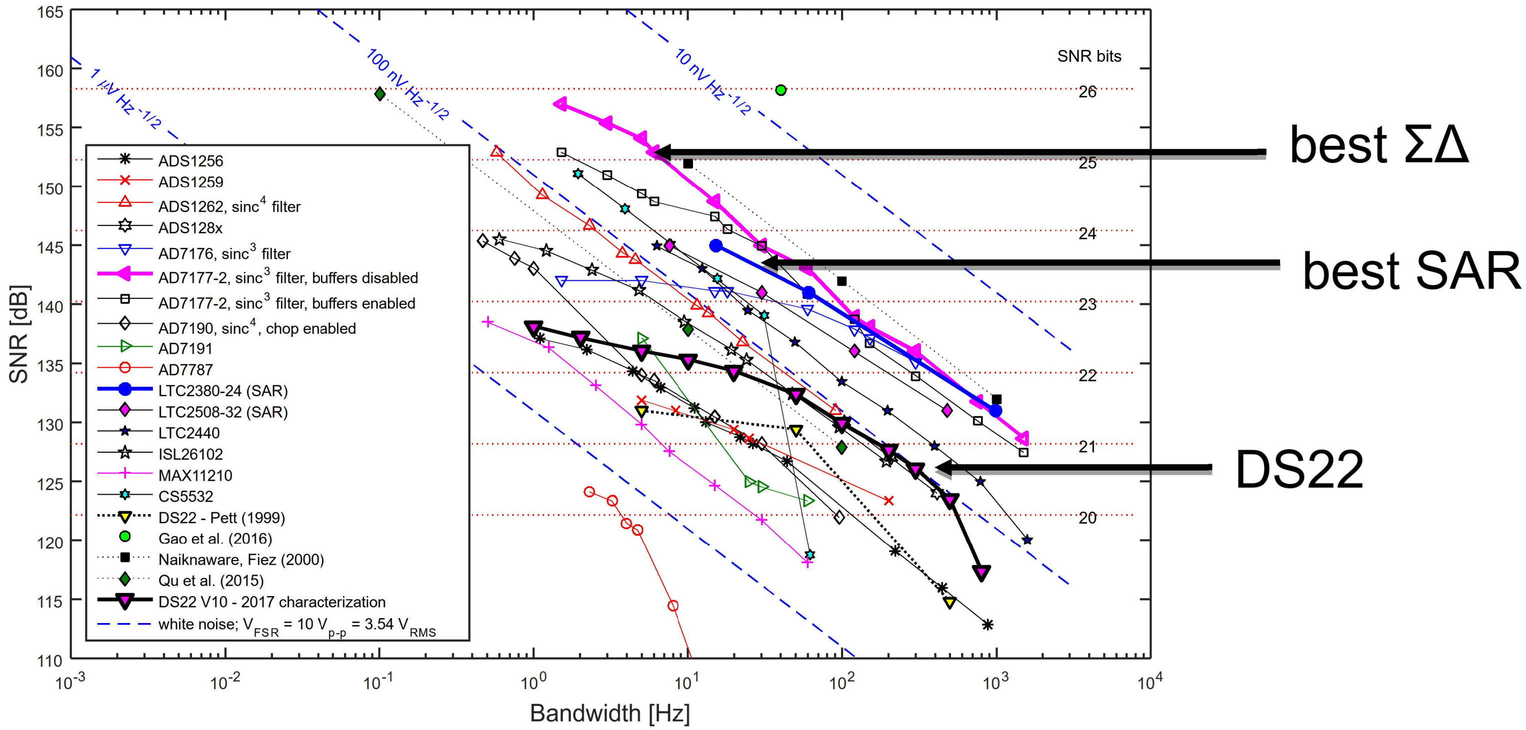


	Class 0		
	total PC	ADC	
Setting resolution [ppm]	0.5	0.2	T = *const.*
Initial uncertainty after cal. [2xrms ppm]	2.0	1.0	
Linearity [ppm] [max abs ppm]	2.0	1.0	
Stability during a fill * (12h) [max abs ppm]	**0.7**	**0.2**	
Short term stability (20min) [2xrms ppm]	**0.2**	**0.1**	
Noise (<500Hz) [2xrms ppm]	**3.0**	**1.0**	
Fill to fill repeatability [2xrms ppm]	**0.4**	**0.1**	
Long term fill to fill stability [max abs ppm]	8.0	4.0	
Temperature coefficient [max abs ppm/C]	**1.0**	**0.2**	ΔT = 0.5 ºC

[4] D. Gamba *et al*. Update of beam dynamics requirements for HL-LHC electrical circuits.CERN-ACC-2019-0030

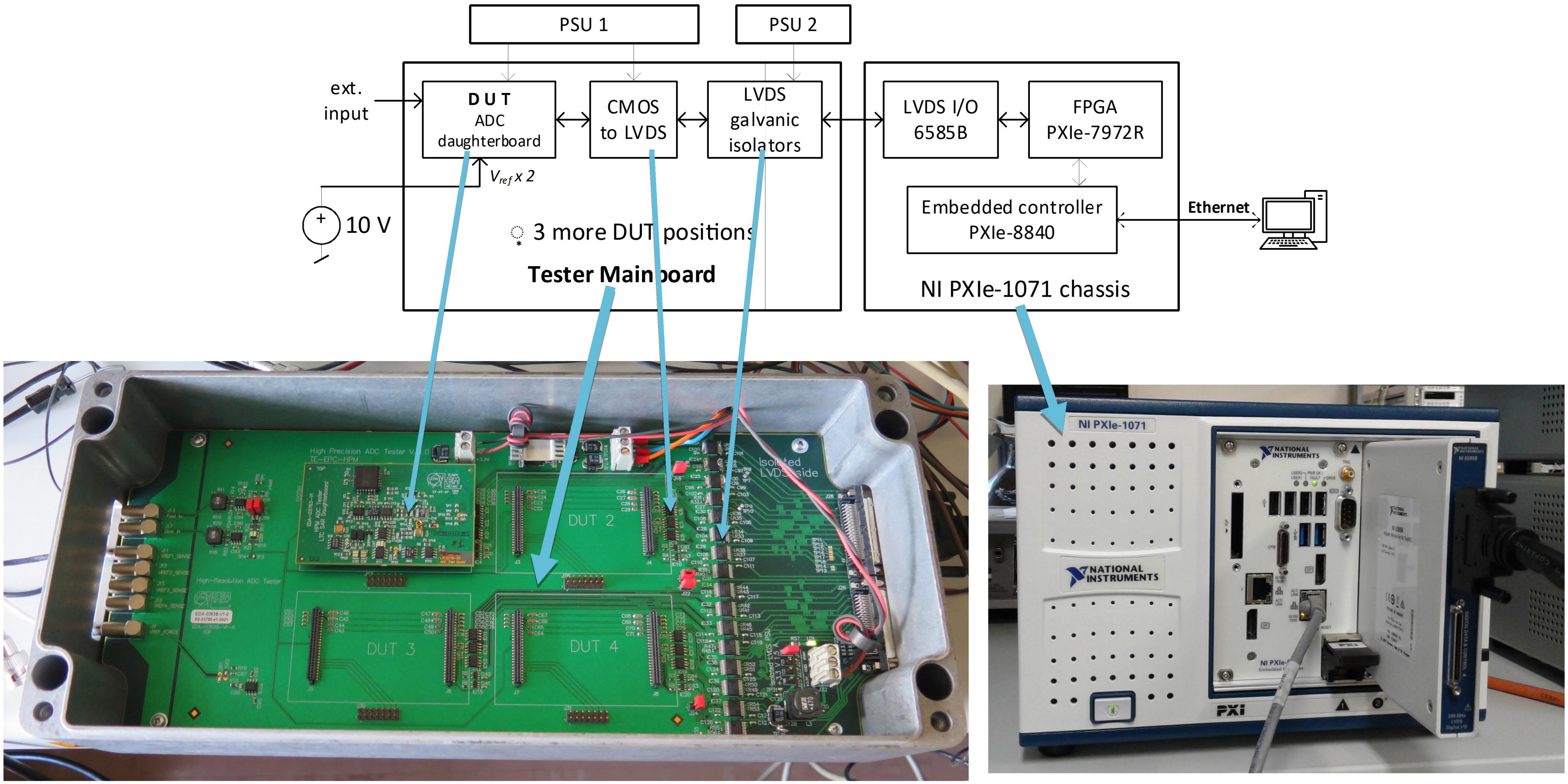
HPM7177 – starting points

- Market study of commercial ADCs – noise, linearity, temperature drift, etc. (2017)

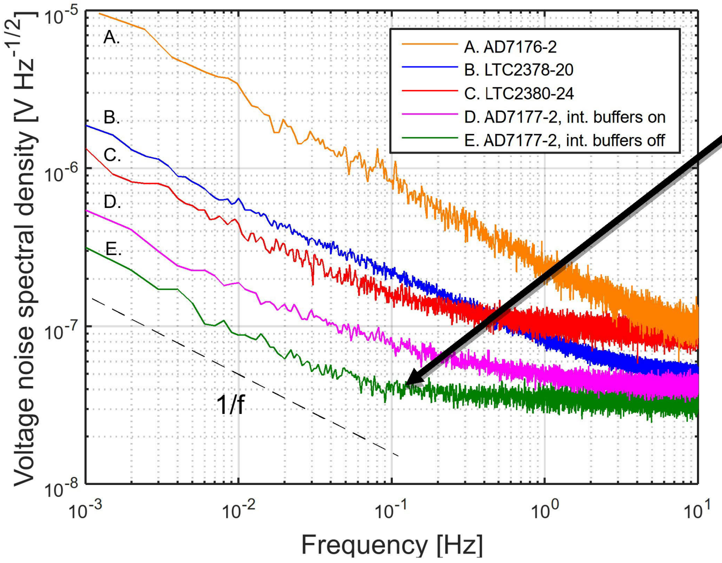


[5] Beev, N. **Analog to digital conversion beyond 20 bits.** I2MTC-2018 (Houston, TX)

Testing of commercial ADCs



Selection of AD7177-2



AD7177-2 is the clear winner

- 32 nV $Hz^{-1/2}$ white noise
- 15 nV_{RMS}/decade 1/f noise
- $f_{corner} \approx 0.05$ Hz

- reproducible between devices

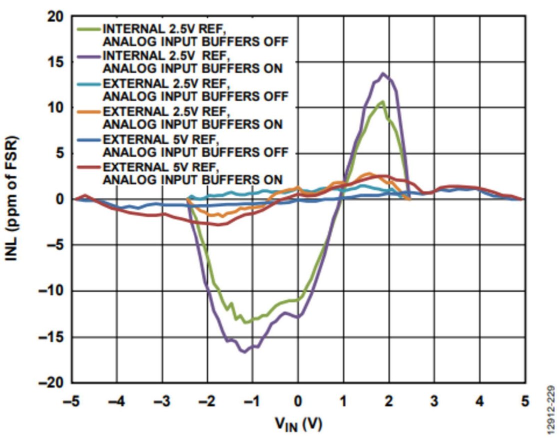


Figure 19. Integral Nonlinearity (INL) vs. V_{IN} (Differential Input)

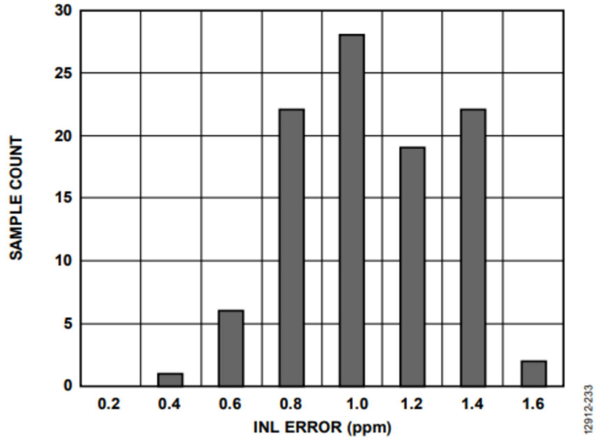


Figure 23. Integral Nonlinearity (INL) Distribution Histogram (All Input Buffers Disabled, Differential Input, V_{REF} = 5 V External, 100 Units)

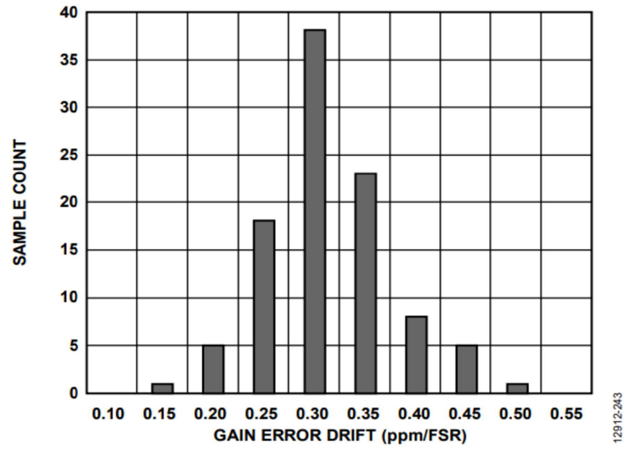
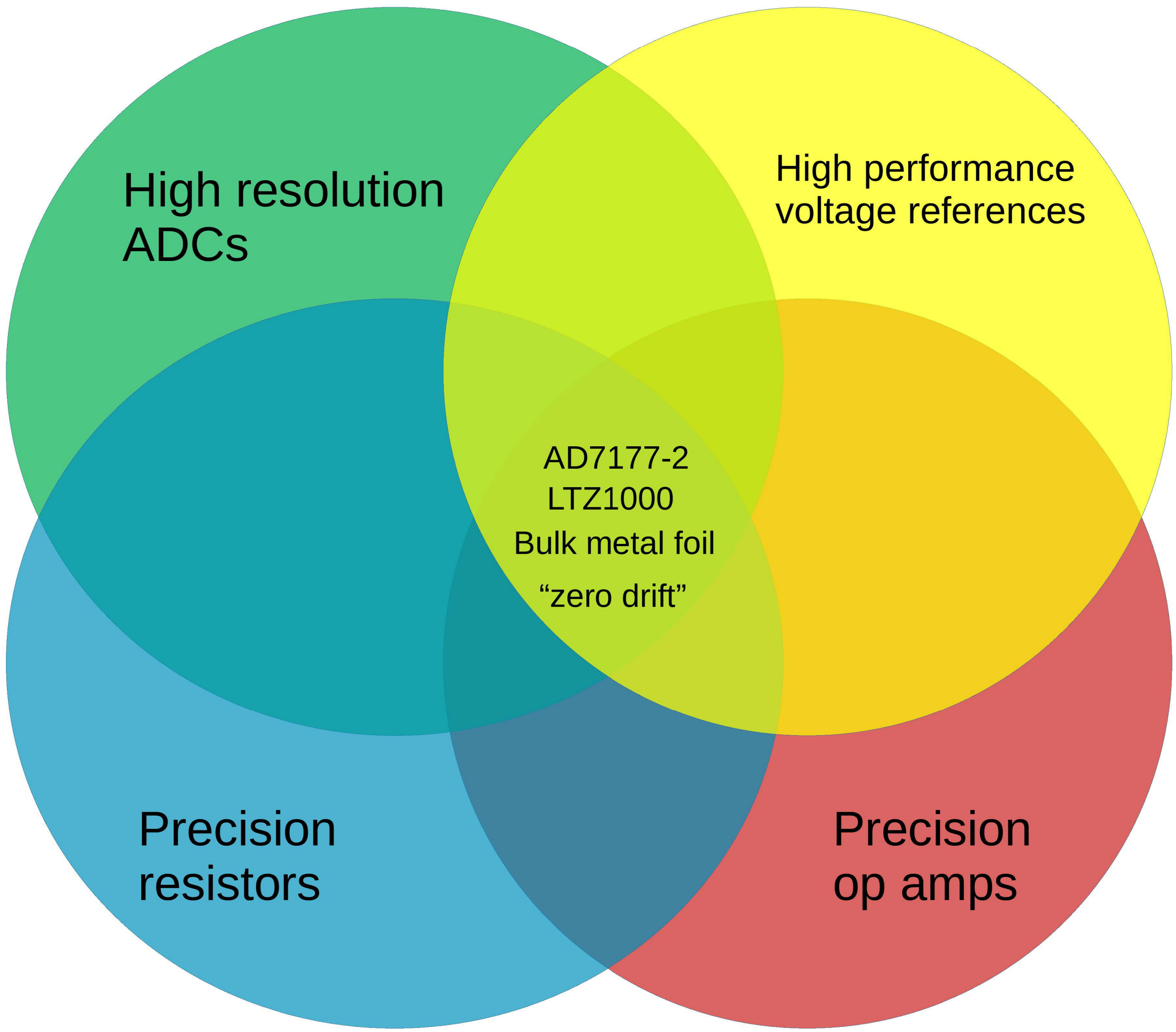
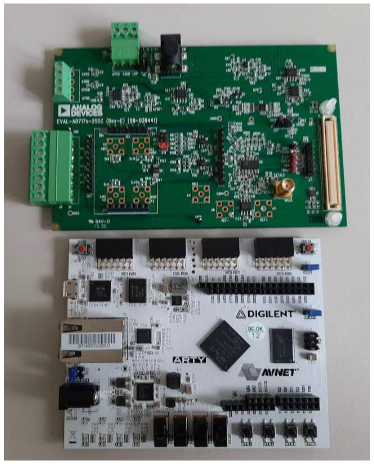


Figure 33. Gain Error Drift Distribution Histogram (All Input Buffers Disabled, 100 Units)

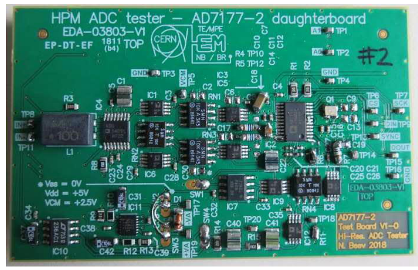
HPM7177 - Concept



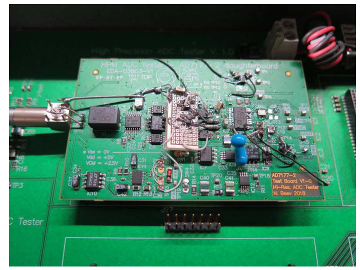
HPM7177 – Evolution



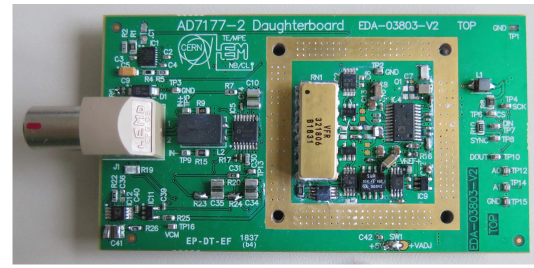
V0.01



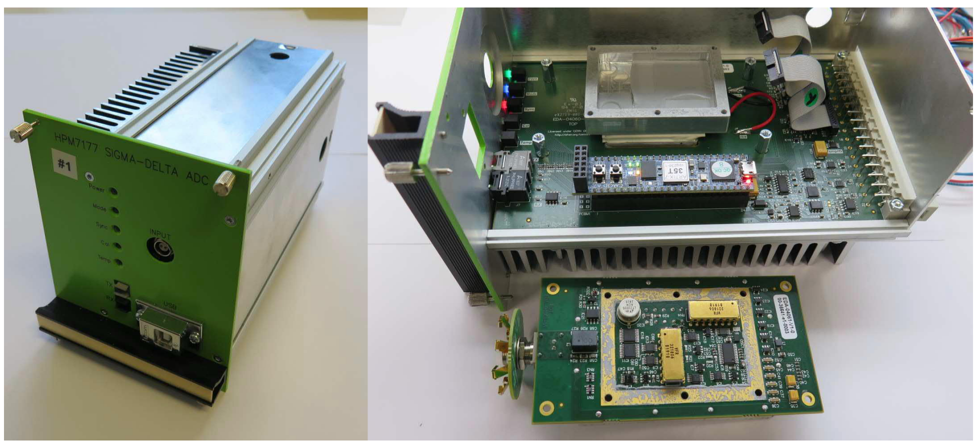
V0.1



V0.15



V0.2



V1

with LTZ1000

V2

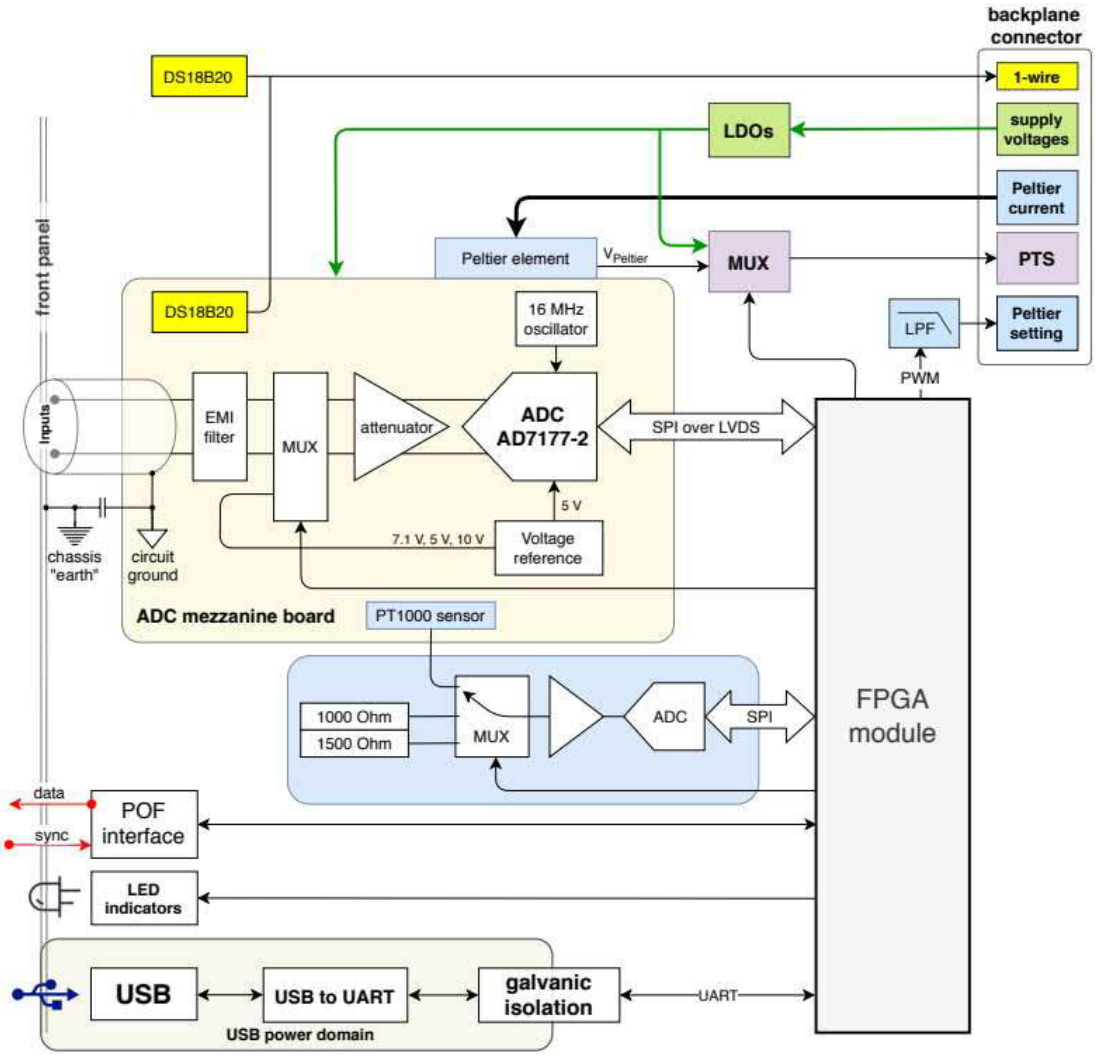
...coming soon...

V3

with ADR1000

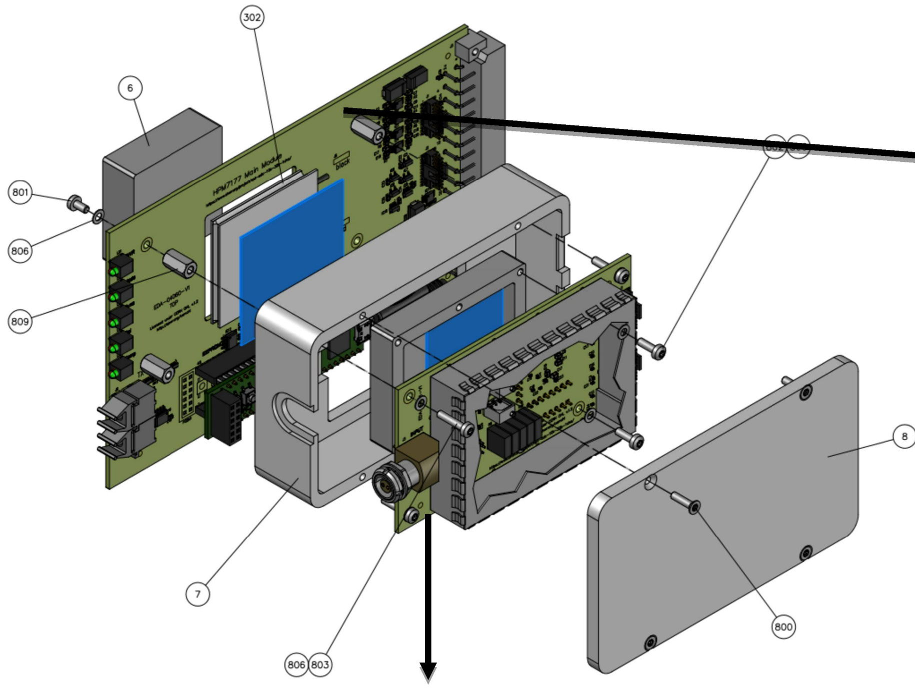
HiLumi HL-LHC PROJECT

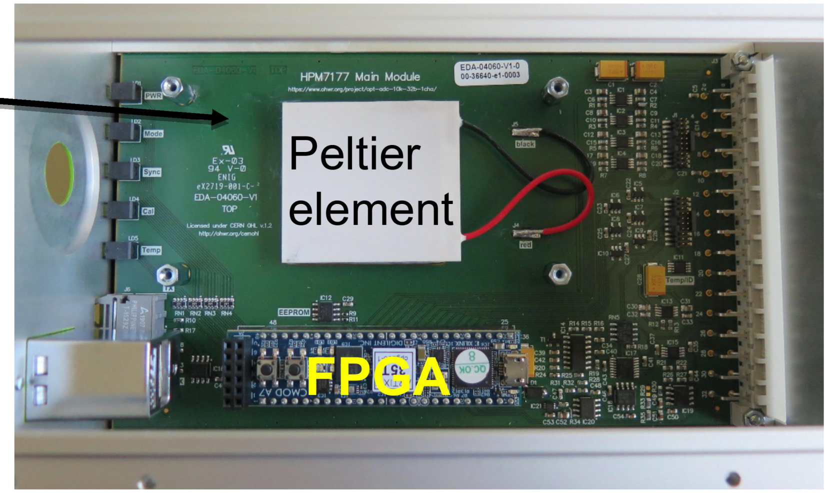
HPM7177 - Architecture



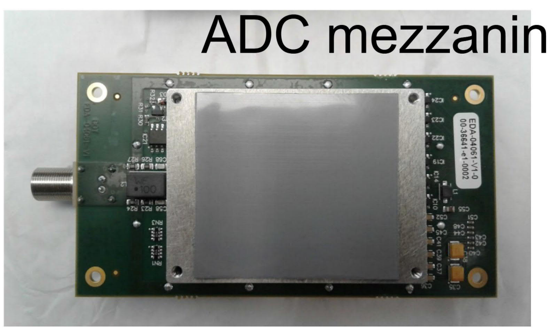
https://ohwr.org/project/opt-adc-10k-32b-1cha/wikis/

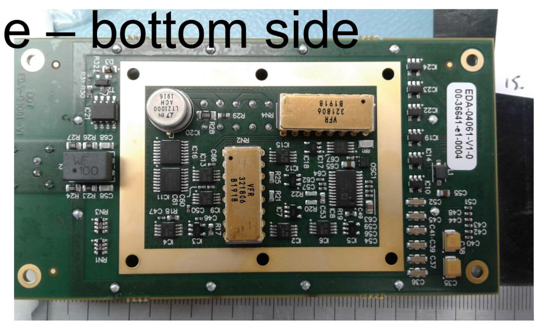
HPM7177 – Realization

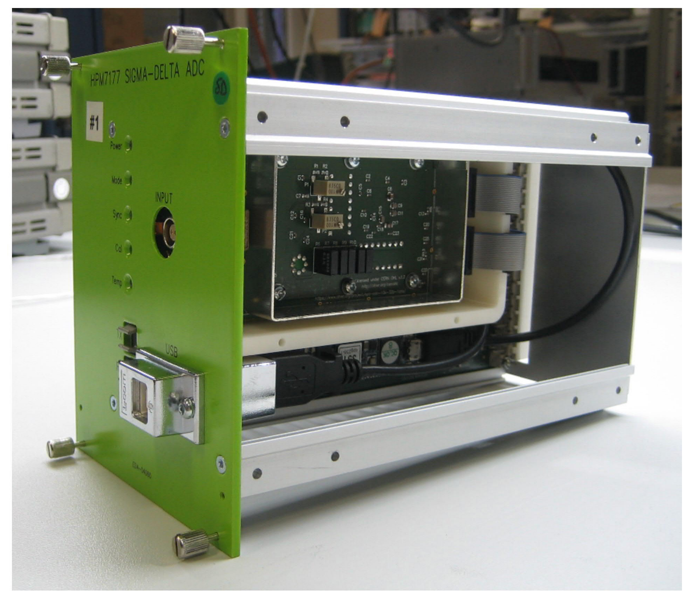




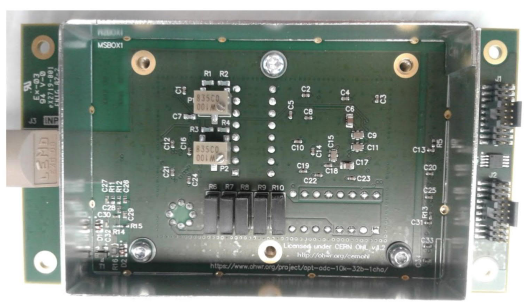
ADC mezzanine – bottom side





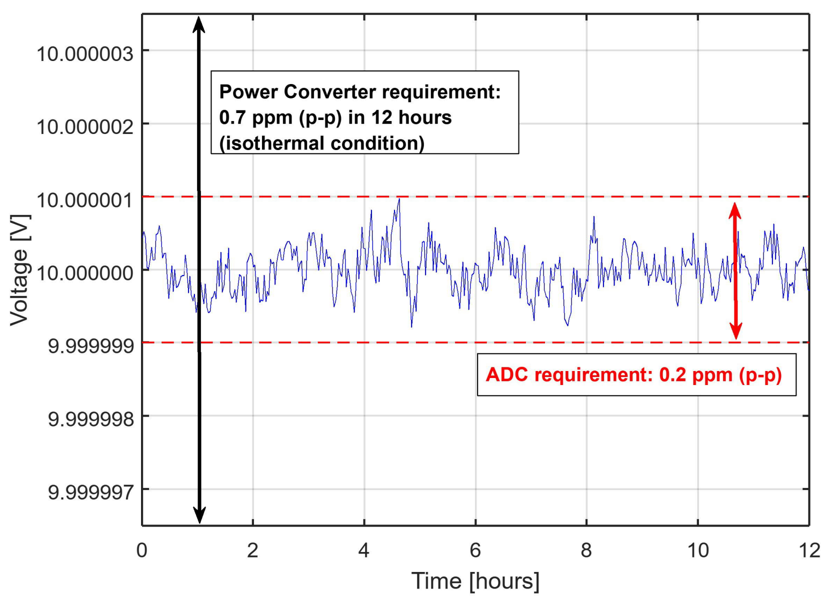


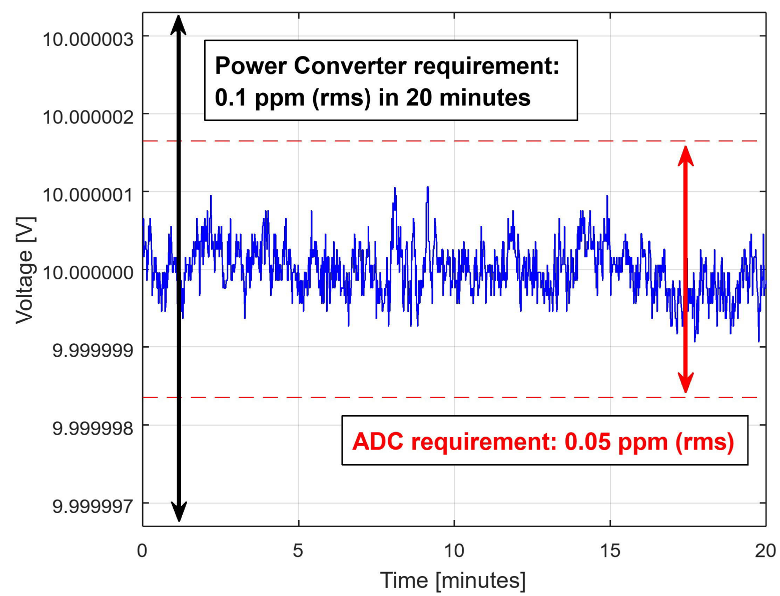
ADC mezzanine - top side



Characterization - Noise and stability

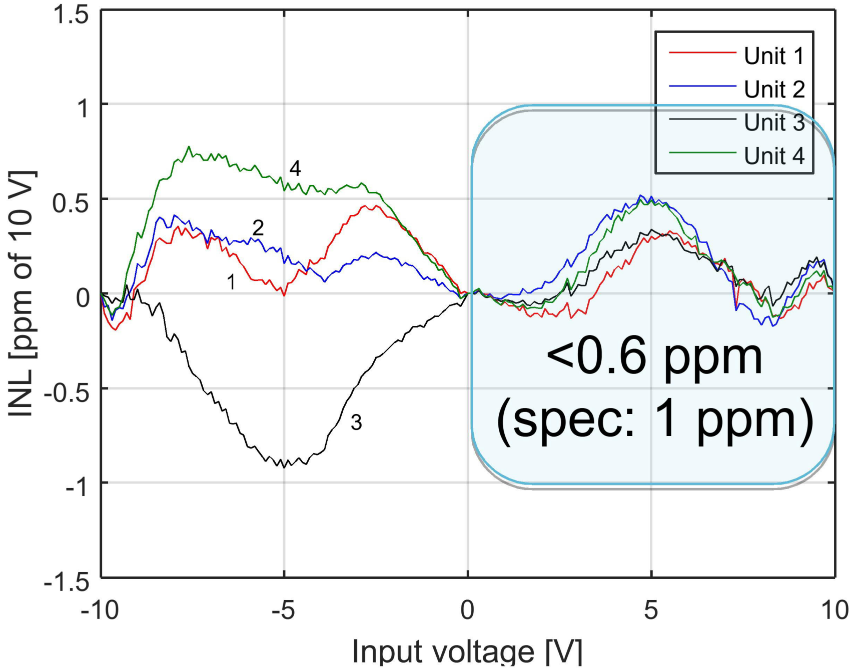
- 12-hour stability – a typical LHC fill
- Short-term stability (20 min.) – important for K-modulation, fully in the current regulation loop bandwidth (<0.1 Hz)
- 500 Hz bandwidth noise – mostly for monitoring of the power converter; has little or no effect on the current regulation

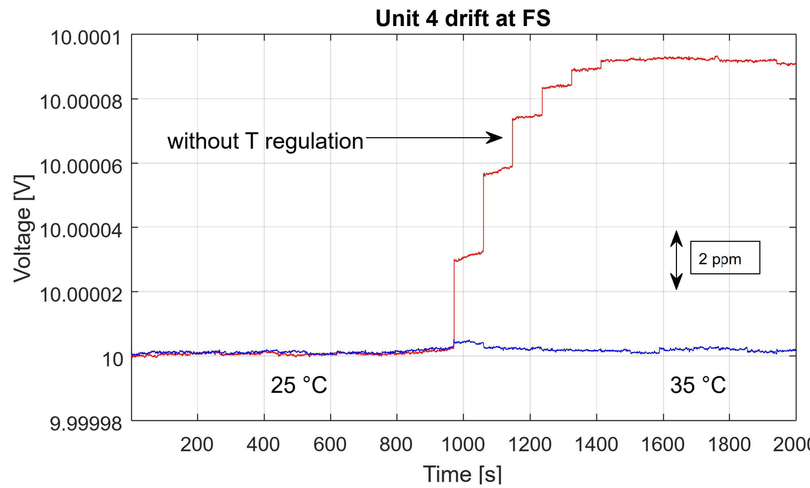




Characterization – Linearity and TC

- Integral non-linearity (INL) for Class 0 circuits is defined for (0 to +FS)
- Thanks to the active temperature control, TC is very low in all units tested so far (<0.05 ppm/degree C)



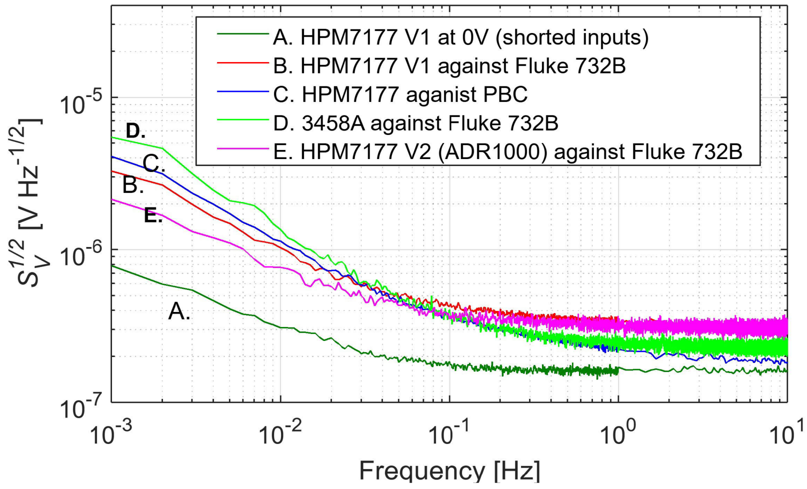


	Offset drift [ppm/°C]	Gain drift [ppm/°C]
Unit 1 (V1)	+0.017 ± 0.003	-0.032 ± 0.006
Unit 2 (V1)	+0.0065 ± 0.002	+0.03 ± 0.005
Unit 3 (V1)	+0.0046 ± 0.002	+0.01 ± 0.006
Unit 4 (V1)	+0.014 ± 0.002	-0.006 ± 0.006

Characterization results - summary

Specification	Conditions	Unit	HL-LHC Class 0 ADC guideline	HPM7177
Noise	0.1 – 500 Hz	ppm (rms)	0.5	0.36
Short-term stability	1 – 100 mHz	ppm (rms)	0.05	< 0.023 (V1)
Fill stability	20 µHz to 10 mHz	ppm (p-p)	0.2	< 0.2
Linearity	*2-point* (0 to +FS)	ppm	1	0.6
Temperature coefficient	T_{amb} = 20°C to 40°C	ppm/°C	0.2	< 0.05

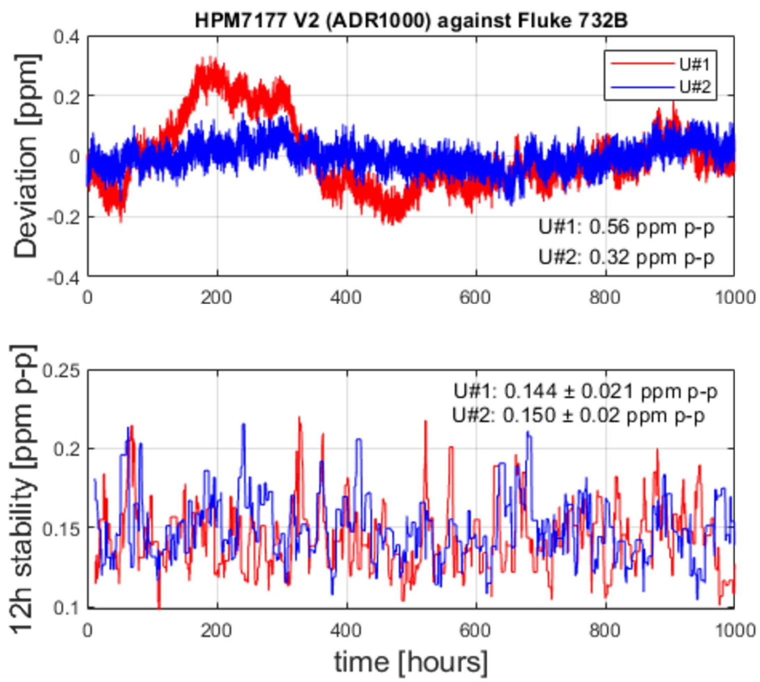
Some recent results with V2 prototypes

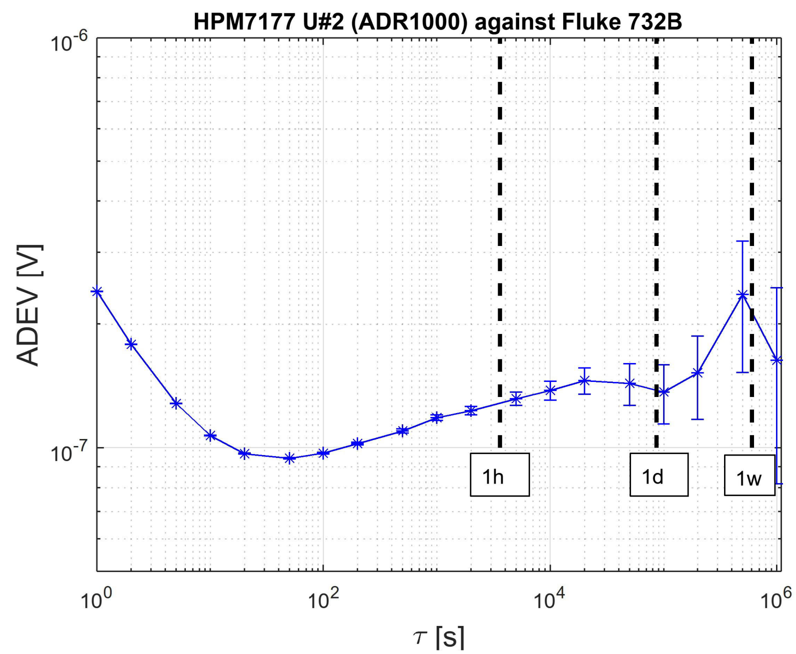


LF noise (0.001-0.1Hz) against Fluke 732B

- 276 nV_{RMS} (3458A)
- 230 nV_{RMS} (HPM7177 V1)
- 168 nV_{RMS} (HPM7177 V2)

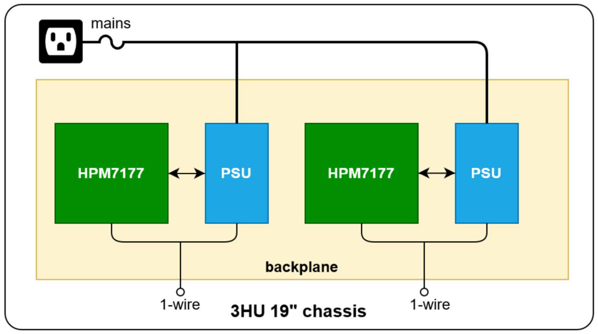
contribution of 732B ≈ 110 nV_{RMS}

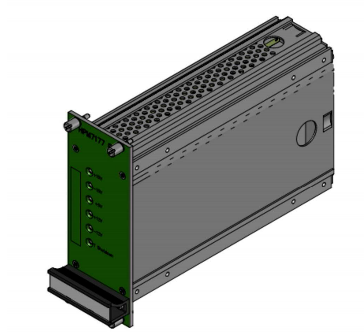




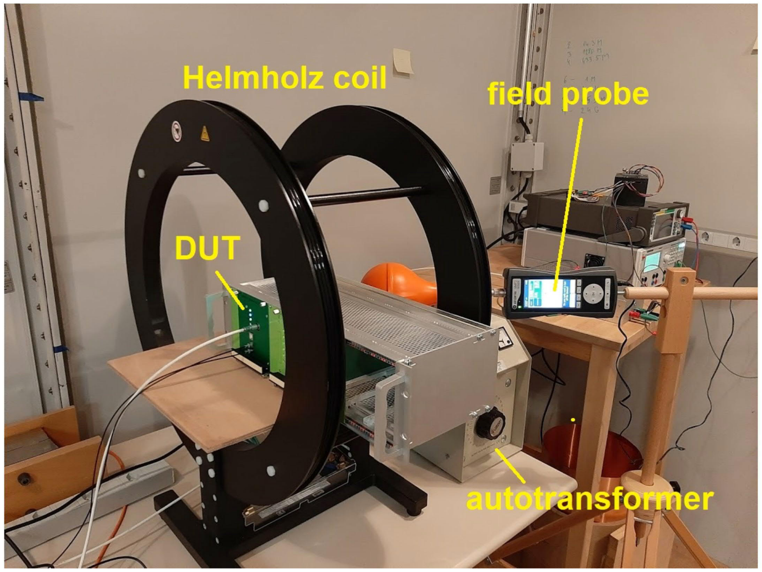
Chassis and power supply

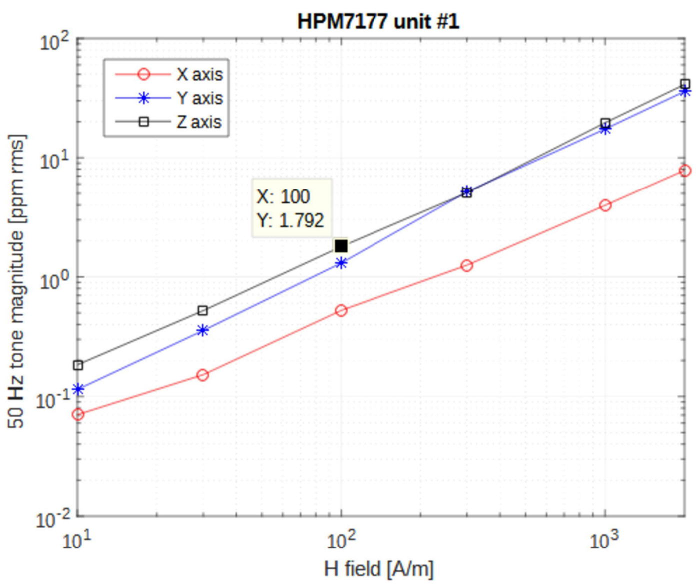
- The 19” chassis hosts two ADCs and two PSUs
- As of September 2021 the V2 prototypes of the PSU are under production and the chassis design is being revised





EMC tests – LF magnetic field susceptibility





- According to IEC 61000-4-8B

- 50 Hz up to 1000 A/m

+ *2000 A/m (beyond standard)*

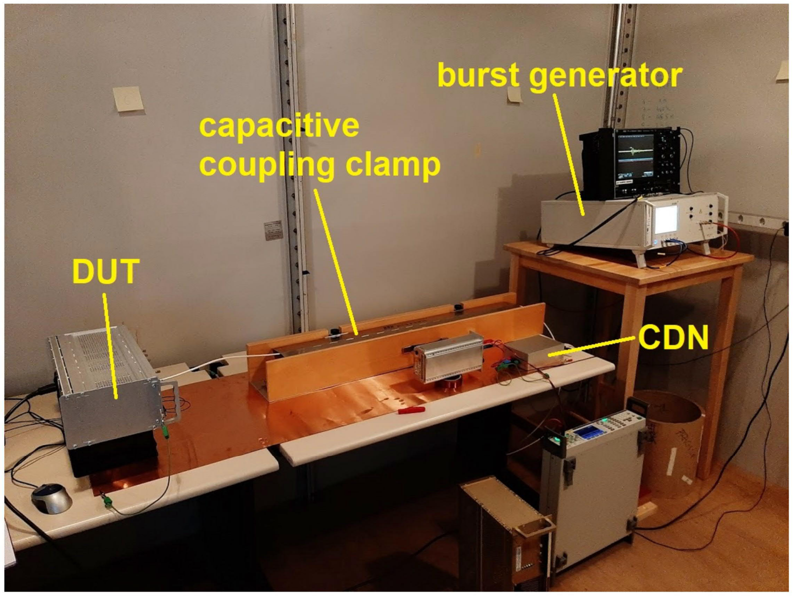
- DC up to 1000 A/m

+*1500 A/m (beyond standard)*

- No detectable sensitivity to DC fields
- AC field sensitivity at 50 Hz is highest in the Z direction

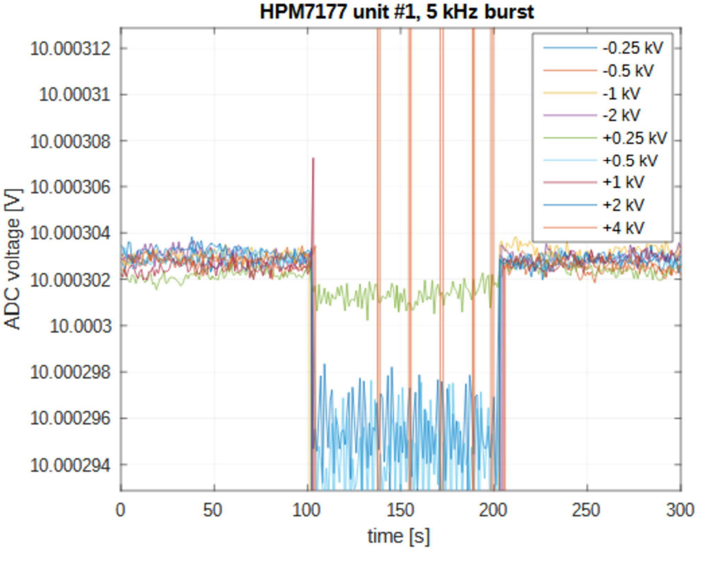
≈0.018 ppm A^{-1} m

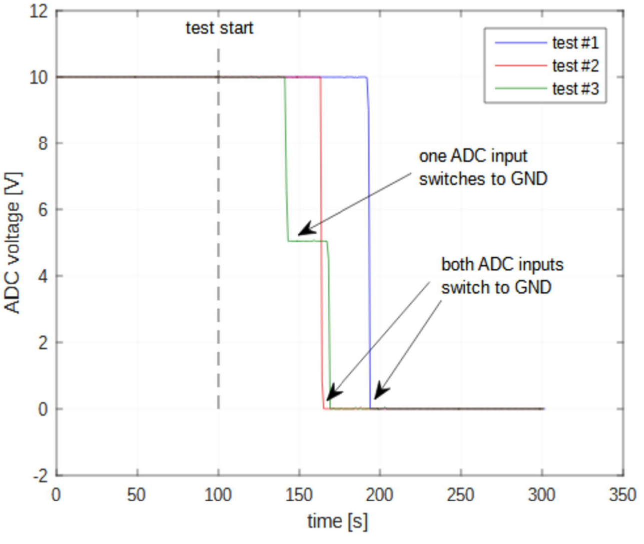
EMC tests – EFT susceptibility



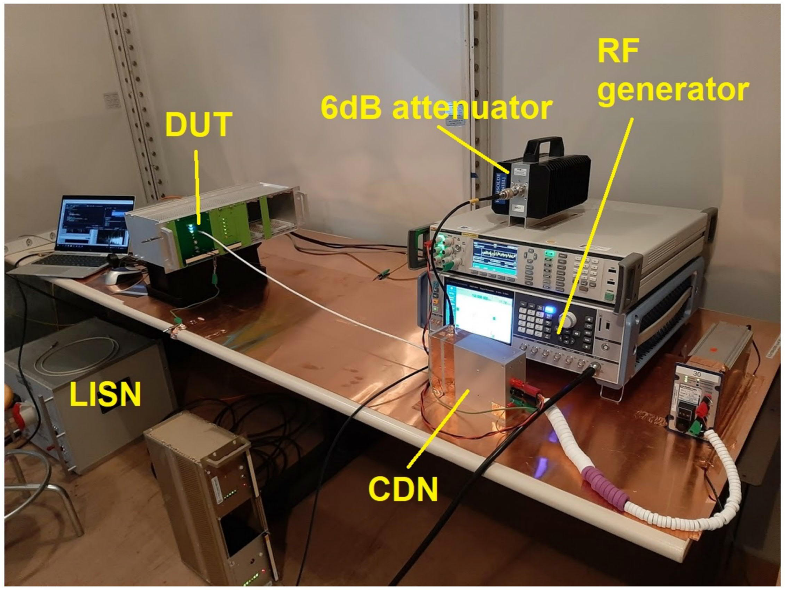
- According to IEC 61000-4-4B
- 5 kHz/15 ms and 100 kHz/0.75 ms burst
- ±0.25 to ±2 kV
- *±4 kV (beyond standard)*

- The ADC chip fails at -4 kV tests.
- The fault is software-reversible
- A HW modification was made in V3 to fix this issue



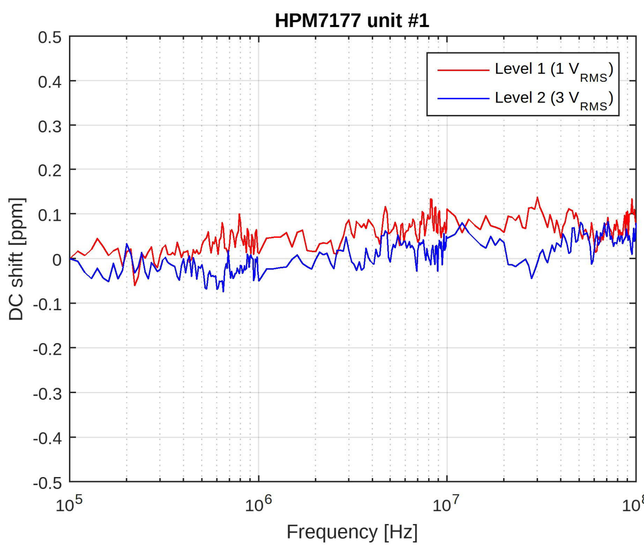


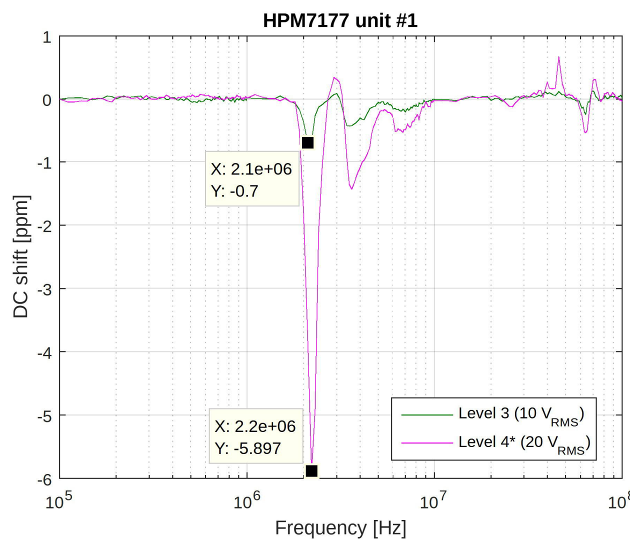
EMC tests – conducted RF susceptibility



- According to IEC 61000-4-6B
- RF with 1 kHz 80% AM
- RF 10 kHz to 100 MHz
- Levels: 1,3,10 V_{RMS} (open circuit) *20 V_{RMS} (beyond standard)*

- No effects visible at levels 1 and 2
- Sub-ppm DC shifts at level 3
- A few ppm shifts at level 4
- Sensitivity at some specific frequencies (N*10kHz, 16 MHz)





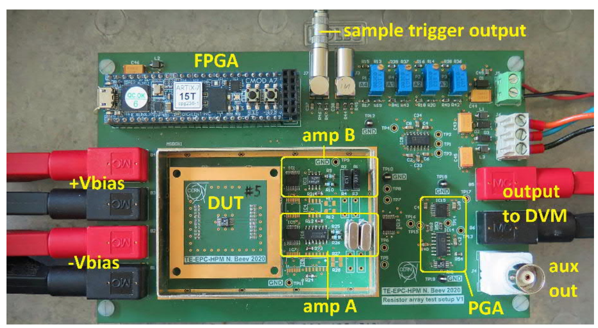
Next steps

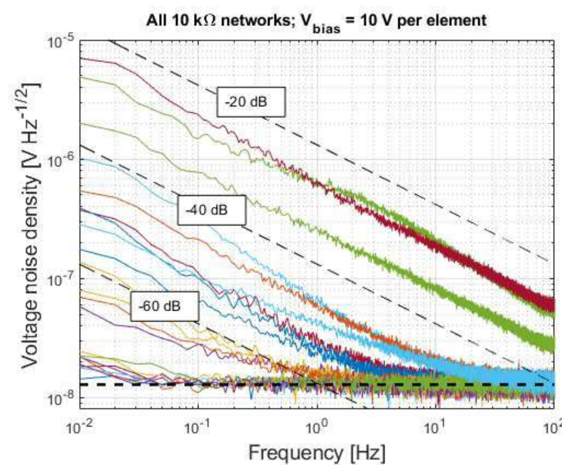
- Ongoing tender for the production of 110 units:
  - pre-series for the IT String project (2022)
  - series for HL-LHC (2023/2024)
- Consolidation of the FPGA configuration and firmware
- Integration tests with FGC 3.1
- CE certification of the chassis and PSU
- Ultimate noise and linearity characterization using the 10 V Programmable Josephson Voltage Standard (PJVS) at PTB – Braunschweig *(cancelled in 2020 due to COVID-19)*

Excess Noise in Thin Film and Metal Foil Resistor Networks

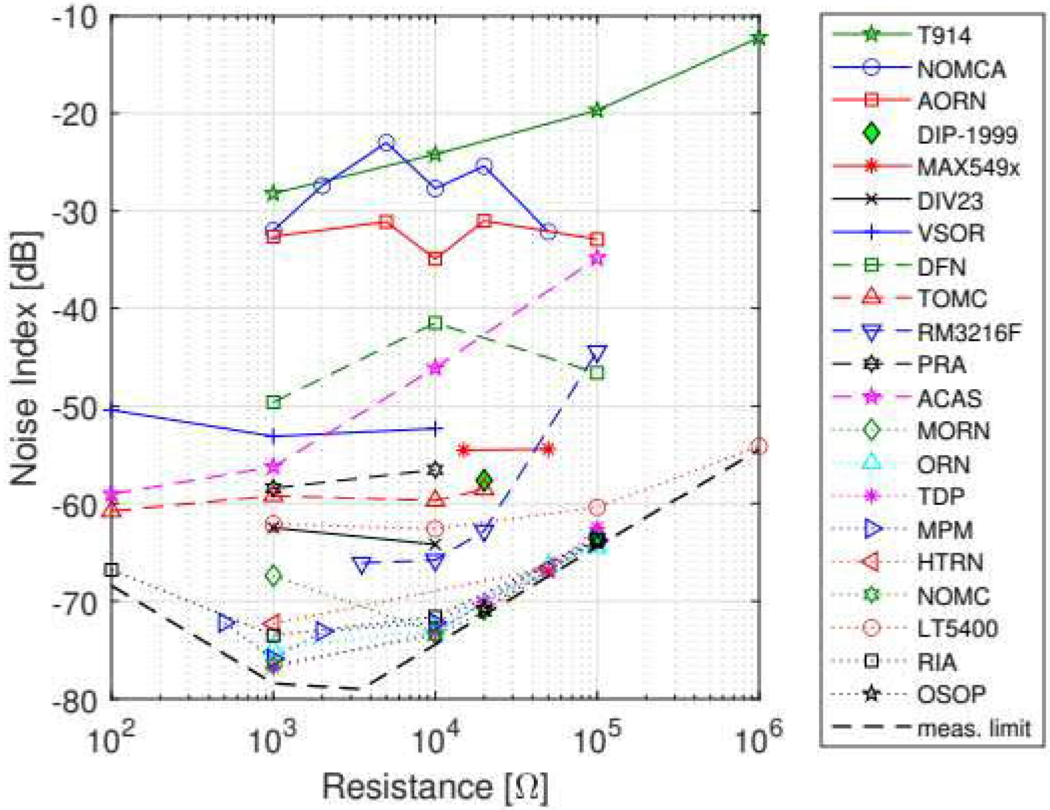
- Excess noise – due to fluctuating resistance.
- Thin film, foil and wirewound resistors have the lowest levels.
- Relatively difficult to measure → not always well specified by manufacturers.

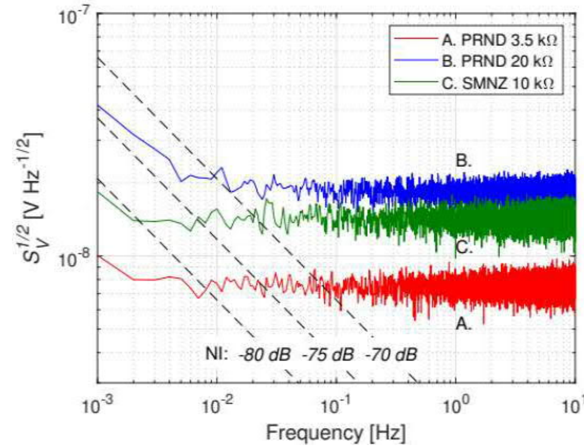
- A special test setup was devised
- >100 commercially available devices were tested
- 24 different families: 21 thin film and 3 BMF.
- Values from 100Ω to 1 MΩ
- A few hours per test
- Results span a few orders of magnitude
- Lowest noise was found in metal foil and NiCr thin films on Si substrates

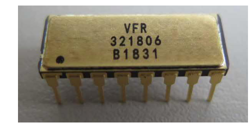




Excess Noise in Thin Film and Metal Foil Resistor Networks







NI [dB]	NiCr		TaN	other
> -40			NOMCA, AORN	T914 *(Tetrinox®)*
-40 to -60	ACAS, PRA	DFN	DIP-1999, VSOR	MAX549x *(CrSi)*
< -60	RM3216F, LT5400, NOMC, MORN, OSOP, HTRN	TOMC, RIA, ORN, TDP, MPM	DIV23	**metal foil: NiCr with additives** SMN / SMNZ, PRND, VHD

substrate: Si, Al_2O_3, Al_2O_3 (foil)

[6] N. Beev. Measurement of Excess Noise in Thin Film and Metal Foil Resistor Networks (2021)
https://arxiv.org/pdf/2109.02448

Thin Film vs Metal Foil

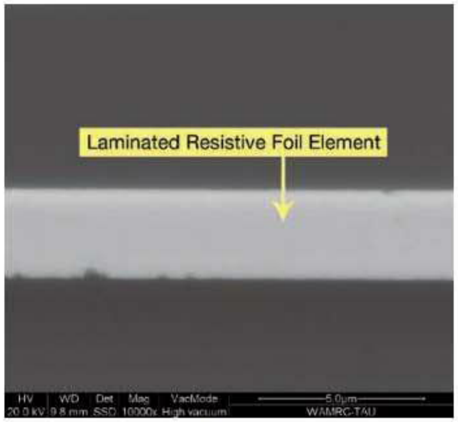


Figure 1. VSM0805 100R (X10,000)

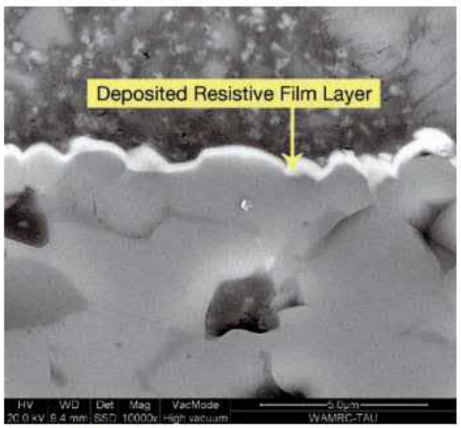
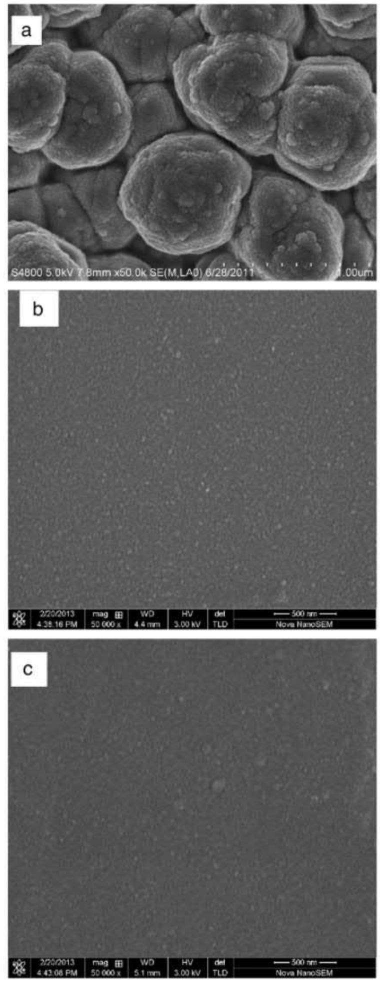
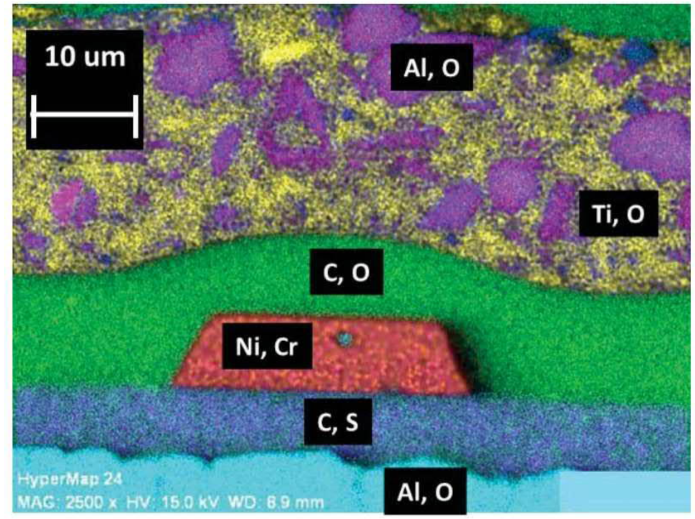


Figure 2. Thin film resistor 110R (X10,000)

[7]





Foil gridline cross-section [9]

NiCr film surface [8]
a) Cu foil substrate
b) glass substrate
c) silicon substrate

[7] R. Goldstein *et al*. **Study of Foil Resistors Under Exposure to High-Temperature, Moisture, and Humidity.** VPG Technical Note 110

[8] L. Lai *et al.* **Comparison of microstructure and electrical properties of NiCr alloy thin film deposited on different substrates.** Surface and Coatings Technology, 235:552–560 (2013)

[9] J. Brusse and L. Panaschchenko. **A Screening Method Using Pulsed-Power Combined with Infrared Imaging to Detect Pattern Defects in Bulk Metal Foil or Thin Film Resistors**. SPCD-TN66231 (2018)

Thank you!