

SPECIFICATIONS FOR LCD MODULE

| | |
|--------------------------|---|
| CUSTOMER | |
| CUSTOMER PART NO. | |
| AMPIRE PART NO. | 13232ASWQW-02 <small>(preliminary spec)</small> |
| APPROVED BY | |
| DATE | |

Approved For Specifications

Approved For Specifications & Sample

| APPROVED BY | CHECKED BY | ORGANIZED BY |
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| | | |

RECORD OF REVISION

| Revision Date | Page | Contents | Editor |
|----------------------|-------------|-----------------|---------------|
| 2007/4/4 | - | New Release | Lorry |

1 FEATURES

- (1) Display format : 132×32 dots, 1/49duty, 1/7 bias.
- (2) Construction : LCD panel , COG, IC, Metal Pin and White LED Back-Light.
- (3) Display type : STN LCD, Transmissive, Negative, Blue mode, Antiglare, 4:30 o'clock view
- (4) Controller : ST7588T
- (5) Extended temperature type.
- (6) ROHS compliant.

2 MECHANICAL DATA

| Parameter | Stand Value | Unit |
|----------------------------------|--------------------------------|------|
| Dot size | 0.67(W) × 0.56(H) | mm |
| Dot pitch | 0.71(W) × 0.6(H) | mm |
| Active area | 93.68(W) ×19.16 (H) | mm |
| Viewing area | 98.0 (W) ×23.0 (H) | mm |
| Module size Without Metal PIN | 113.0(W) × 34.24(H) × 15.0 (T) | mm |

3 ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|------------------------------|---------|------|---------|------|
| Logic Circuit Supply Voltage | VDD-VSS | -0.5 | +3.6 | V |
| LCD Driving Voltage | VLCD | -0.5 | +13.5 | V |
| Input Voltage | VI | -0.5 | VDD+0.5 | V |
| Operating Temp. | TOP | -20 | 70 | °C |
| Storage Temp. | TSTG | -30 | 80 | °C |

4 ELECTRO-OPTICAL CHARACTERISTICS

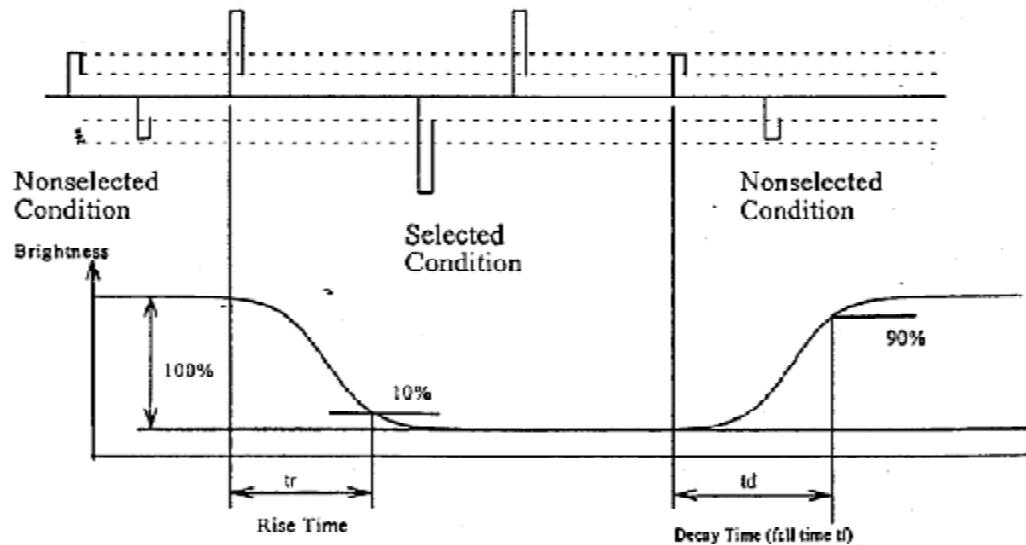
| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Note |
|---|---------|----------------|--------|-------|---------|------|--------|
| ----- Electronic Characteristics ----- | | | | | | | |
| Logic Circuit Supply Voltage | VDD-VSS | -- | 2.4 | -- | 3.3 | V | |
| LCD Driving Voltage | VLCD | 25 °C | 8.5 | 9.0 | 9.5 | V | |
| Input Voltage | VIH | -- | 0.7VDD | -- | VDD | V | |
| | VIL | -- | -0 | -- | 0.3 VDD | V | |
| Logic Supply Current | IDD | VDD=3.0V | -- | 0.2 | 0.4 | mA | |
| ----- Optical Characteristics (FSTN) ----- | | | | | | | |
| Contrast | CR | 25°C | -- | (6) | -- | | Note 1 |
| Rise Time | tr | 25°C | -- | (200) | -- | ms | Note 2 |
| Fall Time | tf | 25°C | -- | (200) | -- | ms | |
| Viewing Angle Range | θ f | 25°C & CR≥2 | -- | (40) | -- | Deg. | Note 3 |
| | θ b | | -- | (35) | -- | | |
| | θ l | | -- | (40) | -- | | |
| | θ r | | -- | (40) | -- | | |
| Frame Frequency | ff | 25°C | -- | 70 | -- | Hz | |

() : For Reference only. These data should be measured and defined according real LCD.

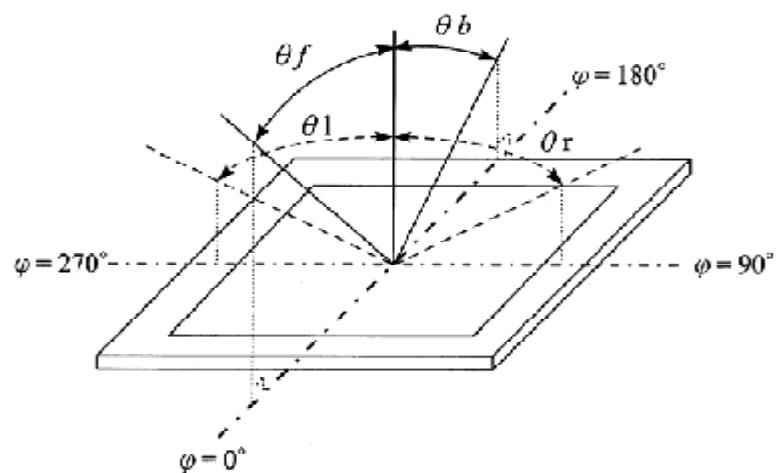
(NOTE 1) Contrast ratio :

CR = (Brightness in OFF state) / (Brightness in ON state)

(NOTE 2) Response time :



(NOTE 3) Viewing angle



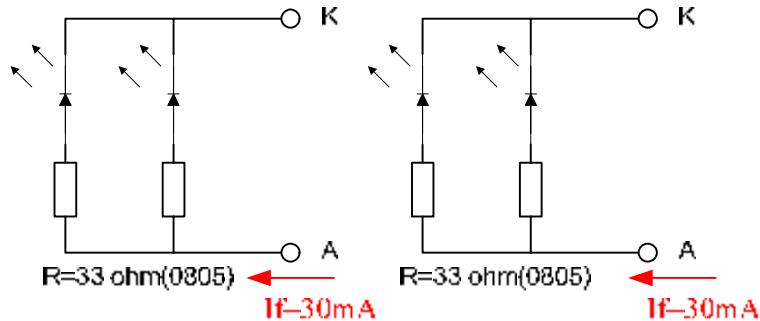
4.1 LED Back-light Electrical Specification

| ---- White LED Back-light Characteristics ----- | | | | | | | |
|---|--------|-----------------------------|------|-------|------|-------------------|--------|
| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Note |
| Forward Current | IF | -- | -- | 30x2 | 40x2 | mA | Note 4 |
| LCM Luminous intensity (Full White pattern) | | IF=30mA \times 2 Total | -- | T.B.D | -- | cd/m ² | Note 4 |
| Forward Voltage | VF | IF=30mA each side | 3.0 | 3.2 | 3.5 | V | Note 5 |
| LED C.I.E | X | IF=30mA \times 2 Total | 0.28 | 0.31 | 0.34 | | Note 6 |
| | Y | IF=30mA \times 2 Total | 0.29 | 0.32 | 0.35 | | |

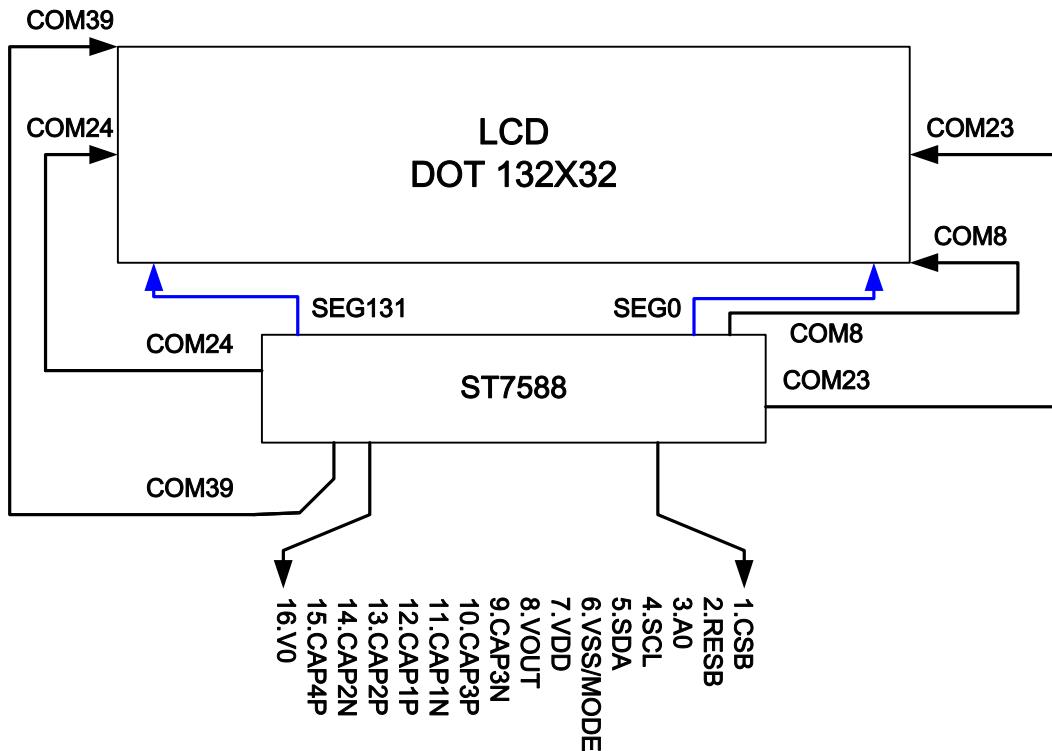
Note 4: Luminous intensity is decided by forward current of White LED.

Note 5: White LEDs are with voltage tolerance.

Note 6: White LEDs are with color tolerance.



5 BLOCK DIAGRAM & POWER SUPPLY



Internal Setting: D0=SCL , D1=D2=D3=SDA , D4~D7=VDD ,T5~T0= OPEN, MS=VDD,
Mode1=Mode0=VSS, PS[2:0]=010, VOUT connect to CAP5P

6 INTERFACE

| No. | Symbol | Function |
|-----|----------|--------------------------------------|
| 1 | /CSB | Chip select terminal. |
| 2 | RESB | Reset terminal. |
| 3 | A0(RS) | Connector to the address bus of MPU. |
| 4 | SCL | Serial clock input |
| 5 | SDA | Serial data input |
| 6 | VSS/MODE | Ground (0V) |
| 7 | VDD | Power supply for logic (VDD) |
| 8 | VOUT | Internal Booster circuit. |
| 9 | CAP3N | |
| 10 | CAP3P | |
| 11 | CAP1N | |
| 12 | CAP1P | |
| 13 | CAP2P | |
| 14 | CAP2N | |
| 15 | CAP4P | |
| 16 | V0 | |

When VDD=2.4~2.7V,
5x booster connection.

```

    graph LR
      7[VDD] --- Z1[zener]
      8[VOUT] --- Z2[zener]
      9[CAP3N] --- Z3[zener]
      10[CAP3P] --- Z4[zener]
      11[CAP1N] --- Z5[zener]
      12[CAP1P] --- Z6[zener]
      13[CAP2P] --- Z7[zener]
      14[CAP2N] --- Z8[zener]
      15[CAP4P] --- Z9[zener]
      Z1 --- R1[Resistor]
      Z2 --- R2[Resistor]
      Z3 --- R3[Resistor]
      Z4 --- R4[Resistor]
      Z5 --- R5[Resistor]
      Z6 --- R6[Resistor]
      Z7 --- R7[Resistor]
      Z8 --- R8[Resistor]
      Z9 --- R9[Resistor]
      R1 --- V0[V0]
      R2 --- V0
      R3 --- V0
      R4 --- V0
      R5 --- V0
      R6 --- V0
      R7 --- V0
      R8 --- V0
      R9 --- V0
  
```

C=1.0uF~4.7uF

When VDD=2.7~3.3V,
4x booster connection.

```

    graph LR
      7[VDD] --- Z1[zener]
      8[VOUT] --- Z2[zener]
      9[CAP3N] --- Z3[zener]
      10[CAP3P] --- Z4[zener]
      11[CAP1N] --- Z5[zener]
      12[CAP1P] --- Z6[zener]
      13[CAP2P] --- Z7[zener]
      14[CAP2N] --- Z8[zener]
      Z1 --- R1[Resistor]
      Z2 --- R2[Resistor]
      Z3 --- R3[Resistor]
      Z4 --- R4[Resistor]
      Z5 --- R5[Resistor]
      Z6 --- R6[Resistor]
      Z7 --- R7[Resistor]
      Z8 --- R8[Resistor]
      R1 --- V0[V0]
      R2 --- V0
      R3 --- V0
      R4 --- V0
      R5 --- V0
      R6 --- V0
      R7 --- V0
      R8 --- V0
  
```

C=1.0uF~4.7uF

7 TIMING CHARACTERISTICS

SERIAL INTERFACE (4-Line Interface)

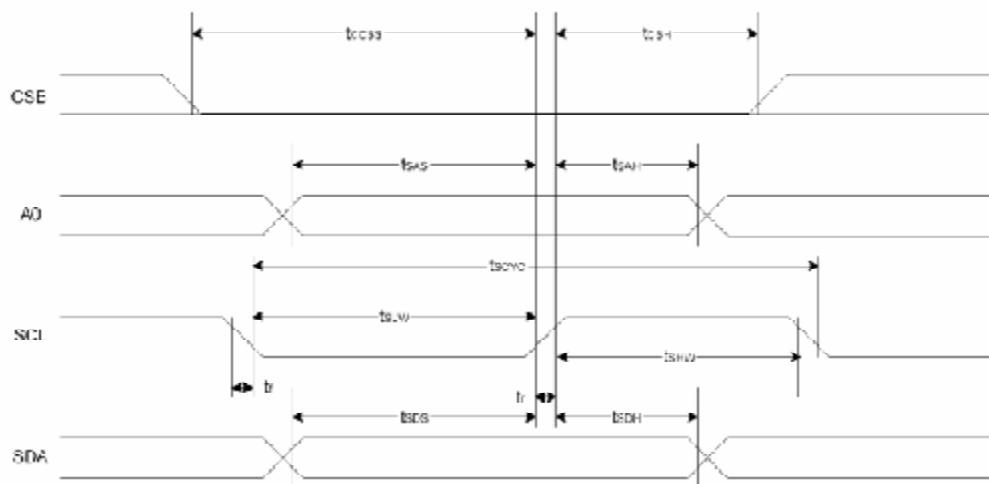


Figure 29

($V_{DD} = 3.3V$, $T_a = -30$ to 85°C)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---------------------|--------|-----------|-----------|--------|------|-------|
| | | | | Min. | Max. | |
| Serial Clock Period | | t_{SCL} | | 100 | -- | |
| SCL "H" pulse width | SCL | t_{SHW} | | 60 | -- | |
| SCL "L" pulse width | | t_{SLW} | | 60 | -- | |
| Address setup time | A0 | t_{SAS} | | 20 | -- | |
| Address hold time | | t_{SAH} | | 80 | -- | ns |
| Data setup time | SDA | t_{SDS} | | 20 | -- | |
| Data hold time | | t_{SDH} | | 20 | -- | |
| CS-SCL time | | t_{CSL} | | 30 | -- | |
| CS-SCL time | CSB | t_{CSH} | | 120 | -- | |

($V_{DD} = 2.7V$, $T_a = -30$ to 85°C)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---------------------|--------|-----------|-----------|--------|------|-------|
| | | | | Min. | Max. | |
| Serial Clock Period | | t_{SCL} | | 120 | -- | |
| SCL "H" pulse width | SCL | t_{SHW} | | 70 | -- | |
| SCL "L" pulse width | | t_{SLW} | | 70 | -- | |
| Address setup time | A0 | t_{SAS} | | 20 | -- | |
| Address hold time | | t_{SAH} | | 100 | -- | ns |
| Data setup time | SDA | t_{SDS} | | 20 | -- | |
| Data hold time | | t_{SDH} | | 20 | -- | |
| CS-SCL time | | t_{CSL} | | 30 | -- | |
| CS-SCL time | CSB | t_{CSH} | | 150 | -- | |

■ RESET TIMING

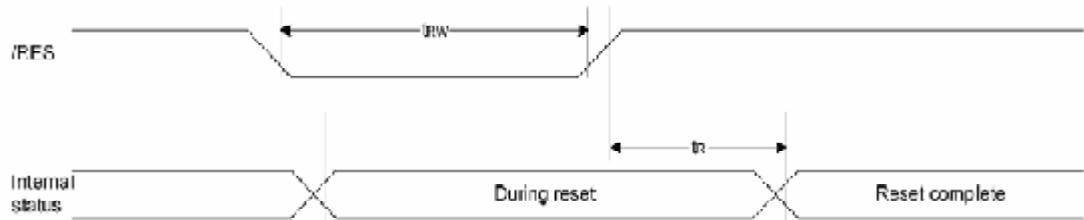


Figure 31

(V_{DD} = 3.3V, T_A = -30 to 85 °C)

| Item | Signal | Symbol | Condition | Rating | | | Units |
|-----------------------|--------|----------------|-----------|--------|------|------|-------|
| | | | | Min. | Typ. | Max. | |
| Reset time | | t _R | | — | — | 400 | ns |
| Reset "L" pulse width | /RES | t _W | | 1200 | — | — | |

(V_{DD} = 2.7V, T_A = -30 to 85 °C)

| Item | Signal | Symbol | Condition | Rating | | | Units |
|-----------------------|--------|----------------|-----------|--------|------|------|-------|
| | | | | Min. | Typ. | Max. | |
| Reset time | | t _R | | — | — | 350 | ns |
| Reset "L" pulse width | /RES | t _W | | 1600 | — | — | |

8 QUALITY AND RELIABILITY

8.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : $25 \pm 5^{\circ}\text{C}$

Humidity : 60 + 25% RH.

8.2 SAMPLING PLAN

Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

8.3 ACCEPTABLE QUALITY LEVEL

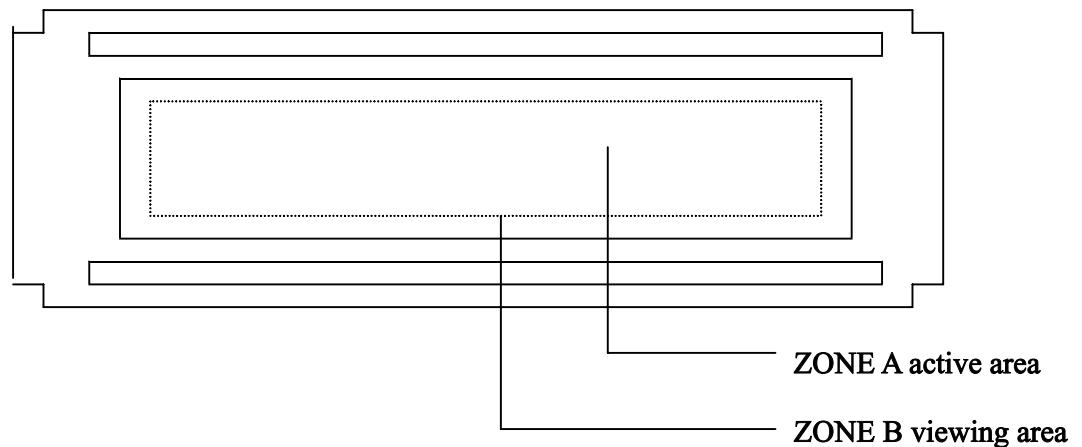
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

8.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.

8.5 INSPECTION QUALITY CRITERIA

| Item | Description of defects | | | Class of Defects | Acceptable level (%) | | |
|----------------------|--|-----------|--------|------------------|----------------------|--|--|
| Function | Short circuit or Pattern cut | | | Major | 0.65 | | |
| Dimension | Deviation from drawings | | | Major | 1.5 | | |
| Black spots | Ave . dia . D | area A | area B | Minor | 2.5 | | |
| | D<0.2 | Disregard | | | | | |
| | 0.2<D<0.3 | 3 | 4 | | | | |
| | 0.3<D<0.4 | 2 | 3 | | | | |
| | 0.4<D | 0 | 1 | | | | |
| Black lines | Width W, Length L | A | B | Minor | 2.5 | | |
| | W<0.03 | disregard | | | | | |
| | 0.03<W≤0.05 | 3 | 4 | | | | |
| | 0.05<W≤0.07 , L≤3.0 | 1 | 1 | | | | |
| | See line criteria | | | | | | |
| Bubbles in polarizer | Average diameter D $0.2 < D < 0.5$ mm for N = 4 , D > 0.5 for N = 1 | | | Minor | 2.5 | | |
| Color uniformity | Rainbow color or newton ring. | | | Minor | 2.5 | | |
| Glass Scratches | Obvious visible damage. | | | Minor | 2.5 | | |
| Contrast ratio | See note 1 | | | Minor | 2.5 | | |
| Response time | See note 2 | | | Minor | 2.5 | | |
| Viewing angle | See note 3 | | | Minor | 2.5 | | |



8.6 RELIABILITY

| Test Item | Test Conditions | | Note |
|----------------------------|---|--|------|
| | Extend Temp. type | | |
| High Temperature Operation | 70±3°C , t=96 hrs | | |
| Low Temperature Operation | -20+3°C , t=96 hrs | | |
| High Temperature Storage | 80±3°C , t=96 hrs | | 1,2 |
| Low Temperature Storage | -30+3°C , t=96 hrs | | 1,2 |
| Thermal Shock Test | -30°C ~ 25°C ~ 80°C 30 m in. 5 min. 30 min. (1 cycle) Total 5 cycle | | 1,2 |
| Humidity Test | 40 °C, Humidity 90%, 96 hrs | | 1,2 |
| Vibration Test (Packing) | Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis | | 2 |

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

9 HANDLING PRECAUTIONS

- (1) A LCD module is a fragile item and should not be subjected to strong mechanical shocks.
- (2) Avoid applying pressure to the module surface. This will distort the glass and cause a change in color.
- (3) Under no circumstances should the position of the bezel tabs or their shape be modified.
- (4) Do not modify the display PCB in either shape or positioning of components.
- (5) Do not modify or move location of the zebra or heat seal connectors.
- (6) The device should only be soldered to during interfacing. Modification to other areas of the board should not be carried out.
- (7) In the event of LCD breakage and resultant leakage of fluid do not inhale, ingest or make contact with the skin. If contact is made rinse immediately.
- (8) When cleaning the module use a soft damp cloth with a mild solvent, such as Isopropyl or Ethyl alcohol. The use of water, ketone or aromatic is not permitted.
- (9) Prior to initial power up input signals should not be applied.
- (10) Protect the module against static electricity and observe appropriate anti-static precautions.

10 OUTLINE DIMENSION

