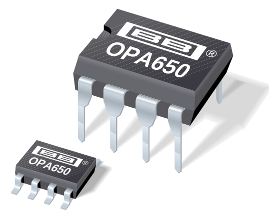


OPA650

Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- LOW POWER: 50mW
- UNITY GAIN STABLE BANDWIDTH: 560MHz
- LOW HARMONICS: –77dBc at 5MHz
- FAST SETTLING TIME: 20ns to 0.01%
- LOW INPUT BIAS CURRENT: 5µA
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.03°
- HIGH OUTPUT CURRENT: 85mA

APPLICATIONS

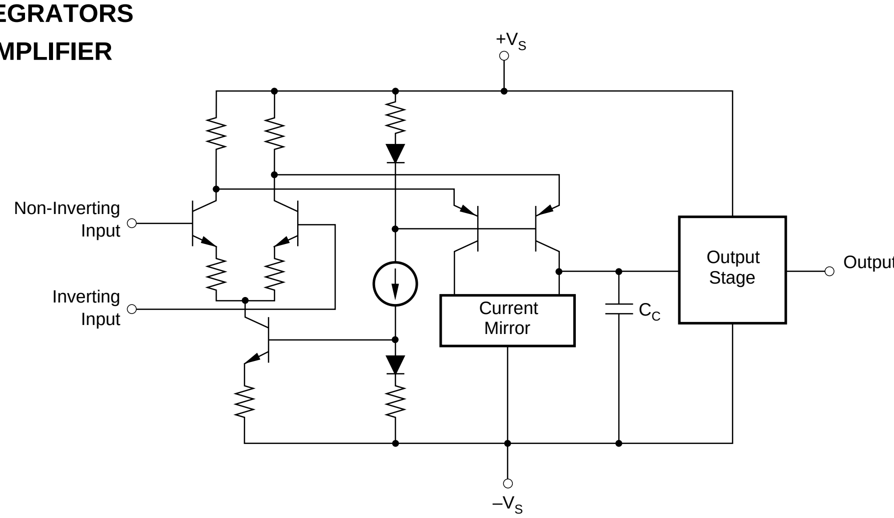
- HIGH RESOLUTION VIDEO
- BASEBAND AMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

DESCRIPTION

The OPA650 is a low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 560MHz as well as a 12-bit settling time of only 20ns. The low distortion allows its use in communications applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its “classical” operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA650 is also available in dual (OPA2650) and quad (OPA4650) configurations.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

 PDS-1264B Printed in U.S.A. September, 1995

SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA650P, U MIN	OPA650P, U TYP	OPA650P, U MAX	OPA650PB, UB MIN	OPA650PB, UB TYP	OPA650PB, UB MAX	UNITS
FREQUENCY RESPONSE								
Closed-Loop Bandwidth(2)	G = +1		560			*(1)		MHz
	G = +2		140			*		MHz
	G = +5		37			*		MHz
	G = +10		18			*		MHz
Gain Bandwidth Product			180			*		MHz
Slew Rate	G = +1, 2V Step		240			*		V/µs
Over Specified Temperature			220			*		V/µs
Rise Time	0.2V Step		1			*		ns
Fall Time	0.2V Step		1			*		ns
Settling Time 0.01%	G = +1, 2V Step		19.6			*		ns
0.1%	G = +1, 2V Step		10.2			*		ns
1%	G = +1, 2V Step		6.3			*		ns
Spurious Free Dynamic Range	G = +1, f = 5.0 MHz, V_O = 2Vp-p							
	R_L = 100Ω		73			*		dBc
	R_L = 200Ω		77			*		dBc
Differential Gain	G = +1, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.01			*		%
Differential Phase	G = +1, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.03			*		Degrees
Bandwidth for 0.1dB Gain Flatness	G = +2		25			*		MHz
INPUT OFFSET VOLTAGE								
Input Offset Voltage			±1	±5		0.6	±2.5	mV
Average Drift			±3			*		µV/°C
Power Supply Rejection (+V_S)	$\|V_S\|$ = 4.5V to 5.5V	60	76		70	*		dB
(–V_S)		47	53		50	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		5	20		*	10	µA
Over Temperature				30			20	µA
Input Offset Current	V_{CM} = 0V		0.5	1		0.2	0.5	µA
Over Temperature				3			2	µA
NOISE								
Input Voltage Noise								
Noise Density, f = 100Hz			43			*		nV/√Hz
f = 10kHz			9.4			*		nV/√Hz
f = 1MHz			8.4			*		nV/√Hz
f = 1MHz to 100MHz			8.4			*		nV/√Hz
Integrated Noise, BW = 10Hz to 100MHz			84			*		µVp-p
Input Bias Current Noise								
Current Noise Density, f = 0.1MHz to 100MHz			1.2			*		pA/√Hz
Noise Figure (NF)								
	R_S = 10kΩ		4			*		dB
	R_S = 50Ω		19.5			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±2.8			*		V
Over Specified Temperature		±2.2			*			V
Common-Mode Rejection	V_{CM} = ±0.5V	65	90		70	*		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		kΩ || pF
Common-Mode			16 || 1			*		MΩ || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	45	51		46	*		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	43			44			dB
OUTPUT								
Voltage Output								
Over Specified Temperature	No Load	±2.2	±3.0		±2.4	*		V
	R_L = 250Ω	±2.2	±2.5		±2.4	*		V
	R_L = 100Ω	±2.0	±2.3		±2.2	*		V
Current Output, Sourcing		75	110		*	*		mA
Over Specified Temperature		65			*			mA
Current Output, Sinking		65	85		*	*		mA
Over Specified Temperature		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	0.1MHz, G = +1		0.08			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Derated Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current			±5.1	±7.75		±5.1	±6.5	mA
Over Specified Temperature				±8.75			±7.5	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P			100			*		°C/W
U			125			*		°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Frequency response can be strongly influenced by PC board parasitics. The OPA650 is nominally compensated assuming 2pF parasitic load. The demonstration board, DEM-OPA65xP, shows a low parasitic layout for this device.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5V
Internal Power Dissipation	See Thermal Conditions
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA650U, UB	SO-8 Surface Mount	182
OPA650P, PB	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

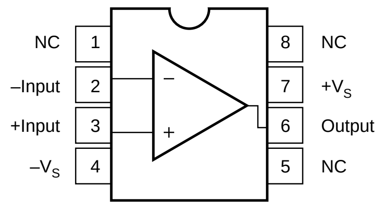
ORDERING INFORMATION(1)

MODEL	PACKAGE	TEMPERATURE RANGE
OPA650U, UB	SO-8 Surface Mount	–40°C to +85°C
OPA650P, PB	8-Pin Plastic DIP	–40°C to +85°C

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by pin 8. Refer to mechanical section for the location.

PIN CONFIGURATION

Top View DIP/SO-8



ELECTROSTATIC DISCHARGE SENSITIVITY

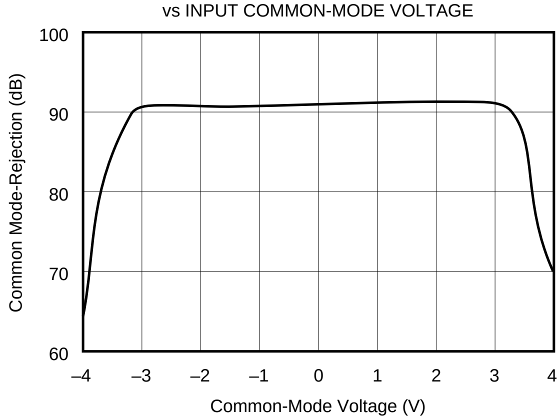
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

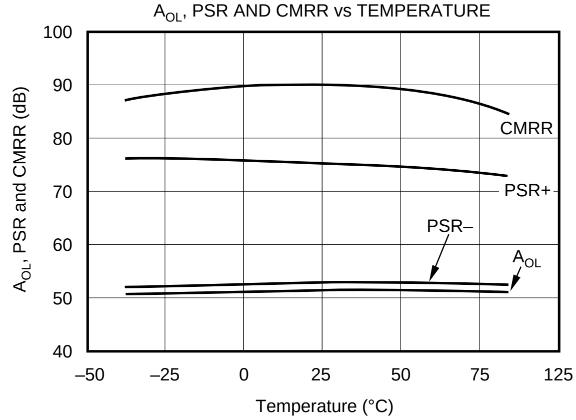
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for Gain of +1.

COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE

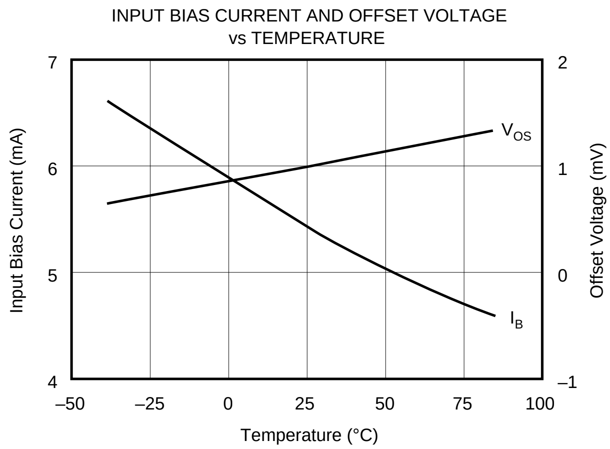


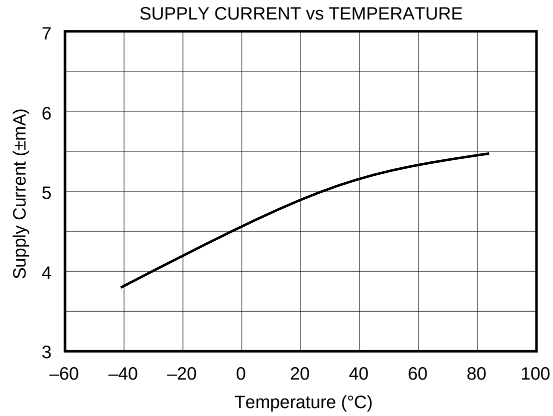
A_{OL}, PSR AND CMRR vs TEMPERATURE

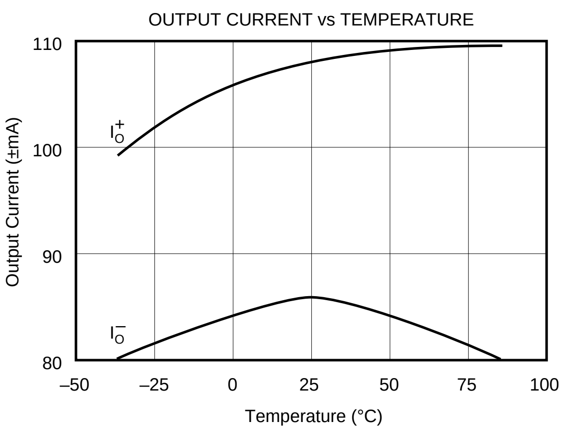


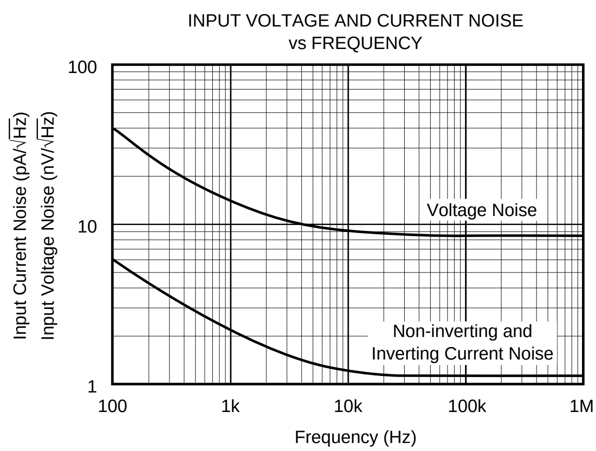
TYPICAL PERFORMANCE CURVES (CONT)

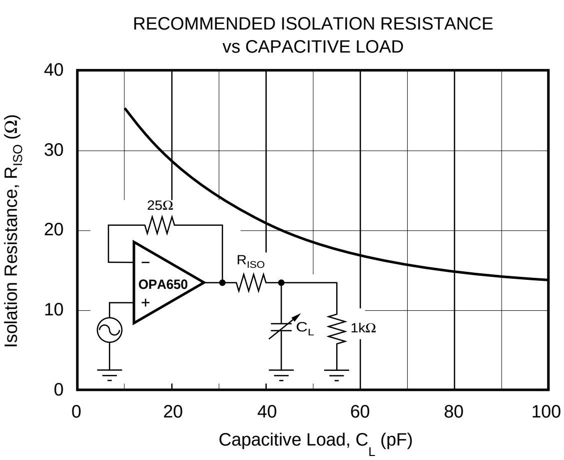
$T_A = +25°C$, $V_S = ±5V$, $R_L = 100\Omega$, and $R_{FB} = 402\Omega$ unless otherwise noted. $R_{FB} = 25\Omega$ for Gain of +1.

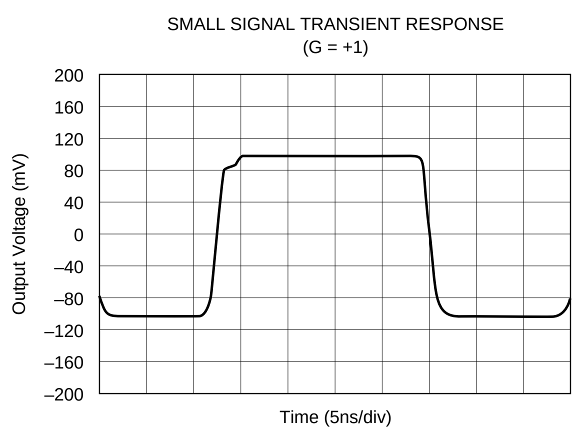








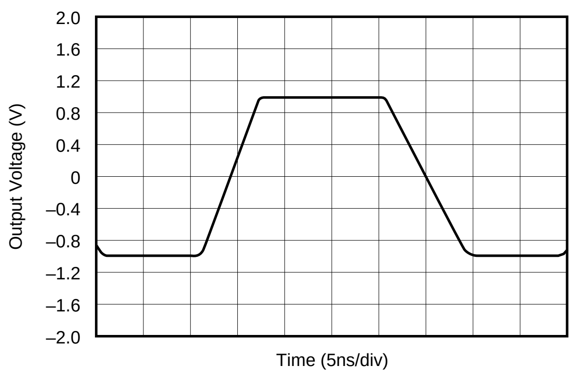




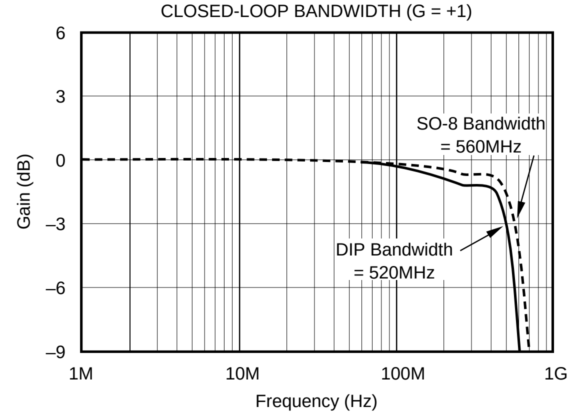
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for Gain of +1.

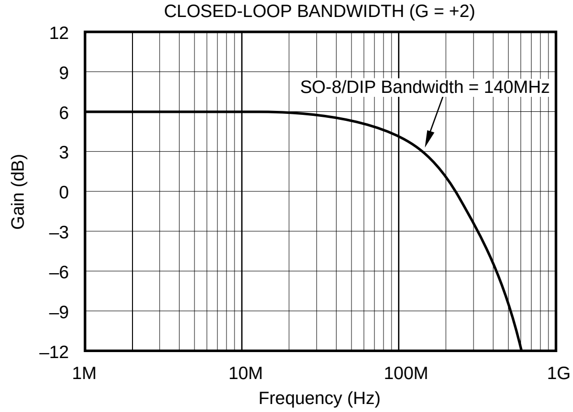
LARGE SIGNAL TRANSIENT RESPONSE (G = +1)



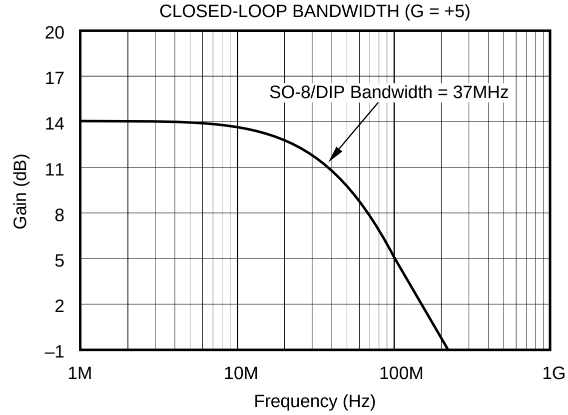
CLOSED-LOOP BANDWIDTH (G = +1)



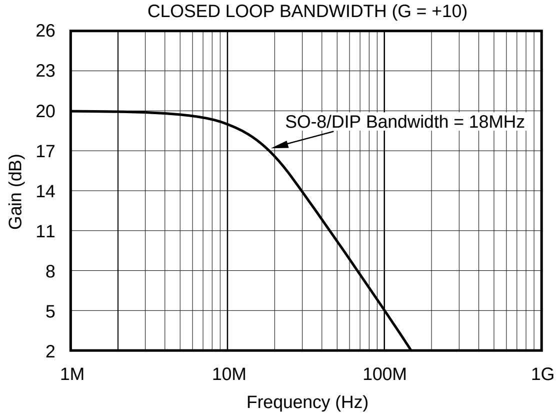
CLOSED-LOOP BANDWIDTH (G = +2)



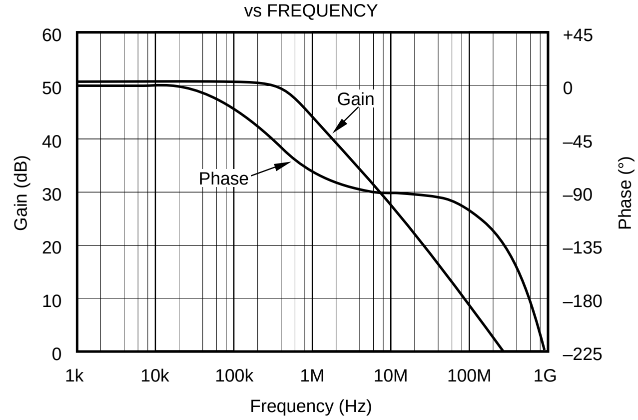
CLOSED-LOOP BANDWIDTH (G = +5)



CLOSED LOOP BANDWIDTH (G = +10)

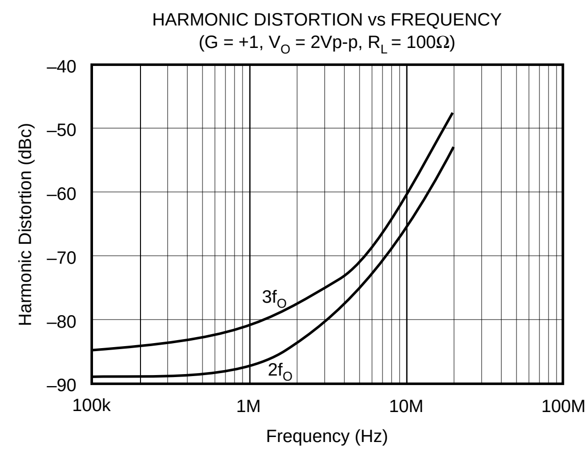


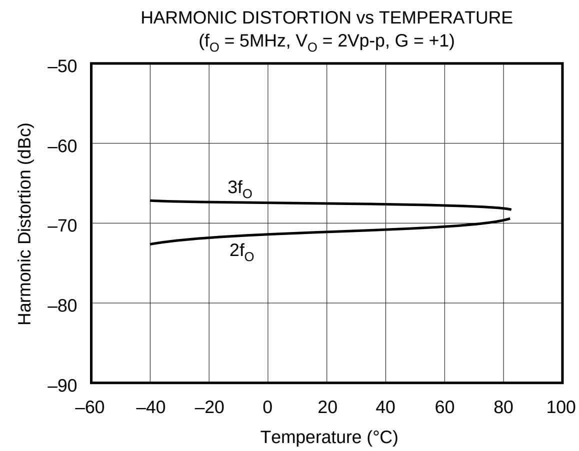
OPEN-LOOP GAIN AND PHASE vs FREQUENCY

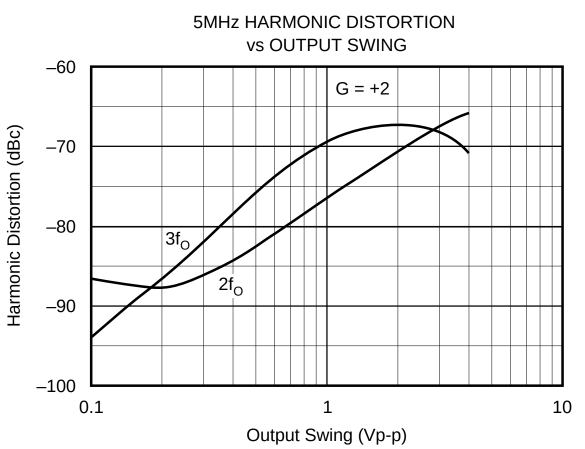


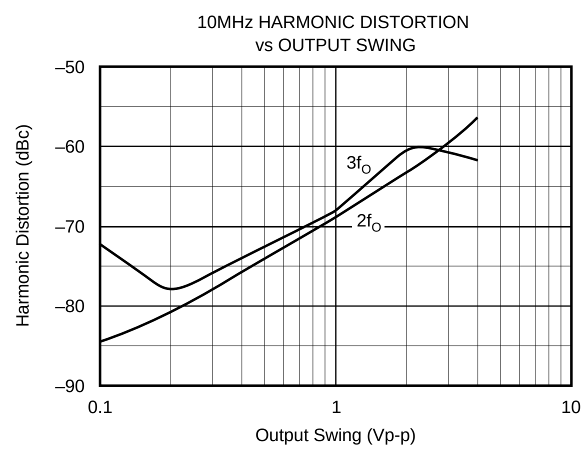
TYPICAL PERFORMANCE CURVES (CONT)

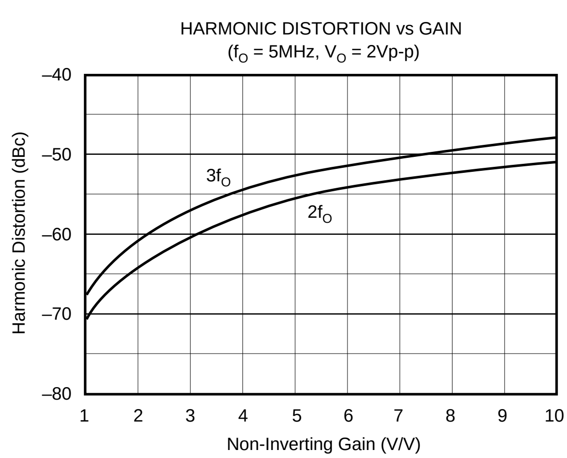
T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for Gain of +1.











DISCUSSION OF PERFORMANCE

The OPA650 is a low power, wideband voltage feedback operational amplifier. Each channel is internally compensated to provide unity gain stability. The OPA650's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA650 well suited for implementing filter and instrumentation designs. The OPA650's AC performance is optimized to provide a gain bandwidth product of 180MHz and a fast 0.1% settling time of 10.2ns, which is an important consideration in high speed data conversion applications. Along with its excellent settling characteristics, the low DC input offset of ±1mV and drift of ±3µV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the current feedback OPA658.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high frequency amplifier like the OPA650 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA650. Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as non-inverting input termination resistors, should also be placed close to the package.

Even with a low parasitic capacitance shunting external resistors, excessively high resistor values can create significant time constants and degrade performance. Good metal film or surface mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this adds a pole and/or zero below 500MHz that can affect circuit operation. Keep resistor values as low as possible consistent with output loading considerations. The 402Ω feedback used for the Typical Performance Plots is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for a unity gain follower. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA650 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high speed part like the OPA650 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

The OPA650 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single supply operation. Figure 1 shows one approach to single-supply operation.

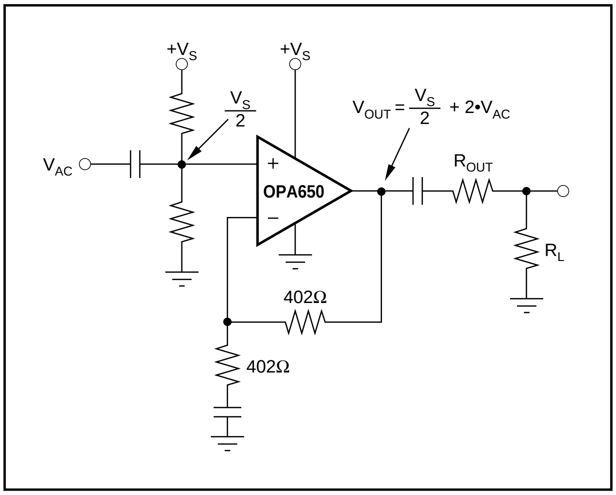


FIGURE 1. Single Supply Operation.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 2 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.

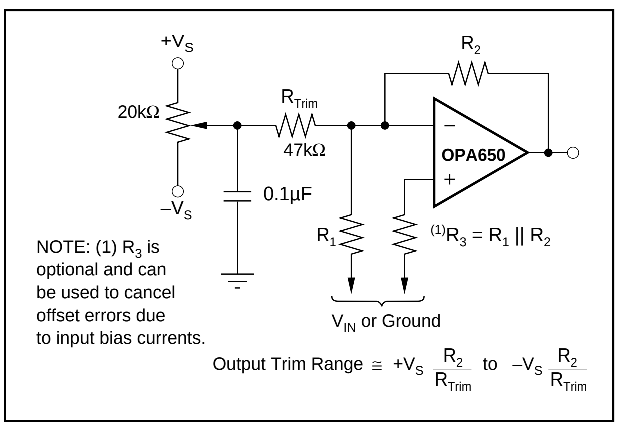


FIGURE 2. Offset Voltage Trim.

ESD PROTECTION

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA650.

OUTPUT DRIVE CAPABILITY

The OPA650 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive a 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA650 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as driving A/D converters require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA650 maintains very low-closed loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing.

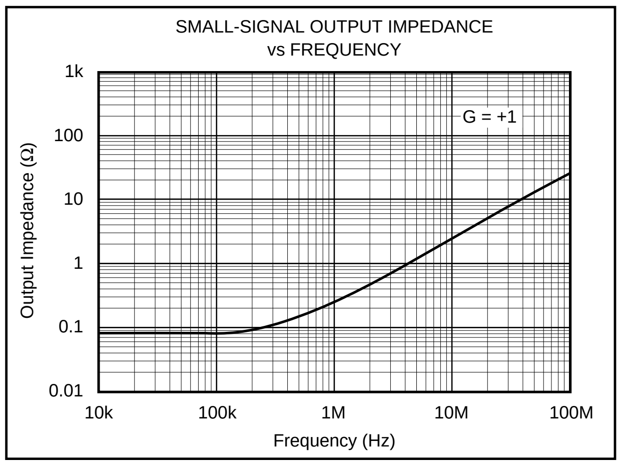


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA650 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D\theta_{JA}$. The total internal power dissipation (P_D) is a combination of the total quiescent power (P_{DQ}) and the power dissipated in of the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is a fixed DC voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \cdot R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for an OPA650U at $A_V = +2$, $R_L = 100\Omega$, $R_{FB} = 402\Omega$, $\pm V_S = \pm 5V$, with the output at $|V_S/2|$, and the specified maximum $T_A = +85°C$. $P_D = 10V \cdot 8.75mA + (5^2)/(4 \cdot (100\Omega \| 804\Omega)) = 158mW$. Maximum $T_J = +85°C + 0.158W \cdot 125°C/W = 105°C$.

DRIVING CAPACITIVE LOADS

The OPA650's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be isolated by connecting a small resistance, usually 15Ω to 30Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

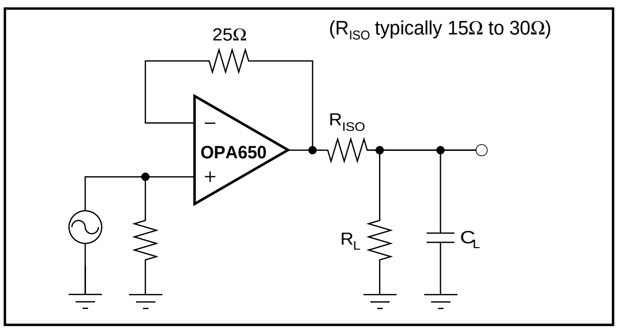


FIGURE 4. Driving Capacitive Loads.

FREQUENCY RESPONSE COMPENSATION

The OPA650 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain greater than one to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Frequency response for other gains are shown in the Typical Performance Curves.

The high frequency response of the OPA650 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high-frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee-network) is recommended to avoid using large value resistors with large time constants.

PULSE SETTLING TIME

High speed amplifiers like the OPA650 are capable of extremely fast settling time with a pulse input. Excellent frequency response flatness and phase linearity are required to get the best settling times. As shown in the specifications table, settling time for a ±1V step at a gain of +1 for the OPA650 is extremely fast. The specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 2V step, 1% settling corresponds to an error band of ±20mV, 0.1% to an error band of ±2mV, and 0.01% to an error band of ±0.2mV. For the best settling times, particularly into an ADC capacitive load, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to ground return currents in the supply decoupling capacitors. For highest performance, consider the OPA642 which isolates the output stage decoupling from the rest of the amplifier.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. The percentage change in closed-loop gain over a specified change in output voltage level is defined as DG. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. DG and DP are both specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA650's harmonic distortion characteristics into a 100Ω load are shown versus frequency and power output in the typical performance curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 5. Remember to include the contribution of the feedback network when calculating the effective load resistance seen by the amplifier.

NOISE FIGURE

The OPA650 voltage noise spectral density is specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA650's Noise Figure vs Source Resistance is shown in Figure 6.

SPICE MODELS AND EVALUATION BOARD

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models and evaluation PC boards (DEM-OPA65xP) are available for the OPA650. Contact the Burr-Brown Applications Department to receive a SPICE diskette.

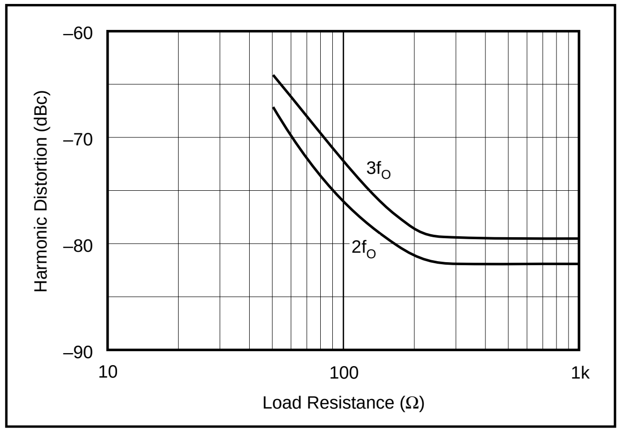


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

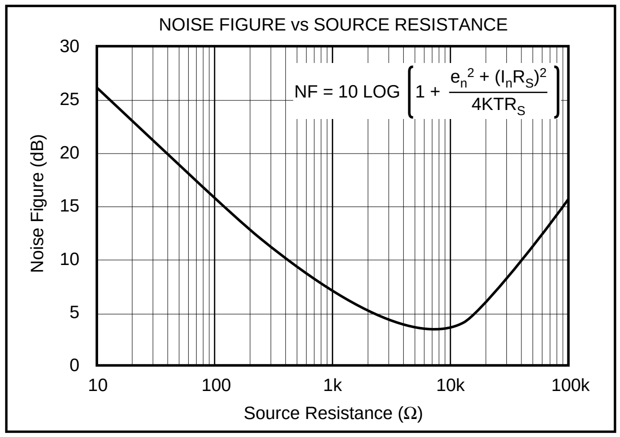


FIGURE 6. Noise Figure vs Source Resistance.

TYPICAL APPLICATION

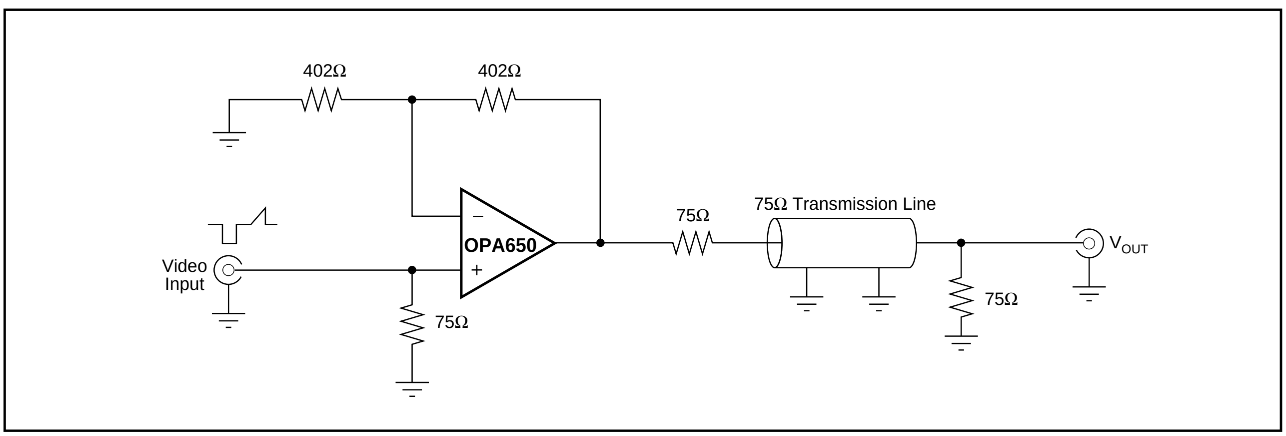
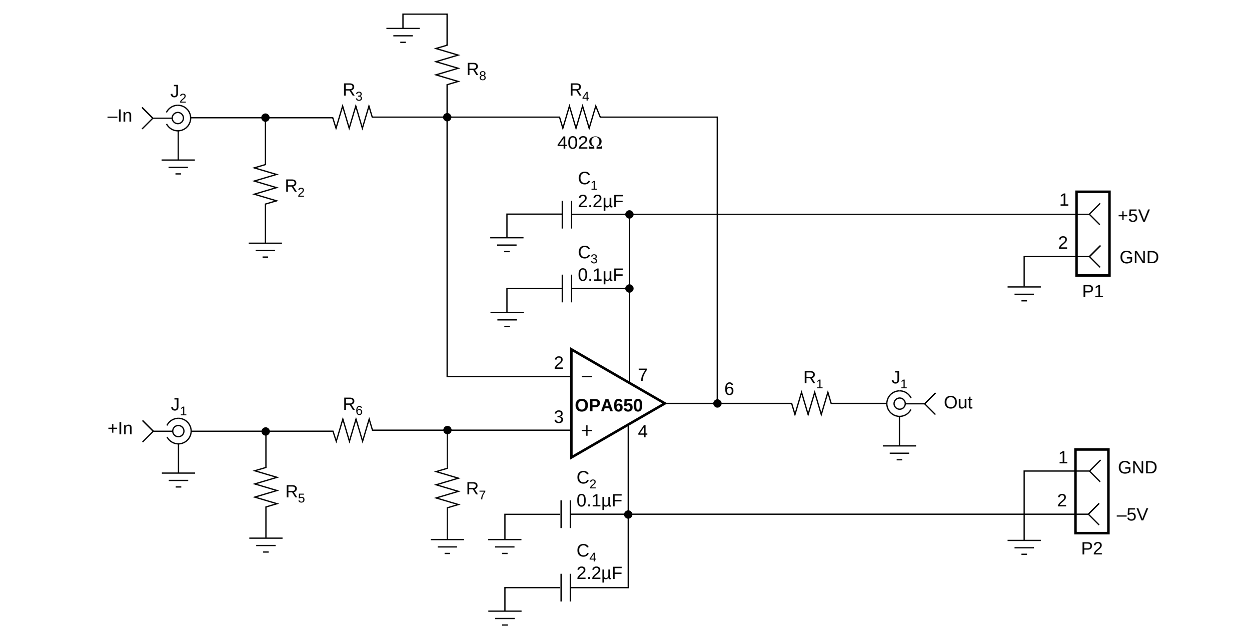


FIGURE 7. Low Distortion Video Amplifier.



NOTE: Values for R_1, R_3, R_5, R_6, and R_7 are chosen according to desired gain.

FIGURE 8. Layout Detail For DEM-OPA65X Demonstration Board.

DEM-OPA65XP Demonstration Board Layout

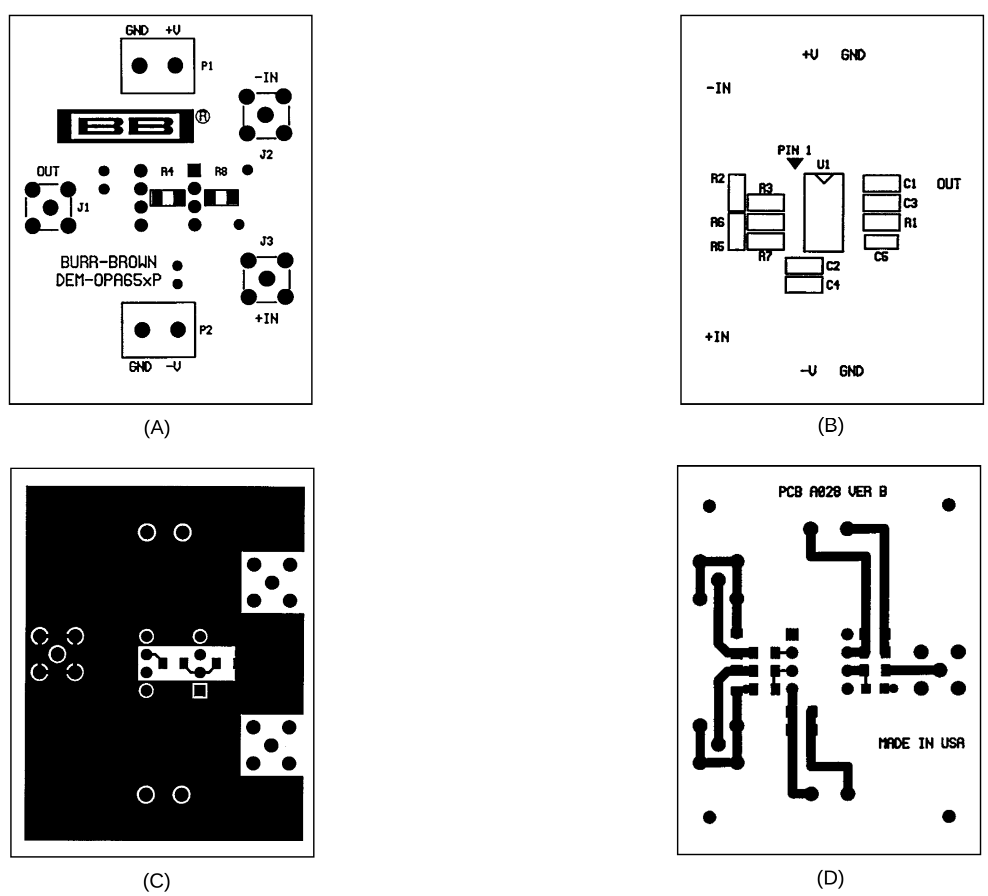
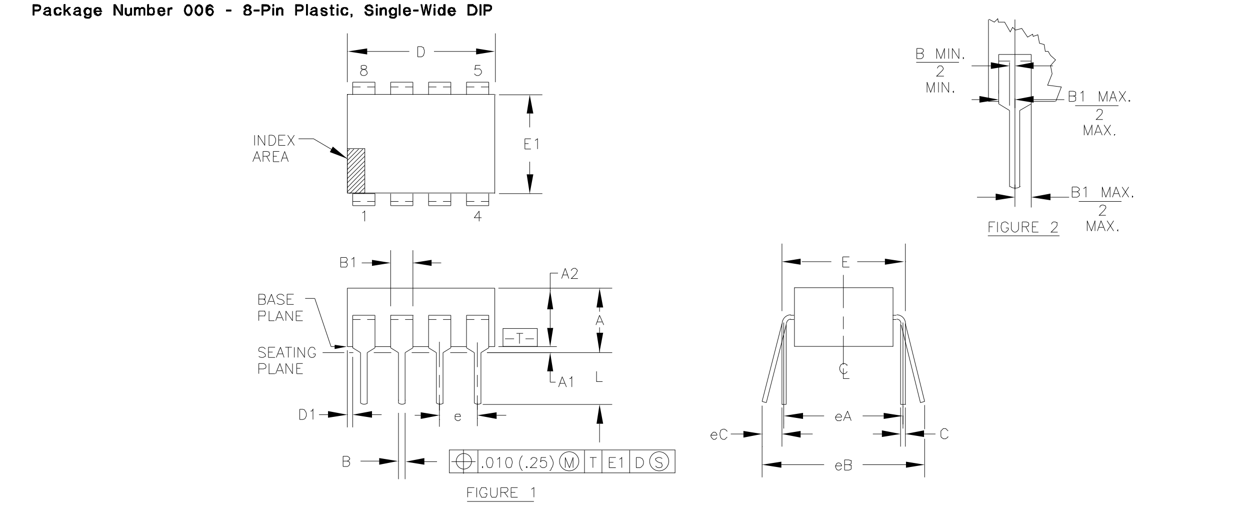


FIGURE 9a. Evaluation Board Silkscreen (Bottom). 9b. Evaluation Board Silkscreen (Top). 9c. Evaluation Board Layout (Solder Side). 9d. Evaluation Board Layout (Layout Side).

PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



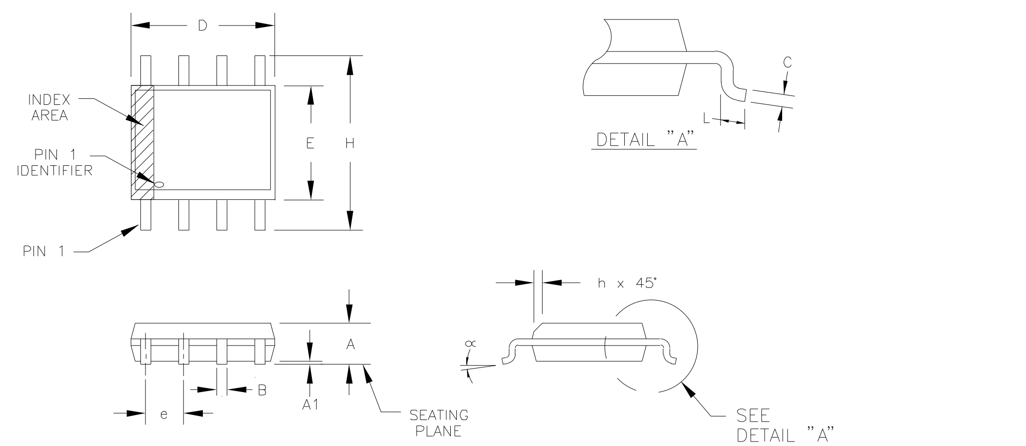
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3	N	8		8		7
A1	.015	--	0.38	--	3						
A2	.115	.195	2.92	4.95							
B	.014	.022	0.36	0.56							
B1	.045	.070	1.14	1.78							
C	.008	.015	0.20	0.38							
D	.348	.430	8.84	10.92	4						
D1	.005	--	0.13	--							
E	.300	.325	7.62	8.26	5						
E1	.240	.280	6.10	7.11	4						
e	.100 BASIC		2.54 BASIC								
eA	.300 BASIC		7.63 BASIC		5						
eB	--	.430	--	10.92	6						
L	.115	.160	2.92	4.06	3						

NOTES:

1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 4, 5, AND 8) MAY BE CONFIGURED AS SHOWN IN FIGURE 2.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 REV.: D
JEDEC NUMBER: MS–001

Package Number 182 - 8-Lead SO-8 Surface Mount



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE	DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.054	.068	1.37	1.73							
A1	.004	.009	0.10	0.23							
B	.014	.019	0.36	0.48							
C	.008	.0098	0.20	0.25							
D	.189	.196	4.80	4.98							
E	.150	.157	3.81	3.99							
e	.050 BASIC		1.27 BASIC								
H	.229	.244	5.82	6.20							
h	.010	.019	0.25	0.48							
L	.016	.050	0.41	1.27							
N	8		8								
∝	0°	8°	0°	8°							

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5–1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.086 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 REV.: F
JEDEC NUMBER: MS–012