MAXIM

ERRATA SHEET
DS1265W

_____ *Revision B Errata*

The errata listed below describe situations where DS1265W revision B modules perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata in subsequent die revisions.

*This errata sheet only applies to DS1265W revision B modules. Revision B components are branded on the topside of the package with a six-digit code in the form yywwBx, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and the x is an alphabetic character identifying the internal static memory components. To obtain an errata sheet on another DS1265W die revision, visit our website at **www.maxim-ic.com/errata**.*

1) ADDRESS SETUP TIME

Description:
If the delay between valid address and $\overline{WE}$ (write enable) falling edge (t_{AW}) is less than 10ns, the DS1265W may not work correctly.

Workaround:
Allow at least 10ns (t_{AW}) delay between presentation of the address to the falling edge of $\overline{WE}$.