DS21554/DS21Q554
5V E1 Single-Chip Transceivers

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REVISION A4 ERRATA

The errata listed below describe situations where DS21554/DS21Q554 revision A4 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS21554/DS21Q554 revision A4 components. Revision A4 components are branded on the top side of the package with a six-digit code in the form yyww A4, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. The die revision can also be determined through the lower four bits of the IDR register at location 0Fh. To obtain an errata sheet on another DS21554/DS21Q554 die revision, visit our website at www.maxim-ic.com/errata.

1. TRANSMIT AND RECEIVE SIGNALING BUFFERS DO NOT OPERATE CORRECTLY IF INTERLEAVED BUS OPERATION (IBO) IS ENABLED

Description:
If IBOP is enabled, hardware signaling using the TSIG and RSIG pins is not available. The receive-signaling change (RSC) interrupt does not operate, and signaling reinsertion in the receive path is nonfunctional.

Work Around:
Do not use hardware signaling in IBO mode. Other functionality associated with IBO is still available. The device will correctly interleave the serial data streams at RSER, and signaling is available in the receive-signaling registers. Changes in signaling states can still be identified in software by reading the receive-signaling registers each multiframe and comparing the contents with the previous multiframe of signaling.

2. IT IS POSSIBLE FOR THE 8MCLK PIN TO OUTPUT 24.576MHz ON POWER-UP

Description:
It is possible for the 8MCLK pin to output 24.576MHz on power-up.

Work Around:
To avoid this situation, reset the PLL by writing a 01h into location ACh. After 1ms, clear the reset bit by writing a 00h into location Ach.

3. DURING JTAG OPERATION, THE JTDO PIN WILL TRANSITION ON THE FALLING EDGE OF JTCLK

Description:
The JTDO pin transitions with the falling edge of JTCLK, rather than with the next rising edge.

Work Around:
To remove the possibility of misinterpretation of the data output, it is recommended that a 0.001µF capacitor be placed from JTDO to ground.

4. EQUALIZER GAIN LIMIT

Description:
When using the equalizer gain limit (EGL) function (bit LICR.4 = 0), the receiver may squelch an input signal with more than -7.5dB of attenuation.

Work Around:
For signals in the -7.5dB to -12dB range, set the EGL bit to 1. No other known work around exists for this erratum.

5. NEW FEATURE ADDED IN REVISION B1

Description:
The receive monitor mode included in the released data sheet became an official feature with the B1 die revision. This feature was purposefully omitted from prior versions of the data sheet because the mode was experimental, and early revisions of the device did not meet the intended objectives. Once the B1 revision had been evaluated and found to function properly, the feature was added to the data sheet.

Work Around:
None.

6. INCORRECT ERROR COUNT REPORTED IN ERROR-COUNT REGISTERS

Description:
The error-count registers may report an error count that is one error higher than the actual error count, which is due to a potential internal collision at the one-second timer boundary during data transfer from the error counter to the error-count register. The actual error count internal to the part will be accurate in this situation and all resync criteria will be followed correctly, but the error-count registers may report an error count that is one error higher than the actual error count.

Work Around:
None.

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