DS21Q50
Quad E1 Single-Chip Transceiver

www.maxim-ic.com

REVISION A1 ERRATA

The errata listed below describe situations where DS21Q50 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS21Q50 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. The die revision can also be dtermined through the lower four bits of the IDR register at location 0Fh. These four bits contain "0000" on A1 revision devices. To obtain an errata sheet on another DS21Q50 die revision, visit our website at www.maxim-ic.com/errata or contact technical support at telecom.support@dalsemi.com.

1. 16MHz INTERLEAVE BUS OPERATION REQUIRES TIMING ADJUSTMENTS TO COORDINATE CLOCK AND DATA

Description:
In 16MHz interleaved bus operation (IBO), the timing of the clock and data signals requires modification to correctly interpret the data stream. The 8MHz IBO operation is unaffected by this condition.

Work Around:
Please contact telecom.support@dalsemi.com for more details on the modifications required.

2. LINE BUILD-OUT SETTING "120Ω WITH HIGH RETURN LOSS" DOES NOT MEET TEMPLATE

Description:
The output waveform of the line build-out selected by LICR bit settings L2 = 1, L1 = 0, and L0 = 1 does not meet specifications and should not be used.

Work Around:
There is no known work around for this erratum.

3. RECEIVER INITIALIZATION

Description:
The receiver requires a test mode setting to ensure proper operation.

Work Around:
Program a value of B0h to address location 1Fh to properly initialize the receiver.