DS26401
Octal T1/E1/J1 Framer

REVISION A1 ERRATA

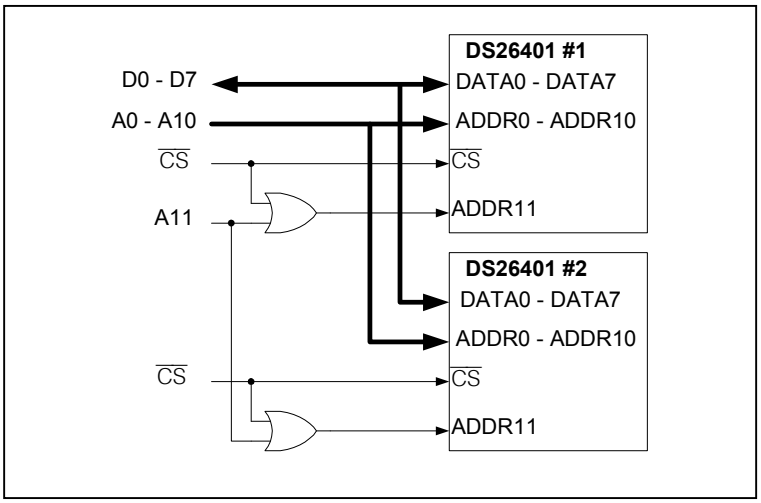
The errata listed below describe situations where DS26401 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26401 revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS26401 die revision, visit our website at www.maxim-ic.com/errata or contact technical support at telecom.support@dalsemi.com.

1. GLOBAL ADDRESS SPACE NOT BLOCKED WITH $\overline{CS}$

Description:
The Global Registers in address space 0x0F0-0x0FF are not gated with $\overline{CS}$. Write operations to other devices on the bus at these addresses 0x0F0 and 0x0F1 will affect the GCR1 and GCR2 registers. There are also unused registers in this space that must remain at 0x00 for proper operation.

Hardware-Based Work Around:
OR the ADDR[11] input with $\overline{CS}$ to ensure that ADDR[11] is a logical 1 when the DS26401 is not being accessed.



Software-Based Work Around:
Access the DS26401 with Motorola timing; use Intel timing to access other devices on the parallel bus.

2. FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE

Description:
The DS26401 does not correctly identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS26401 will not report the LFA alarm when the Japanese JT-G704 LFA pattern of '11111111 11111111' is present in the facilities data link. The DS26401 will only respond to the normal G.704 LFA pattern of '11111111 00000000.'

Work Around:
To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to a 0. The TFDLS bit is located in the TCR2 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly and an update is indicted by the RFDLF status bit. The RFDL status bit is located in the RLS7 register. Since the Japanese ESF LFA alarm pattern is 2 bytes long, the RFDL register has to be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm is active, and will remain active until 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, at which point the alarm will become deactive.