DS26502
T1/E1/J1/64KCC BITS Element

REVISION A2 ERRATA

The errata listed below describe situations where DS26502 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26502 revision A2 components. Revision A2 components are branded on the top side of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS26502 die revision, visit our website at www.maxim-ic.com/errata.

1. TRANSMIT OPEN-CIRCUIT DETECT STATUS BIT IS NOT FUNCTIONAL IN COMPOSITE CLOCK MODE

Description:
The transmit open-circuit detect status bit (TOCD) in SR1.1 is not functional in composite clock mode. This bit will always be 0 when operating in composite clock mode.

Work Around:
None.

2. TCLKO OUTPUT PIN IS NOT FUNCTIONAL IN 6312kHz CLOCK MODE

Description:
The Transmit Clock Output pin TCLKO is not functional in the Transmit 6312kHz clock mode (TMODE[3:0] = 1011). When in 6312kHz clock mode, this pin will be driven low and will not output the intended transmit clock frequency as selected by the TCSS1 and TCSS0 bits in the Transmit PLL Control Register (TPCR.1 and TPCR.0).

Work Around:
The intended functionality of TCLKO in 6312kHz mode can be achieved by configuring the part as shown when operating in software mode. This will allow the user to output the intended 6312kHz clock frequency on TCLKO.

1) Set the transmit mode to 64kHz + 8kHz Synchronization mode (set TMODE[3:0] = 1001).
2) Power down the line side transmitter pins (set TPD = 0 in LIC1).
3) Configure TSYNCIO as an input pin in order to keep the part from transmitting a sync pulse (set TSIO = 0 in IOCR1).
4) Select the PLL_CLK as the transmit clock source (set TCSS1 = 0, TCSS0 = 1 in the Transmit PLL Control Register (TPCR).
5) Select the PLL_CLK frequency to be 6312kHz (set TPLLOFS[1:0] = 11 in TPCR).
6) Set the PLL_CLK source (set TPLLSS in TPCR) correctly for the given application.

There is no direct work around if the part is used in Hardware Mode. The PLL_OUT pin can be configured in Hardware Mode to output the 6312kHz clock frequency, however this should not be tied directly to TCLKO as TCLKO could still be driven by the part.

3. TEST1 AND TEST0 BITS DO NOT FUNCTION AS STATED IN THE DATA SHEET

Description:
The TEST1 and TEST0 bits (TSTRREG.5 and TSTRREG.4) do not function as indicated in the data sheet. These bits are intended to allow the user to force all output and I/O pins to a known state, either all high, all low, or tri-state. In some operating modes, the function of these bits is suppressed by the operating mode that the part is configured for, so that any output pins that are tri-stated based on the operating mode selected are still tri-stated regardless of the setting of the TEST1 and TEST0 bits. The affected operating modes and the associated pins are shown in the table below. The pins shown in the table will not be forced into the state indicated by the TEST1 and TEST0 bits and will instead remain tri-stated.

Table 1. Pins That Do Not Function According to the Settings of TEST1 and TEST0

RMODE3	RMODE2	RMODE1	RMODE0	RECEIVE PATH OPERATING MODE	AFFECTED PINS
0	0	0	0	T1 D4	400HZ
0	0	0	1	T1 ESF	400HZ
0	0	1	0	J1 D4	400HZ
0	0	1	1	J1 ESF	400HZ
0	1	0	0	E1 FAS	400HZ
0	1	0	1	E1 CAS	400HZ
0	1	1	0	E1 CRC4	400HZ
0	1	1	1	E1 CAS and CRC4	400HZ
1	0	0	0	E1 G.703 2048kHz Synchronization Interface	400HZ
1	0	0	1	64kHz + 8kHz Synchronization Interface	400HZ, RSER, RAIS
1	0	1	0	64kHz + 8kHz + 400Hz Synchronization Interface	RSER, RAIS
1	0	1	1	6312kHz Synchronization Interface	400HZ, RS_8K, RLOF, RSER, RAIS
1	1	0	0	Reserved	—
1	1	0	1	Reserved	—
1	1	1	0	Reserved	—
1	1	1	1	Reserved	—

Work Around:
None.

4. RLOF MAY FUNCTION INCORRECTLY WHEN THE PART IS CONFIGURED IN 64kHz + 8kHz + 400Hz SYNCHRONIZATION INTERFACE MODE

Description:
When the receive path is configured for 64kHz + 8kHz + 400Hz Synchronization Interface mode (RMODE[3:0] = 1010b) and a receive loss of frame (RLOF) event occurs because the 400Hz indication is missing or late, RLOF may be prematurely de-asserted before the actual RLOF event has been cleared. The 400Hz boundary is indicated by the absence of an 8kHz bipolar violation (BPV). If a BPV is present at the 400Hz location and it is negative, the RLOF indication will only stay asserted for 125μs, at which time it will become de-asserted until another violation occurs. However, if the BPV is positive, RLOF will function properly and stay asserted until correct framing of the 400Hz signal is re-established.

Work Around:
None.

5. RS_8K AND 400HZ PINS DO NOT FUNCTION PROPERLY WHEN THE RECEIVE PATH IS SET TO EITHER COMPOSITE CLOCK MODE AND LOCAL LOOPBACK IS ENABLED

Description:
When local loopback is enabled (LBCR.3 = 1) and the receive path is configured for either of the composite clock modes (RMODE[3:0] = 1001b or 1010b), the RS_8K and 400HZ pins are not functional and will not output an 8kHz pulse or a 400Hz pulse, respectively.

Work Around:
None.

6. THE SYNCHRONIZATION SIGNALS RS_8K AND 400Hz OCCUR 15.625µs EARLY WHEN THE RECEIVE PATH IS CONFIGURED TO OPERATE IN COMPOSITE CLOCK MODE

Description:
The RS_8K and 400Hz synchronization signals occur 15.625µs early (one 64kHz clock cycle) when the part is configured for either of the receive composite clock modes (RMODE[3:0] = 1001b or 1010b). If the receive path is configured for 64kHz + 8kHz operation, the 8kHz synchronization pulse will occur one 64kHz clock cycle early. If the receive path is configured for 64kHz + 8kHz + 400Hz operation, both the 8kHz and the 400Hz synchronization pulses will occur one 64kHz clock cycle early.

Work Around:
None.

7. T1 AND E1 TRANSMIT WAVEFORMS MAY NOT BE CENTERED IN THEIR RESPECTIVE TEMPLATES AND MAY FAIL TEMPLATE COMPLIANCE IN CERTAIN LINE BUILD-OUTS

Description:
When the transmit path is configured in certain T1 or E1 line build-outs (LBOs), the transmit waveform may fail template compliance or the transmit waveform may not be centered in the corresponding template. To center the waveforms, several factory test registers should be set as shown below. The setting is also dependent on the use of the automatic gain controller (AGC) and the use of the impedance matching (IM) feature.

Work Around:
In order to center the transmit waveforms, set the factory test registers as shown. This work around is not available in hardware mode.

MODE	AGC	IM	ADDRESS	VALUE
T1 LBO1	On	On or Off	F1h	0Ah
T1 LBO2	On	On or Off	F1h	0Ah
T1 LBO3	On	On or Off	F1h	0Ah
T1 LBO4	On	On or Off	F1h	0Ah
E1 LBO0	On or Off	Off	F1h F2h	20h 08h
E1 LBO0	On or Off	On	F1h	20h
E1 LBO1	On	On or Off	F1h	20h
E1 LBO5	On	On or Off	F1h	20h

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