DS26518
Octal T1/E1/J1 Transceiver

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REVISION A1 ERRATA

The errata listed below describe situations where DS26518 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26518 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS26518 die revision, visit our website at www.maxim-ic.com/errata.

1. RECEIVE LOOP CODE STATUS BITS

Description:
Receive loop code status bits do not work in DS26518 Rev A1. The following bits are incorrect:

BIT LOCATION	BIT NAME	BIT DESCRIPTION
RRTS3.0	LUP	Loop-Up Code Detected Condition
RRTS3.1	LDN	Loop-Down Code Detected Condition
RRTS3.2	LSP	Spare Code Detected Condition
RLS3.0	LUPD	Loop-Up Code Detected Condition Detect
RLS3.1	LDND	Loop-Down Code Detected Condition Detect
RLS3.2	LSPD	Spare Code Detected Condition Detect
RLS3.4	LUPC	Loop-Up Code Detected Condition Clear
RLS3.5	LDNC	Loop-Down Code Detected Condition Clear
RLS3.6	LSPC	Spare Code Detected Condition Clear

Work Around:
Use the internal BERT to detect loop codes. Configure the internal BERT to detect a repetitive pattern for the loop code. Map all the receive data bits to the internal BERT (unframed mode). Loop code is detected when the BERT pattern matches and the BERT bit-error rate is less than 10%.

Transmit loop codes work correctly.

2. AUTOMATIC RAI INSERTION

Description:
When automatic RAI insertion is enabled, the RAI is not automatically inserted if CRC-4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC-4 is enabled).

Work Around:
Monitor the CRC-4 sync counter bits (RRTS7.[7:3]) in register E1RRTS7 (Receive Real-Time Status Register 7—E1 Mode). If CSC count value exceeds 16, manually transmit the RAI alarm via the alarm bit (E1TNAF.5) in the Transmit Non-Align Frame register (E1TNAF). If CRC-4 sync is found, stop the alarm via the E1TNAF alarm bit.

3. RECEIVE FRAMER SOFT RESET

Description:
The receive framer soft reset bit (SFTRST.1 in the RMMR register) does not work.

Work Around:
Disable the port using the frame-enable bit (FRM_EN.7 in the RMMR register). Write 00 to all addresses in the framer span. Then write FF to latched status addresses in framer span.

4. TRANSMIT FRAMER SOFT RESET

Description:
The transmit framer soft reset bit (SFTRST.1 in the TMMR register) does not work.

Work Around:
Disable the port using the frame-enable bit (FRM_EN.7 in TMMR register). Write 00 to all addresses in the framer span. Then write FF to latched status addresses in framer span.

5. E1 AUTO RESYNC

Description:
E1 auto resync does not work.

Work Around:
Disable auto resync (SYNCE.1 in the RCR1 register). Monitor FAS resync criteria (FASRC.4 in the RLS2 register) and CAS resync criteria (CASRC.5 in the RLS2 register) latched status bits for FAS and CAS resync criteria to determine when to manually resync the receive port. This can be done using the resync configuration bit (RESYNC.0 in the RCR1 register). Monitor PCVCR for CRC-4 resync criteria (915/1000 CRC-4 codeword errors) to determine when to manually resync the receive port using the resync configuration bit. PCVCR should be updated on one-second intervals (1000 possible CRC-4 codeword errors in one second).

6. T1 RECEIVE SYNC

Description:
T1 receive sync may get into a state where it cycles in and out of sync. This occurs when the T1 receive sync cannot align to a new frame alignment that is 2 bits before the current frame alignment.

Work Around:
When the user receives a loss-of-frame condition (RLS1.RLOFD) that repeatedly clears and sets, the user should check if the change-of-frame alignment latched status bit (COFA.5 in the RLS2 register) is set at least once per 20ms over a period of 200ms. If COFA is being set at that rate, the user should implement the following:

Disable the receive data path via the receive-port frame-enable configuration bit (FRM_EN.7 in the RMMR register) for 5μs. Doing so separates the old sync and the new sync by more than 2 bits, allowing the new sync to be properly detected.

7. TRANSMIT SYNC INITIALIZATION

Description:
When using a transmit sync source other than the internal sync (e.g., TSYNC as an input), the transmit data path cannot update the alignment to sync input boundary if the new alignment is 1 bit before the current frame alignment.

Work Around:
When minimum delay mode is enabled and when sync source such as PLB, TSYNC configured as input, transmit synchronizer, or transmit elastic store is used, the following routine can be used to ensure the sync is properly updated.

Wait for the new sync source to be applied and stable. Disable the transmit data path via the transmit port frame-enable configuration bit (FRM_EN.7 in the TMMR register) for 5μs. This separates the old sync and the new sync by more than 2 bits and the new sync should now be properly detected.

8. RSIG PIN/SIGNALING REINSERTION IN ELASTIC STORE/IBO MODE

Description:
When only some ports have elastic store/IBO enabled, the RSIG pins for elastic store/IBO-enabled ports are not valid. This also affects signaling reinsertion.

Work Around:
To use the RSIG pin or signaling reinsertion when elastic store or IBO mode is enabled, all ports should have the elastic store/IBO enabled.

9. RECEIVE CRC-16 DISPLAY BIT RCRCD

Description:
Receive CRC-16 display (located in bit 7 of the RHC register) does not work.

Work Around:
If all ports (Rx and Tx) are configured for E1 mode, this function will work.

10. TRANSMIT END OF MESSAGE AND LOOP BIT TEOML

Description:
Transmit end of message and loop bit (located in bit 2 of the THC1 register) does not work.

Work Around:
Manually reload HDLC FIFO with packet data to repeat the packet. Or, if all ports (Rx and Tx) are configured for E1 mode this function will work.

11. RECEIVE ELASTIC STORE SLIP LATCHED STATUS BIT RSLIP

Description:
Receive elastic store slip latched status bit RSLIP (located in bit 5 in the RLS4 register) is not latched.

Work Around:
RSLIP bit is an OR of the RESEM (RLS4.6) and RESF (RLS4.7) bits, which are latched status bits. Clear RESEM and RESF to clear RSLIP.

12. TRANSMIT ELASTIC STORE SLIP LATCHED STATUS BIT TSLIP

Description:
Transmit elastic store slip latched status bit TSLIP (located in bit 5 in the TLS1 register) is not latched.

Work Around:
TSLIP bit is an OR of the TESEM (TLS1.6) and TESF (TLS1.7) bits, which are latched status bits. Clear TESEM and TESF to clear TSLIP.

13. RRTS7 READ ISSUE

Description:
When switched from T1 to E1 without using hardware reset, RRTS7 reads an ORed output of E1 RRTS7, T1 RFDL.

Work Around:
Use global soft reset when switching from T1 to E1.

14. E1 RECEIVE MULTIFRAME LATCHED STATUS CAS MODE

Description:
E1 receive signaling registers (RS1–RS16) are updated 10μs after the RMF bit is set.

Work Around:
Wait at least 10μs after RMF bit detect before reading the RS1–RS16 registers.

15. E1 RECEIVE MULTIFRAME LATCHED STATUS CSS MODE

Description:
E1 RMF (RLS4.0) latched status bit in CCS mode is sometimes set on the multiframe boundary, and again 1 frame after the multiframe boundary. The RS1–RS16 registers in CCS mode are updated one frame after the multiframe boundary.

Work Around:
Wait at least 250μs after detecting RMF before clearing the latched status bit and reading the RS1–RS16 registers.

16. RECEIVE DATA PATH INSERTION FUNCTIONS

Description:
Receive data path insertion functions (idle code, digital milliwatt, bit inversion, internal BERT direction reversed, force signaling all ones) do not pass through RSER when elastic store or IBO mode is enabled. Receive data path insertion functions do pass through RSER when elastic store is disabled, and always pass through internal loopbacks (per-channel loopback, payload loopback).

Work Around:
None.

17. RECEIVE T1 COFA STATUS BIT

Description:
Receive T1 COFA status bit does not report multiframe change of frame alignment.

Work Around:
None.

18. BPCLK REFERENCE SELECT

Description:
REFCLKIO cannot be selected as reference clock for BPCLK.

Work Around:
None.

19. TTIP3/TRING3 PINS

Description:
TTIP3 and TRING3 pins are reversed.

Work Around:
This has no effect on operation of the device, unless it is configured for transmit G.703 clock synchronization mode (LTIPSR.TG703), in which case the blocking cap on TTIP3 should be placed on TRING3.