Rev: 030909

ERRATA SHEET
DS26518

Revision A2 Errata

The errata listed below describe situations where DS26518 revision A2 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata when the opportunity to redesign the product presents itself.

This errata sheet only applies to DS26518 revision A2 components. Revision A2 components are branded on the topside of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another DS26518 die revision, visit our website at ***www.maxim-ic.com/errata****.*

1) RECEIVE LOOP CODES STATUS BITS

Description:
Receive loop code status bits do not work in the DS26518 rev A2. The following are the incorrect bits:

BIT LOCATION	BIT NAME	BIT DESCRIPTION
RRTS3.0	LUP	Loop Up Code Detected Condition
RRTS3.1	LDN	Loop Down Code Detected Condition
RRTS3.2	LSP	Spare Code Detected Condition
RLS3.0	LUPD	Loop Up Code Detected Condition Detect
RLS3.1	LDND	Loop Down Code Detected Condition Detect
RLS3.2	LSPD	Spare Code Detected Condition Detect
RLS3.4	LUPC	Loop Up Code Detected Condition Clear
RLS3.5	LDNC	Loop Down Code Detected Condition Clear
RLS3.6	LSPC	Spare Code Detected Condition Clear

Workaround:
Use the internal BERT to detect loop codes. Configure the internal BERT to detect a repetitive pattern for the loop code. Map all the receive data bits to the internal BERT (unframed mode). Loop code is detected when the BERT pattern matches and the BERT bit error rate is less than 10%.

Transmit loop codes work correctly.

2) AUTOMATIC RAI INSERTION

Description:
When automatic RAI insertion is enabled, the RAI is not automatically inserted if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled).

Workaround:
Monitor the CRC4 sync counter bits (RRTS7[7:3]) in register E1RRTS7 (Receive Real-Time Status Register 7–E1 Mode). If CSC count value exceeds 16, manually transmit the RAI alarm via the alarm bit

(E1TNAF.5) in the Transmit Nonalign Frame Register (E1TNAF). If CRC4 sync is found, stop the alarm via the E1TNAF alarm bit.

3) RECEIVE FRAMER SOFT RESET

Description:
The receive framer soft reset bit (SFTRST bit 1 in the RMMR register) does not work.

Workaround:
Disable the port using the frame enable bit (FRM_EN bit 7 in the RMMR register). Write 00 to all addresses in the framer span. Then write FF to latched status addresses in framer span.

4) TRANSMIT FRAMER SOFT RESET

Description:
The transmit framer soft reset bit (SFTRST bit 1 in the TMMR register) does not work.

Workaround:
Disable the port using the frame enable bit (FRM_EN bit 7 in the TMMR register). Write 00 to all addresses in the framer span. Then write FF to latched status addresses in framer span.

5) RECEIVE ESTORE SLIP LATCHED STATUS BIT RSLIP

Description:
The receive estore slip latched status bit, RSLIP (located in bit 5 in register RLS4), is not latched.

Workaround:
The RSLIP bit is an OR of the RESEM (RLS4.6) and RESF (RLS4.7) bits, which are latched status bits. Clear RESEM and RESF to clear RSLIP.

6) TRANSMIT ESTORE SLIP LATCHED STATUS BIT TSLIP

Description:
The transmit estore slip latched status bit, TSLIP (located in bit 5 in register TLS1), is not latched.

Workaround:
The TSLIP bit is an OR of the TESEM (TLS1.6) and TESF (TLS1.7) bits, which are latched status bits. Clear TESEM and TESF to clear TSLIP.

7) RRTS7 READ ISSUE

Description:
When switched from T1 to E1 without using hardware reset, RRTS7 reads an ORed output of E1 RRTS7, T1 RFDL.

Workaround:
Use global soft reset when switching from T1 to E1.

8) E1 RECEIVE MULTIFRAME LATCHED STATUS CAS MODE

Description:
The E1 receive signaling registers (RS1–RS16) are updated 10µs after the RMF bit is set.

Workaround:
Wait at least 10µs after the RMF bit detect before reading the RS1–RS16 registers.

9) E1 RECEIVE MULTIFRAME LATCHED STATUS CSS MODE

Description:
The E1 RMF (RLS4.0) latched status bit in CCS mode is sometimes set on the multiframe boundary, and again one frame after the multiframe boundary. The RS1–RS16 registers in CCS mode are updated one frame after the multiframe boundary.

Workaround:
Wait at least 250µs after detecting RMF before clearing the latched status bit and reading RS1–16 registers.

10) TTIP3/TRING3 PINS

Description:
TTIP3 and TRING3 pins are reversed.

Workaround:
This has no affect on operation of the device, unless it is configured for transmit G.703 clock synchronization mode (LTIPSR.TG703), in which case the blocking cap on TTIP3 should be placed on TRING3.

11) TTIP/TRING OUTPUTS NOT HIGH IMPEDANCE WITH TXENABLE LOW DURING POWER-UP

Description:
The TTIPn/TRINGn line drivers should be high impedance whenever TXENABLE is low. On rev A2 devices, the TTIPn/TRINGn line drivers are briefly enabled during power-up, even if TXENABLE is low. This may cause the inactive DS26518 in a Y-cable application to attenuate the transmit waveform of the active DS26518 and create a bit error, as seen in the figures below.

Figure 1

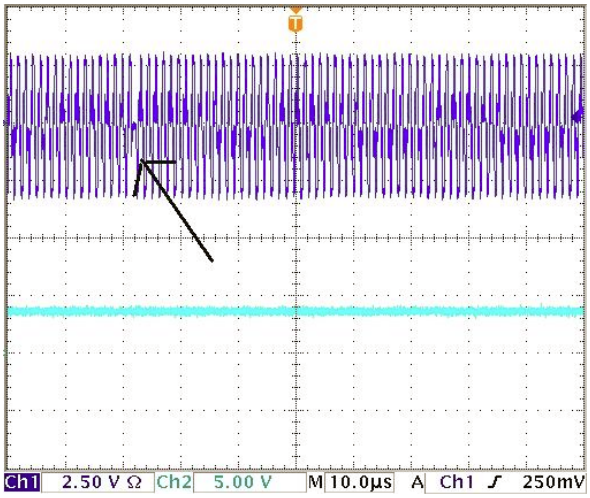
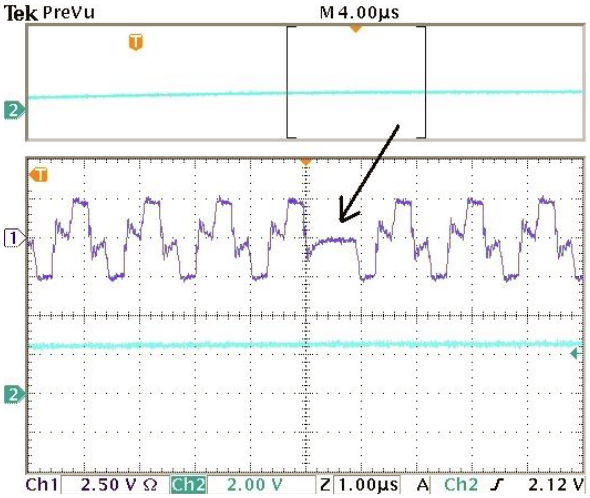


Figure 2



Workaround:
None.