MAXIM

ERRATA SHEET
DS26522

_____ *Revision A1 Errata*

The errata listed below describe situations where DS26522 revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26522 revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another DS26522 die revision, visit our website at www.maxim-ic.com/errata.

1) FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE

Description:
The DS26522 does not identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS26522 does not report the LFA alarm when the Japanese JT-G704 LFA pattern of "11111111 11111111" is present in the facilities data link. The DS26522 only responds to the normal G.704 LFA pattern of "11111111 00000000."

Workaround:
To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to 0. The TFDLS bit is located in the TCR2 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly, and the RFDLF status bit indicates an update. The RFDLF status bit is located in the SR8 register. Because the Japanese ESF LFA alarm pattern is 2 bytes long, the RFDL register must be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm will be set. If 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, the alarm will be cleared.

2) PROGRAMMABLE CHANNEL BLANKING MAY LEAD TO DROPPED DATA UNDER CERTAIN IBO OPERATING MODES

Description:
When the part is programmed for channel blanking with channel 1 and channel 2 blanked at the same time, data can be dropped if the T1 rate data is being mapped onto an E1 rate backplane in byte-interleaved IBO mode.

Workaround:
None.

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3) ERROR COUNT REGISTERS COULD ROLL OVER AT 0xFFFFh IN MANUAL UPDATE MODE

Description:
The error count registers can roll over after the counters have saturated in manual update mode (ERCNT.MCUS = 0). This rollover will not occur when the error count registers are not set to be updated manually; they will saturate as stated in the data sheet.

Workaround:
Ensure that the manual error counter update bit is set (ERCNT.MECU = 1) before the registers are allowed to saturate.

4) DELAY TIME BETWEEN SUBSEQUENT WRITE/READ ACCESSES REQUIRES AN 80ns WAIT TIME

Description:
In the data sheet, the parameter denoted as t10 in the AC characteristics is written so it only applies to subsequent (back to back) write or read accesses to the device. However, t10 actually applies to any write or read access whether from the DS26522 or any other device on the bus. This means that when the processor bus is accessing DS26522, it is always necessary to have an 80ns dead time period before any write or read to DS26522.

Workaround:
The first solution is to change the bus timing so that there is at least an 80ns wait time between accesses to DS26522 or any other device on the bus. This will ensure enough time for the DS26522 to properly write or read to the internal registers.

The second solution is to change the bus hardware to include gating of the write and read lines until the chip-select line goes active. This solution also needs to maintain the current data sheet timing restriction of parameter t10, otherwise subsequent writes or reads to DS26522 will be in error.

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