



# DS26528

## T1/E1/J1 Octal Transceiver

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### REVISION A1 ERRATA

The errata listed below describe situations where DS26528 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26528 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS26528 die revision, visit our website at [www.maxim-ic.com/errata](http://www.maxim-ic.com/errata).

#### 1. RECEIVE AUTOMATIC GAIN CONTROL (AGC) LOOP MAY CAUSE BIT ERRORS WHEN THE INPUT SIGNAL IS AT +2dB

##### Description:

The analog receiver may cause bit errors when the input level is at +2dB with respect to the receiver's own 0dB reference due to the AGC loop. This is a result of an unintended rollover in the digital AGC up/down counter used in the receive AGC. This behavior may also be present in monitor mode if an overload condition occurs where the receive input level is at +2dB.

##### Work Around:

Write 80h to the REF EQMD register at the appropriate offset (1014h 1034h, 1054h, 1074h, 1094h, 10B4h, 10D4h and 10F4h). This will adjust the receive-input level into the +4dB range, which eliminates the problem since the errata is only prevalent when the input level is at +2dB. If monitor mode is used, a resistive attenuator should be used with an attenuation amount slightly greater than or equal to the amount of monitor gain to prevent overload, which would cause the same problem.

#### 2. TRANSMIT WAVEFORMS MAY NOT BE CENTERED IN THEIR RESPECTIVE TEMPLATES

##### Description:

Transmit waveforms may not be centered in their respective templates leading to possible template violations or less than ideal template compliance.

##### Work Around:

To better center the transmit waveforms, the following registers should be set as shown. Table 1 shows the register map addresses for the registers that should be set for each port.

**Table 1. Transmit Register Address**

PORT #	TXLAA	TXLAB	TXLAC	TXLAD	TXLAE	LTITSR
LIU 1	1008	1009	100A	100B	100C	1001
LIU 2	1028	1029	102A	102B	102C	1021
LIU 3	1048	1049	104A	104B	104C	1041
LIU 4	1068	1069	106A	106B	106C	1061
LIU 5	1088	1089	108A	108B	108C	1081
LIU 6	10A8	10A9	10AA	10AB	10AC	10A1
LIU 7	10C8	10C9	10CA	10CB	10CC	10C1
LIU 8	10E8	10E9	10EA	10EB	10EC	10E1

Table 2 shows the values that should be written to Bit 5 (TIMPL1) and Bit 4 (TIMPL0) of the LTITSR register for each port and indicated operating mode.

**Table 2. LTITSR Register Setting**

MODE	TERMINATION ( $\Omega$ )	TIMPL1	TIMPL0
E1	75	0	0
E1	120	0	1
T1	100	0	0
J1	110	0	0

Table 3 shows the value that should be written to each transmit register for the indicated operating mode. Note: for TXLAE, when there are two values shown, the first value shown is for applications where transmit impedance matching is ON, the second value shown is for applications where transmit impedance matching is OFF.

**Table 3. Transmit Register Value**

LBO	TXLAA	TXLAB	TXLAC	TXLAD	TXLAE
E1 LBO 0	00	05	00	00	07/03
E1 LBO 1	A0	05	00	00	04/02
T1/J1 LBO 0	02	20	01	03	01
T1/J1 LBO 1	A2	18	01	03	01
T1/J1 LBO 2	B2	38	01	03	08
T1/J1 LBO 3	BA	20	01	03	08
T1/J1 LBO 4	A9	58	01	03	08
T1/J1 LBO 5	FB	02	00	00	14
T1/J1 LBO 6	00	00	00	00	15
T1/J1 LBO 7	00	00	00	00	11

### 3. T1.403 TEMPLATE MAY BE VIOLATED IN SOME T1 APPLICATIONS

**Description:**

In some T1 applications, it is possible that the T1 line build-outs will clip the very end of the T1.403 template as the pulse returns to zero after the undershoot portion of the waveform.

**Work Around:**

None.

### 4. INPUT LEAKAGE CURRENT ON RM\_RFSYNC AND RSIG IS HIGHER THAN SHOWN IN THE DATA SHEET

**Description:**

The actual input-leakage current on RM\_RFSYNC and RSIG is approximately 150 $\mu$ A, which is higher than the leakage current shown in the *DC Characteristics* section of the data sheet. There are two analog test buffers that do not power-down correctly in this revision, and the result is an increased leakage current on these two pins.

**Work Around:**

None.

**5. THE DELAY TIME FROM RDB OR DSB ACTIVE TO DATA[7:0] ACTIVE IS 120ns****Description:**

The actual delay time from RDB or DSB active to DATA[7:0] active is 120ns instead of the 75ns shown in the data sheet.

**Work Around:**

None.

**6. SHORT-CIRCUIT PROTECTION MAY ACTIVATE WHEN THE PART IS IN T1 LBO 6 (CSU –15dB) OPERATING MODE WITH IMPEDANCE MATCH ON EVEN IN THE PRESENCE OF A PROPER LOAD****Description:**

When the part is operating in T1 LBO6 mode (CSU –15dB mode) and impedance match is on, it is possible even in the presence of a proper load that the short-circuit protection may activate, causing distorted output waveforms or completely eliminating them.

**Work Around:**

Disable short-circuit protection when operating in this mode by setting bit 4 of the TXCMDC register, which is located at offsets 100Fh, 102Fh, 104Fh, 106Fh, 108Fh, 10AFh, 10CFh, and 10EFh.

**7. OPEN-CIRCUIT DETECTION MAY NOT FUNCTION PROPERLY WHEN IN T1 LBO 1–4 OPERATING MODES AND IMPEDANCE MATCH IS ON****Description:**

When the part is operating with impedance match on in T1 LBO 1–4, the open-circuit detect function may not operate properly and the corresponding status bit OCS in the LRSR register will not be set.

**Work Around:**

None.

**8. FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE****Description:**

The DS21458/455 does not identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS21458/455 will not report the LFA alarm when the Japanese JT-G704 LFA pattern of '11111111 11111111' is present in the facilities data link. The DS21458/455 will only respond to the normal G.704 LFA pattern of '11111111 00000000'.

**Work Around:**

To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to a 0. The TFDLS bit is located in the T1TCR1 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly and an update is indicated by the RFDLF status bit. The RFDLF status bit is located in the SR8 register. Since the Japanese ESF LFA alarm pattern is 2 bytes long, the RFDL register has to be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm will be set. If 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, the alarm will be cleared.

**9. PROGRAMMABLE CHANNEL BLANKING MAY LEAD TO DROPPED DATA UNDER CERTAIN IBO OPERATING MODES****Description:**

When the part is programmed for channel blanking with channel 1 and channel 2 blanked at the same time data can be dropped if T1 rate data is being mapped onto an E1 rate backplane in byte-interleaved IBO mode.

**Work Around:**

None.

**10. ERROR COUNT REGISTERS COULD ROLL OVER AT 0xFFFFh IN MANUAL UPDATE MODE****Description:**

The error count registers can roll over after the counters have saturated if the counters are being updated in manual update mode (ERCNT.MCUS = 0). This roll over will not occur when the error count registers are not set to be updated manually, they will saturate as stated in the datasheet.

**Work Around:**

Ensure that the manual error counter update bit is set (ERCNT.MECU = 1) before the registers are allowed to saturate.

**11. THE RIM7 (E1 MODE) REGISTER IS NOT ACCESSIBLE****Description:**

The RIM7 register (at address 0A6h + (200h x n), where n = 0 to 7 for Ports 1 to 8) is not accessible in E1 Mode. This register indicates changes in state of the Sa bits.

**Work Around:**

Use the other Sa Bit Access registers to determine a change of state of the Sa bits. The Sa bits can be accessed through either the E1RAF/E1RNAF and E1TAF/E1TNAF registers or the E1RSa4 to E1RSa8 and E1TSa4 to E1TSa8 registers. These registers are covered in detail in the DS26528 datasheet.

**12. THE E1RSAIMR REGISTER IS NOT ACCESSIBLE****Description:**

The E1RSAIMR register (at address 014h + (200h x n), where n = 0 to 7 for Ports 1 to 8) is not accessible. This register is used to select which Sa bits can cause a change of state interrupt in the RLS7 register.

**Work Around:**

None.

**13. THE RLS7 (E1 MODE) REGISTER IS NOT ACCESSIBLE****Description:**

The RLS7 register (at address 096h + (200h x n), where n = 0 to 7 for Ports 1 to 8) is not accessible in E1 mode. This register is used to interrupt when bit changes are observed in selected Sa bit positions.

**Work Around:**

None.

**14. THE SaBITS REGISTER IS NOT ACCESSIBLE****Description:**

The SaBITS register (at address 06Eh + (200h x n), where n = 0 to 7 for Ports 1 to 8) is not accessible. This register is used to display the last received Sa bits.

**Work Around:**

Use the other Sa Bit Access registers to determine the status of the Sa bits. The Sa bits can be accessed through either the E1RAF/E1RNAF and E1TAF/E1TNAF registers or the E1RSa4 to E1RSa8 and E1TSa4 to E1TSa8 registers. These registers are covered in detail in the DS26528 datasheet.

**15. THE Sa6CODE REGISTER IS NOT ACCESSIBLE****Description:**

The Sa6CODE register (at address 06Fh + (200h x n), where n = 0 to 7 for Ports 1 to 8) is not accessible. This register is used to display the last received Sa6 Codeword as defined by ETS 300233.

**Work Around:**

Use the other Sa Bit Access registers to determine status of the Sa6 bits. The Sa6 bits can be accessed through either the E1RAF/E1RNAF and E1TAF/E1TNAF registers or the E1RSa4 to E1RSa8 and E1TSa4 to E1TSa8 registers. These registers are covered in detail in the DS26528 datasheet.

**16. THE RSYNC PIN DIRECTION DEFAULT VALUE IS INCORRECT****Description:**

The direction of RSYNC at power up or reset is incorrect. The RSYNC pin defaults to an output. The default direction of the RSYNC pin at power up or reset should be as an input as stated in the datasheet. The default direction is set by RIOCR.RSIO bit, which should default to a 1 but incorrectly defaults to a 0 in this revision.

**Work Around:**

Set the RIOCR.RSIO bit to a 1 after power-up or reset to configure the RSYNC pin as an input.

**17. THE T1 AIS (BLUE ALARM) SET AND CLEAR CRITERIA ARE INCORRECT****Description:**

The T1 AIS (Blue Alarm) set and clear criteria are incorrect. The AIS alarm will be set when, over a 3 ms window, 5 or less zeros are received. The AIS alarm will be cleared when, over a 3ms window, 6 or more zeros are received. This alarm should be set when 4 or less zeros are received and cleared when 5 or more zeros are received.

**Work Around:**

None.