Rev: 012108

ERRATA SHEET
DS26556

Revision A1 Errata

The errata listed below describe situations where DS26556 revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata in subsequent die revisions.

*This errata sheet only applies to DS26556 revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another DS26556 die revision, visit our website at **www.maxim-ic.com/errata**.*

1) TRANSMIT TERMINATING IMPEDANCE MATCH, WHEN ENABLED, MAY RESULT IN TRANSMIT WAVEFORMS THAT FAIL OR ARE NOT CENTERED IN THEIR RESPECTIVE TEMPLATES

Description:
If enabled via the LIU Transmit Impedance and Pulse Shape Selection Register (LTITSR.6 = 0), the Transmit Terminating Impedance Match feature may result in transmit waveforms that are not centered in their respective templates or fail template completely.

Workaround:
The transmit waveforms can be modified by setting several registers in the part to better center the waveforms and remove any template violations. These registers are located at the addresses shown in the table below. Contact the Telecom Support Group at telecom.support@maxim-ic.com for detailed information regarding these errata and the appropriate values with which these registers should be programmed.

PORT #	TXLAA	TXLAB	TXLAC	TXLAD	TXLAE	LTITSR
LIU 1	1008	1009	100A	100B	100C	1001
LIU 2	1028	1029	102A	102B	102C	1021
LIU 3	1048	1049	104A	104B	104C	1041
LIU 4	1068	1069	106A	106B	106C	1061

2) PORT 4 WILL NOT OPERATE IN BYTE SYNCHRONOUS OPERATING MODE

Description:
Port 4 will not operate in Byte Synchronous mode when enable by the RBYT bit in the Cell/Packet Control 2 register (CPC2.RBYT = 1 located at address 1642h). There is a timing issue that will cause data corruption. Bit synchronous mode will operate correctly (CPC2.RBYT = 0).

Workaround:
None.

3) DELAY TIME BETWEEN SUBSEQUENT WRITE/READ ACCESSES REQUIRES AN 80ns WAIT TIME

Description:
In the current data sheet, the parameter denoted as t10 in the AC Characteristics is written so it only applies to subsequent (back to back) write or read accesses to the device. However t10 actually applies to any write or read access whether from the DS26556 or any other device on the bus. This means that when the processor bus is accessing DS26556, it is always necessary to have an 80ns dead time period before any write or read to DS26556.

Workaround:
The first solution is to change the bus timing so that there is at least an 80ns wait time between accesses to DS26556 or any other device on the bus. This will ensure enough time for DS26556 to properly write or read to the internal registers.

The second solution is to change the bus hardware to include gating of the write and read lines until the chip select line goes active. This solution also needs to maintain the current data sheet timing restriction of parameter t10, otherwise subsequent writes or reads to the DS26556 will be in error.