DS3112

TEMPE T3 E3 Multiplexer
3.3V T3/E3 Framer and
M13/E13/G.747 Mux

REVISION A1 ERRATA

The errata listed below describe situations where DS3112 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to fix these errata in subsequent die revisions.

This errata sheet only applies to DS3112 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code of the form yywwA1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS3112 die revision, visit the website at www.maxim-ic.com.

1. B3ZS/HDB3 BPV UNDERCOUNT

Description:
Register BPVCR undercounts BPVs (BiPolar Violations), misinterpreting some BPVs as being part of B3ZS/HDB3 code words.

Work Around:
None

2. E3 CV OVERCOUNT

Description:
In E3CV mode, register BPVCR overcounts CVs (Code Violations), counting every BPV as a CV.

Work Around:
None

3. BERT PRBS SYNC WHEN RECEIVING ALL ZEROES

Description:
The BERT (Bit Error Rate Tester) indicates pattern sync (SYNC=1 in register BERTEC0) when receiving all zeroes but expecting a PRBS signal.

Work Around:
Ignore SYNC = 1 when in PRBS mode and the Read-All-Zeroes bit (RA0) is set in register BERTEC0.

4. HDLC RECEIVE ERROR ON 7E, FF

Description:
When the HDLC controller receives the sequence {7Eh, <packet>, 7Eh, FFh} where FFh is the idle value, it will interpret the {7Eh, FFh} part of the sequence as an aborted 1-byte packet. This 1-byte packet will be written to the receive HDLC FIFO with the OBYTE and CBYTE bits set and PS1 = PS0 = 1, indicating abort detected. In addition, the Receive-Abort Sequence-Detected bit (RABT) in the HDLC Status Register (HSR) will be set.

Work Around:
Ignore receive FIFO entries that have OBYTE = CYBTE = PS1 = PS0 = 1.

5. HDLC ASYNCHRONOUS LOGIC ERROR

Description:
The HDLC receive FIFO may lose a byte of data when the FIFO is read while data is also being written to the FIFO.

Work Around:
1) Wait until the complete packet is in the receive FIFO before reading it out (RPE bit set in HSR Register).
2) Run the CPU clock synchronous to the T3 clock.

6. HDLC FIFO BIT ERRORS

Description:
The HDLC receive and transmit FIFOs can introduce bit errors. 1 byte out of a few million can have a bit wrong, based on lab tests at Dallas.

Work Around:
None

7. FEAC RFFO LOGIC ERROR IN 8-BIT BUS MODE

Description:
The Receive FEAC FIFO Overflow (RFFO) bit in the FEAC Status Register (FSR, address 92h) is not updated and cleared when only the upper byte of the register (93h) is read in 8-bit bus mode.

Work Around:
1) Operate in 16-bit bus mode.
2) In 8-bit mode, read the lower byte (92h) to update the register and then read the upper byte (93h).

8. FEAC RFFE LOGIC ERROR

Description:
The Receive FEAC FIFO Empty (RFFE) bit in the FEAC Status Register (FSR, address 92h) is not always set when the last byte is read from the FIFO.

Work Around:
Run the CPU clock synchronous with the T3 clock.

9. TFL<3:0> ASYNCHRONOUS TIMING PROBLEM

Description:

The HDLC controller's Transmit FIFO Level bits, TFL<3:0> in register HSR, are updated asynchronously to any reads of the HSR register. This means that a read of HSR can happen at an instant when some of the TFL bits have been updated but others have not been updated, resulting in a bad TFL value being read.

Work Around:

Read the HSR register until two consecutive reads have identical TFL values. This will yield the true TFL value.

10. NO TEST* PULLUP RESISTOR

Description:

The DS3112 data sheet says that the Factory Test Input pin TEST* should be left open-circuited because the pin has an internal 10kΩ pullup. In fact, the TEST* pin does not have a pullup resistor.

Work Around:

Wire TEST* to V_{DD} for proper operation 7.

11. BPV/EXZ INSERTION NOT RELIABLE

Description:

The DS3112 has a timing problem with the Bipolar Violation Insert and Excessive Zero Insert functions controlled by the BPVI and EXZI bits in register T3E3EIC. As a result, the DS3112 does not always insert BPVs or ExZs when directed to do so.

Work Around:

Avoid comparing observed BPV/ExZ counts with intended BPV/ExZ insertion rates, and instead compare insertion rates actually observed by one piece of equipment with those observed by another.

12. HDLC RECEIVE FIFO REMPTY BIT PROBLEM IN 8-BIT BUS MODE

Description:

The assignment of the REMPTY bit to the RHDLC register (address 82-83h) makes possible a situation in which invalid data might be read from the HLDC Receive FIFO when in 8-bit bus mode. The following can happen:

(1) When the FIFO is initially empty (lower byte data is invalid, upper byte REMPTY = 1), the user reads the data in the lower byte of the receive FIFO.
(2) Before the user can read the upper byte of the FIFO, the DS3112 asynchronously writes data into the FIFO, setting REMPTY = 0.
(3) The user then reads the upper byte of the FIFO and sees REMPTY = 0, which indicates that the invalid data read in step 1 is actually valid.

Work Around:

Wait until a complete packet is in the FIFO, as indicated by the RPE bit in the HSR register an then read the FIFO until REMPTY = 1 during a period when the DS3112 is not going to be writing the Receive FIFO.

On the next rev of the DS3112, REMPTY will be moved to bit 14 of the HSR register, which is where all other Receive and Transmit FIFO status bits are located. The procedure for reading the Receive FIFO will then be to (1) read the REMPTY bit in HSR, (2) if REMPTY = 0, then read the Receive FIFO.