DS3112
TEMPE T3 E3 Multiplexer 3.3V T3/E3 Framer and M13/E13/G.747 Mux

REVISION C1 ERRATA

The errata listed below describe situations where DS3112 revision C1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3112 revision C1 components. Revision C1 components are branded on the topside of the package with a six-digit code in the form yywwC1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS3112 die revision, visit the website at **www.maxim-ic.com/errata**.

1. FTDEN OUTPUT PULSES ONE CLOCK CYCLE EARLY

Description:

The FTDEN output pin (T3/E3—transmit formatter serial-data enable) pulses one clock cycle earlier than specified in Figure 2.4A of the DS3112 data sheet. This occurs in T3 mode only. FTDEN is early for both data-enable and gapped-clock modes of operation. This only affects unchannelized T3 operation; channelized T3 and E3 are not affected.

This erratum has no effect on the output data stream. Figure 1 shows that whether FTDEN pulses per the data sheet or one cycle early, the formatter output data is the same. The overhead bit is properly inserted between payload bit 84 and payload bit 1. The example in Figure 1 depicts the DS3112 where FTDEN is configured as a data enable. The gapped clock case is identical.

Work Around:

Use an external flip-flop to delay the FTDEN signal one clock cycle.

2. TRANSMIT LIU INTERFACE IS BIPOLAR FORMAT WHEN TRANSMITTING AIS

Description:

When the TAIS bit in the T3E3CR register is asserted to transmit AIS, the output on the HTPOS/HTNEG pins is always bipolar format, even if the DS3112 is configured for unipolar operation (MC1:UNI = 1).

Work Around:

Configure the DS3112 for bipolar interface mode by setting UNI = 0 in the MC1 register. Also configure the neighboring LIU for bipolar interface mode.

3. LOGIC ERROR WHEN TRANSMITTING E3 AIS IN BIPOLAR LIU INTERFACE FORMAT

Description:

When the device is configured for bipolar LIU interface format and E3 operating mode, setting the transmit AIS (TAIS) bit in the T3E3CR register causes the device to drive both HTPOS and HTNEG pins high simultaneously rather than driving alternating ones on the two pins. Since HTPOS = HTNEG = 1 is an illegal state in bipolar interface format, an LIU wired to HTPOS and HTNEG will have unpredictable behavior.

Work Around:

Use the repetitive pattern generator in the DS3112's BERT block to generate E3 AIS (unframed all ones). After the part is initialized for normal operation, set the following registers to begin transmitting E3 AIS:

```
// select unframed BERT pattern generation
BERTMC = 1E1Eh  // BERT set to source and sink T3/E3 payload and framing
bits
T3E3CR:TPT = 1   // T3/E3 formatter set to not insert framing bits

// set BERT to transmit and detect all ones
BERTRP0 = FFFFh  // set repetitive pattern register to all ones
BERTRP1 = FFFFh

BERTC0 = 0F10h  // RPL[3:0]=1111, PBS=0, RINV=0, TINV=0, PS[2:0]=100

BERTC1:TC = 1  // Toggle TC bit to load the pattern generator
BERTC1:TC = 0
```

Set the following registers to stop transmitting E3 AIS and begin transmitting a normal framed E3 signal:

```
BERTMC = 0000h  //  do not source and sink from BERT
T3E3CR:TPT = 0  // T3/E3 formatter set to insert framing bits
```

Note: This procedure also generates unframed all ones in DS3 mode, if desired.

4. RECEIVER AIS, RAI, AND T3IDLE STATUS BITS DO NOT CLEAR DURING LOF

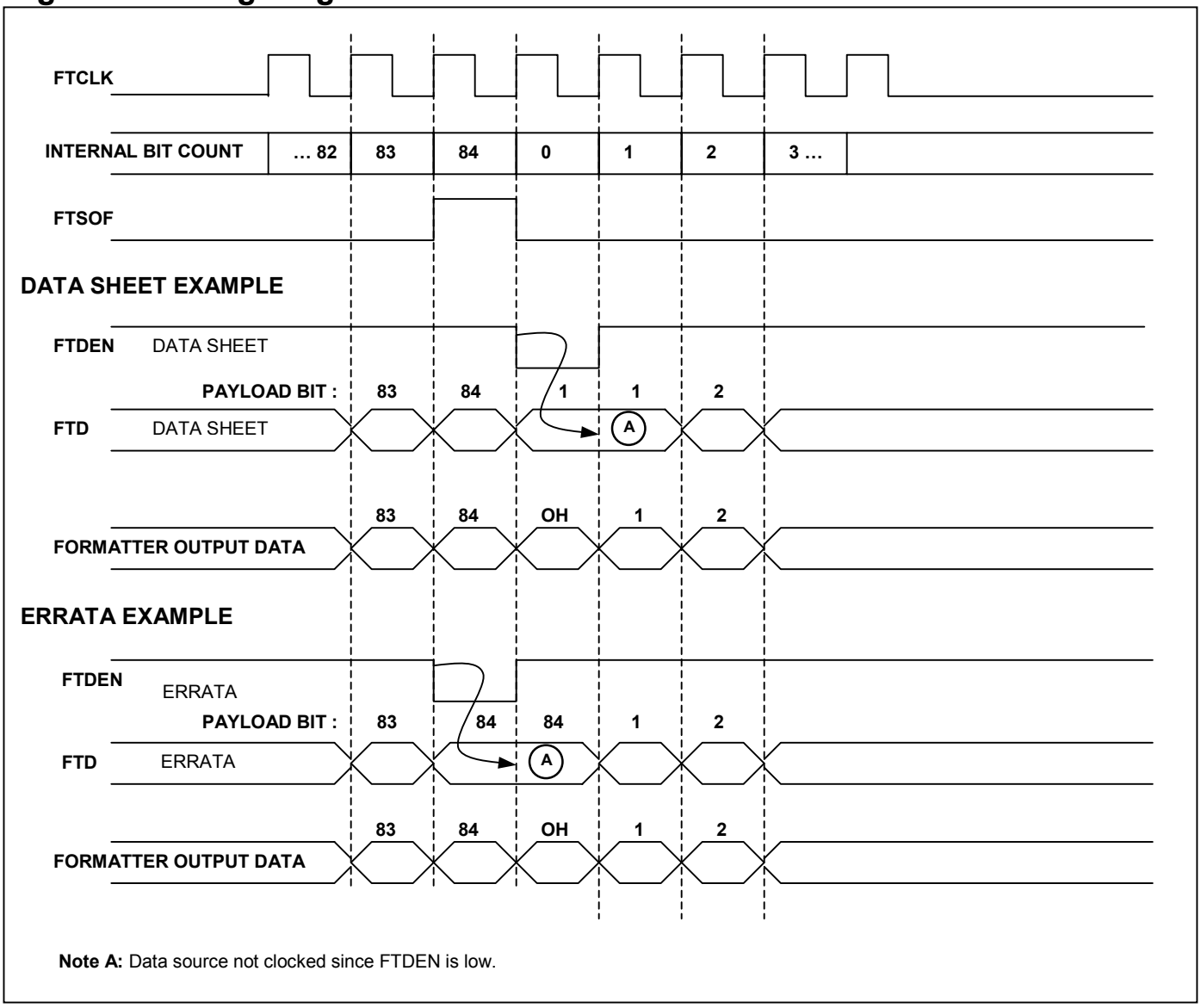
Description:

Any of the T3E3SR:AIS, T3E3SR:RAI, or T3E3SR:T3IDLE status bits that are already set to 1 when the framer declares loss of frame (LOF) (and sets the T3E3SR:LOF status bit) remain set throughout the LOF interval. After the DS3 framer resynchronizes to the framing information in the incoming data stream, the status bits are allowed to update (i.e., clear when read). This erratum only occurs in DS3 mode, not in E3 mode.

Work Around:

If the LOF status bit is set, ignore the AIS, RAI, and T3IDLE status bits.

Figure 1. Timing Diagram



Note A: Data source not clocked since FTDEN is low.

5. TRANSMIT FEAC CAN SEND ADDITIONAL COPIES OF CODEWORD A

Description:

If TFS[1:0] transitions from 01 to 00 after the FEAC transmitter is done sending codeword A 10 times, then the FEAC transmitter erroneously sends codeword A 10 more times before sending all ones. Similarly, if TFS[1:0] transitions from 10 to 00 after the FEAC transmitter is done sending codeword A 10 times and codeword B 10 times, the FEAC transmitter erroneously sends codeword A 10 more times before sending all ones.

Work Around:

For TFS = 01 mode (send codeword A 10 times), immediately after writing TFS to 01, write TFS back to 00. When this is done the FEAC transmitter behaves properly and only sends codeword A 10 times.

For TFS = 10 mode (send codeword A 10 times, then send codeword B 10 times), TFS must be written back to 00 during the transmission of codeword B 10 times. This must be timed by the host processor and should occur 20ms to 30ms after TFS is set to 10.

6. TRANSMIT DS3 AIS ANOMALIES

Description:

Activating and deactivating AIS (T3E3CR1:TAIS set to 1) in DS3 mode can cause the insertion of a bipolar violation and may cause the generation of erroneous P-bits in one or both of the next two M-frames. These anomalies are caused by transitions into and out of DS3 AIS. The formatter transmits DS3 AIS with no errors starting two M-frames after AIS activation and transmits normal traffic with no errors starting two M-frames after AIS deactivation.

Work Around:

None.

7. OUT-OF-SPEC LRCLK FREQUENCIES DURING DS3/E3 LOS, LOF, AIS, OR DS3 IDLE

Description:

When the DS3112 is configured for channelized operation (MC1:UNCHEN = 0), during DS3/E3 LOS, DS3/E3 LOF, DS3/E3 AIS, or DS3 idle, the DS3112 erroneously continues to examine the DS3/E3 and DS2/E2 C bits in the incoming data stream to determine the clock rates for the demultiplexed DS1/E1 tributaries. In these situations the C bits can have values that cause the frequencies of LRCLK1 through LRCLK28, LRCLKA, and LRCLKB to be well outside the 1.544MHz ±32ppm limits specified in ANSI T1.102 for DS1 and the 2.048MHz ±50ppm limits specified in ITU G.703 for E1.

Work Around:

In M13 mode, apply an accurate 1.544MHz clock to the LRCCLK pin. In E13 mode or G.747 mode, apply and accurate 2.048MHz clock to the LRCCLK pin. When LOS, LOF, AIS, or DS3 idle are detected (T3E3SR:LOS, T3E3SR:LOF, T3E3SR:AIS, T3E3SR:IDLE status bits), set the MC1:LRCCEN control bit high to switch the timing of the receive tributary ports to the LRCCLK pin. When these conditions have cleared, set the LRCCEN control bit low to switch back to standard timing.

8. OUT-OF-SPEC LRCLK FREQUENCIES DURING DS2/E2 LOF OR AIS

Description:

When the DS3112 is configured for channelized operation (MC1:UNCHEN = 0), if LOF or AIS occur on any DS2/E2, the DS3112 erroneously continues to examine the DS2/E2 C bits in the incoming data stream to determine the clock rates for the DS1/E1 tributaries demultiplexed from that DS2/E2. In these situations the C bits can have values that cause the LRCLK frequencies of the tributaries associated with the DS2/E2 to be well outside the 1.544MHz ±32ppm limits specified in ANSI T1.102 for DS1 and the 2.048MHz ±50ppm limits specified in ITU G.703 for E1.

Work Around:

When DS2/E2 LOF or AIS are detected (T2E2SR1:LOFn or T2E2SR1:AISn), externally switch the unaffected tributaries from the LRCLKn and LRDATn pins of the DS3112 to an external all-ones (AIS) generator clocked by an accurate DS1 or E1 clock.