



# DS3150

## 3.3V T3/E3/STS-1 Line Interface Unit

[www.maxim-ic.com](http://www.maxim-ic.com)

### REVISION B2 ERRATA

The errata listed below describe situations where DS3150 revision B2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to fix these errata in subsequent die revisions.

This errata sheet only applies to DS3150 revision B2 components. Revision B2 components are branded on the top side of the package with a six-digit code of the form yywwB2, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS3150 die revision, visit the website at [www.maxim-ic.com](http://www.maxim-ic.com).

#### 1. START-UP SEQUENCING PROBLEM IN THE TRANSMITTER

##### Description:

If a clock signal is applied to the transmitter during the first 10ms after power is applied, the transmitter will not work correctly.

##### Work Around:

Hold TCLK low or high for at least 10ms after power-up. If the signal applied to TCLK comes from a local oscillator, one easy way to keep TCLK from toggling during power-up is to connect a small CPU reset (such as Maxim's MAX6316L or MAX6801) to the enable input of the oscillator. During power-up, the CPU reset will disable the oscillator long enough to allow the DS3150B2 to power-up correctly.

In addition to the TCLK pin, there are two other possible clock sources for the transmitter that must be inhibited during power-up: the jitter attenuator (when enabled in the transmit path) and the receiver (when remote loopback is enabled). For proper transmitter operation, power-up the device with LBKS\* and TTS\* pulled to  $V_{DD}$  or  $V_{SS}$  (not left floating).