DALLAS ***MAXIM***

DS3150
3.3V T3/E3/STS-1 Line Interface Unit

www.maxim-ic.com

REVISION B4 ERRATA

The errata listed below describe situations where DS3150 revision B4 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3150 revision B4 components. Revision B4 components are branded on the topside of the package with a six-digit code in the form yyww B4, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS3150 die revision, visit our website at **www.maxim-ic.com/errata**.

1. POWER-ON RESET TIMING ISSUE

Description:

If V_{DD} is ramped too fast during power-up, an internal timing problem may cause some devices to remain stuck in reset. When a device is stuck in reset, the RCLK, RPOS/RNRZ, and RNEG/RLCV pins do not toggle, and the Tx+/Tx- pins either drive no signal or a low-amplitude signal (< 600mV). This condition persists until V_{DD} is ramped down and back up again.

Work Around:

This timing issue can be avoided if V_{DD} is ramped up with a slew rate of 40µs/V or slower.

REV: 012907