DS3181/DS3182/DS3183/DS3184 Single/Dual/Triple/Quad ATM/Packet PHYs with LIUs

REVISION A1 ERRATA

The errata listed below describe situations where DS3181/DS3182/DS3183/DS3184 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3181/DS3182/DS3183/DS3184 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS3181/DS3182/DS3183/DS3184 die revision, visit our website at www.maxim-ic.com/errata.

1. DEACTIVATION OF HIZ PIN ("1") TRI-STATING All LIU TXPn/TXNn OUTPUTS ("Z")

Description:
$\overline{\text{HIZ}}$ and $\overline{\text{JTRST}}$ pins are both active-low ("0") signals and are used to tri-state all digital output and bidirectional pins to high-impedance state ("Z") while maintaining all analog LIU output signals, TXPn and TXNn, in normal/on operational state. For normal operation, $\overline{\text{HIZ}}$ should be tied high ("1"). The expected behavior is listed in the table below:

$\overline{\text{HIZ}}$ (Active low)	$\overline{\text{JTRST}}$ (Active low)	All Digital Outputs	All Analog/LIU Outputs (TXPn/TXNn)
0	0	'Z'	Normal/On
0	1	JTAG/Normal	Normal/On
1	0	Normal	***Normal/On***
1	1	JTAG/Normal	***Normal/On***

In rows 3 and 4 (highlighted in ***bold italic*** fonts), all LIU outputs TXPn/TXNn are incorrectly tri-stated ("Z") when HIZ is inactive ("1").

Work Around:
Activate HIZ ("0") for normal operation. A combination event of activating and deactivating JTRST ("0' then "1") shall place the device into normal operation after completion of JTAG (row 2).

Permanent Fix:
HIZ input will be disconnected from LIU internally. This erratum is understood and will be corrected in revision A2.

2. HIGH TRANSMITTER CURRENT IN LIU(s) DESELECTED BY THE LM BITS IN THE ASSOCIATED PORT CONTROL REGISTER 2 (PORT.CR2)

Description:
When an active LIU is deselected via the Line Mode bits, LM[2:0], in the associated Port Control Register 2, PORT.CR2[10:8], the transmitter is left in its high-current state. If the LIU was in the process of transmitting a logic one ("1") when the clock is stopped, the transformer saturates and the transmitter consumes ~52mA (vs. ~38mA in normal operation).

The problem only occurs when deselecting an active LIU via the Line Mode bits. After power-up or hardware reset (RST="0"), the LIU is in a low-current state.

Work Around:
We recommend that to power down an active LIU, set the Transmit LIU Tri-State bit, TTS="1", the associated Port Control Register 2, PORT.CR2[14] and clear the Line Mode bits, LM[2:0]="000", in associated Port Control Register 2, PORT.CR2[10:8].

Permanent Fix:
Modifying the port to power-down the LIU when LM="000". This erratum is understood and will be corrected in revision A2.

3. SWITCHING BETWEEN SYSTEM LOOPBACK AND NORMAL OPERATION VIA IN THE ASSOCIATED PORT CONTROL REGISTER 4 (PORT.CR4) CAUSING ATM CELL CORRUPTION TOWARD SYSTEM INTERFACE (Rx DIRECTION)

Description:
System loopback mode is intended for off-line diagnostic testing. However, switching between system loopback and normal operation by setting/resetting the System Loopback bit, SLB, in the associated Port Control Register 4, PORT.CR4[11], the receive (Rx) FIFO data continues to be corrupted toward system interface until the Rx FIFO is reset. Traffic in the transmit direction away from system interface is not affected.

Work Around:
When switching between system loopback and normal operation or switching between system interface modes, the receive (Rx) FIFO should be reset as follows:

- Reset Rx FIFO (FF.RCR[0]="1")
- Activate or deactivate system loopback, SLB="1" (PORT.CR4[11])
- Clear Rx FIFO reset (FF.RCR[0]="0")

Permanent Fix:
More robust recovery mechanism will be implemented. This erratum is understood and will be corrected in revision A2.

4. DS3/E3 LOSS OF SIGNAL (LOS) STATUS IS NOT CLEARED WHEN THE ASSOCIATED PORT IS OPERATING IN THE DS3/E3 AMI MODE

Description:
AMI mode is defined as when B3ZS/HDB3 zero suppression mode is disabled in the line encoder/decoder. AMI is not a standard encoded signal and is only used for diagnostics and performance testing.

LOS is set when there are no pulses on RXPn/RXNn (RPOSn/RNEGn when LIU is disabled) for 192 consecutive clocks and is clear when there are no EXZ events on RXPn/RXNn (RPOSn/RNEGn when LIU is disabled) for 192 consecutive clocks (1/3 pulse density in B3ZS and 1/4 pulse density in HDB3 estimation).

The expected behavior for all modes, i.e., B3ZS/HDB3/AMI, when the receive coax cable is disconnected, the LOS status should be set and when the cable is reconnected, the LOS status should clear. However, when receiving an AMI encoded signal, the LOS might never clear, unless it is a simple repeating pattern with less than three B3ZS or four HDB3 zeros in the pattern. When the decoder is programmed not to expect zero code suppression, EXZ is not defined. When LOS is detected, a down stream AIS is generated by default toward system interface.

Work Around:
When an AMI encoded signal is applied to receive signal(s):

- Disable automatic downstream AIS generation, PAIS[2:0], in the associated Port Control Register 1, PORT.CR1[14:12].
- When operating in T3 mode, set the Automatic downstream AIS generation Disable, AAISD, in the associated T3 Port Control Register, T3.RCR[11].
- When operating in E3 G.751 mode, set the Automatic downstream AIS generation Disable, AAISD, in the associated E3 G.751 Port Control Register, E3G751.RCR[11].

- When operating in E3 G.832 mode, set the Automatic downstream AIS generation Disable, AAISD, in the associated E3 G.832 Port Control Register, E3G832.RCR[11].
- Ignore the associated port's LOSL latched status, LINE.RSRL[0]
- Use RLOL latched status, PORT.SRL[1], to determine the status of the receive signal.

Permanent Fix:
LOS detection will be blocked in AMI mode. Receive Loss Of Lock (RLOL) latched status from the LIU(s) is sufficient to determine the present condition status of the receive signal. This erratum is understood and will be corrected in revision A2.

5. UNFRAMED-ALL-ONE STATUS IS NOT CLEARED UNTIL FRAMED SIGNAL IS RECEIVED

Description:
The Unframed-All-One status RUA1, T3/E3.RSR1[8], is set when less than 4 zeroes pattern is applied at receive T3/E3 signal:

- In framed modes, RUA1 should be clear when more than 4 zeroes pattern occurs or OOF is not detected in the receive T3/E3 signal.
- In unframed modes, RUA1 should be clear when more than 4 zeroes pattern occurs in the receive T3/E3 signal.

There is no problem in unframed modes. In framed modes, DS3 and E3, the RUA1 status is set when an unframed all ones signal is applied, but when the cable is pulled the RUAl status remains set. The RUA1 status can only be cleared when a framed signal is applied.

Note: An E3 AIS signal is essentially an unframed all ones signal and it clears when the cable is pulled, but the RUA1 signal in E3 can not cleared until a framed E3 signal is applied.

Work Around:
Ignore RUA1 status in framed modes.

Permanent Fix:
Fix RUA1 implementation in framed mode, per above definition: RUA1 should be clear when more than 4 zeroes pattern occurs or OOF is not detected in the receive T3/E3 signal. This erratum is understood and will be corrected in revision A2.

6. ATM CELL HEC (HEADER ERROR CODE) CORRUPTION IN DSS (DISTRIBUTED SAMPLE SCRAMBLER) MODE

Description:
When DSS mode is enabled, ATM cells being forwarded toward the UTOPIA/POS-PHY 2/3 system interface contain corrupted HEC (Header Error Code) field. Cell header and payload bytes are uncorrupted. The DSS receiver synchronizes properly, but when the data is forwarded in the mode, the HEC is corrupted due to improper data flow through the pipeline registers.

Work Around:
Disable forwarding of HEC field toward system interface in the receiving direction by clear the Receive System HEC Transfer Enable, RHECT='0' (default), of the System Interface Receive Control Register 1, SI.RCR1[0].

Note: HEC transfer would need to be disabled as well in the transmit direction by clear the Transmit System HEC Transfer Enable, THECT='0' (default), of the System Interface Transmit Control Register, SI.TCR[0].

Ignore HEC field being passed through UTOPIA/POS-PHY 2/3 system interface at the Master PHY.

Permanent Fix:
Fix to forward correct HEC field in ATM cells being forwarded toward UTOPIA/POS-PHY 2/3 system interface in DSS mode. This erratum is understood and will be corrected in revision A2.

7. RCLKOn JITTER

Description:
RCLKOn pins have an excessive jitter of ±3ns due to internal cross talk caused by top/chip level routing. Therefore, in subrate or fractional DS3/E3 mode, DS3184 A1 implementation requires the external circuitry, e.g., FPGA/CPLD, must be capable of operating at frequency of at least 62/52/40MHz instead of normal operating line frequency of 51.84/44.736/34.368MHz for Clear-Channel-52Mbps/DS3/E3, respectively.

Work Around:
For subrate or fractional mode, especially Flexible Fractional mode, we recommend using an external FPGA/CPLD that is capable of operating at a minimum frequency of 62/52/40MHz.

Permanent Fix:
Top/chip level routing and shielding of RCLKOn signals by a metal layer change. This erratum is understood and will be correction in revision A2.