ERRATA SHEET
DS34T101/DS34T102/DS34T104/DS34T108

Revision A1 Errata

The errata listed below describe situations where DS34T101/DS34T102/DS34T104/DS34T108 revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata in subsequent die revisions.

*This errata sheet only applies to DS34T101/DS34T102/DS34T104/DS34T108 revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another DS34T101/DS34T102/DS34T104/DS34T108 die revision, visit our website at **www.maxim-ic.com/errata**.*

SECTION 1: CIRCUIT EMULATION ENGINE

1) IPv6 IS NOT SUPPORTED

Description:
The packet classifier on DS34T10x rev A1 devices discards received packets with Ethertype 86DD, the Ethertype for IPv6.

Workaround:
None.

2) UDP CHECKSUM IS NOT SUPPORTED

Description:
DS34T10x rev A1 devices do not calculate the checksum of data when preparing UDP packets for transmission or when receiving UDP packets. RFC-791 makes the UDP checksum optional for IPv4 nodes, but RFC-2460 requires the checksum when UDP packets are originated or received by an IPv6 node.

Workaround:
Use off-chip resources to calculate UDP checksums and provide them to the DS34T10x device for inclusion in the UDP headers of transmitted packets and for comparison with the checksums in the UDP headers of received packets.

OR

Include a fixed, nonzero checksum in the UDP headers of transmitted packets. If intermediate IPv6 nodes are only discarding packets with zero checksums in the UDP headers, this workaround will allow two DS34T10x devices to exchange UDP packets through an IPv6 network.

SECTION 2: T1/E1/J1 FRAMER

1) RECEIVE LOOP CODES STATUS BITS

Description:
Receive loop code status bits do not work in DS34T10x rev A1. The following are the incorrect bits:

BIT	LOCATION BIT NAME	BIT DESCRIPTION
RRTS3.0	LUP	Loop-Up Code Detected Condition
RRTS3.1	LDN	Loop-Down Code Detected Condition
RRTS3.2	LSP	Spare Code Detected Condition
RLS3.0	LUPD	Loop-Up Code Detected Condition Detect
RLS3.1	LDND	Loop-Down Code Detected Condition Detect
RLS3.2	LSPD	Spare Code Detected Condition Detect
RLS3.4	LUPC	Loop-Up Code Detected Condition Clear
RLS3.5	LDNC	Loop-Down Code Detected Condition Clear
RLS3.6	LSPC	Spare Code Detected Condition Clear

Workaround:
Use the internal BERT to detect loop codes. Configure the internal BERT to detect a repetitive pattern for the loop code. Map all the receive data bits to the internal BERT (unframed mode). Loop code is detected when the BERT pattern matches and the BERT bit error rate is less than 10%.

Transmit loop codes work correctly.

2) AUTOMATIC RAI INSERTION

Description:
When automatic RAI insertion is enabled the RAI is not automatically inserted if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled).

Workaround:
Monitor the CRC4 Sync Counter bits (RRTS7[7:3]) in register E1RRTS7 (Receive Real-Time Status Register 7–E1 Mode). If CSC count value exceeds 16, manually transmit RAI alarm via the alarm bit (E1TNAF.5) in the Transmit Non-Align Frame register (E1TNAF). If the CRC4 sync is found, stop the alarm via the E1TNAF alarm bit.

3) RECEIVE FRAMER SOFT RESET

Description:
Receive Framer Soft Reset Bit (SFTRST bit 1 in RMMR register) does not work.

Workaround:
Manually reset the receive framer. Disable port using the Frame Enable bit (FRM_EN bit 7 in RMMR register). Write 00 to all addresses in the framer span. Then write FF to latched status addresses in framer span.

4) TRANSMIT FRAMER SOFT RESET

Description:
Transmit Framer Soft Reset Bit (SFTRST bit 1 in TMMR register) does not work.

Workaround:
Manually reset the transmit framer. Disable port using the Frame Enable bit (FRM_EN bit 7 in TMMR register). Write 00 to all addresses in the framer span. Then write FF to latched status addresses in framer span.

5) T1 RECEIVE SYNC

Description:
T1 receive sync may get into a state where it cycles in and out of sync. This occurs when the T1 receive sync cannot align to a new frame alignment that is 2 bits before the current frame alignment.

Work Around:
When the user receives a loss of frame condition (RLS1.RLOFD) that repeatedly clears and sets, he/she should check to see if the Change of Frame Alignment latched status bit (COFA Bit 5 in register RLS2) is set at least once per 20ms over a period of 200ms. If COFA is being set at that rate, the user should implement the following:

Disable the receive data path via the Receive port Frame Enable config bit (FRM_EN Bit 7 in register RMMR) for 5µs. This will separate the old sync and the new sync by more than 2 bits. This will allow the new sync to be detected properly.

6) TRANSMIT SYNC INITIALIZATION

Description:
When using a transmit sync source other than the internal sync (e.g., TSYNC as an input), the transmit data path cannot update the alignment to sync input boundary if the new alignment is 1 bit before the current frame alignment.

Workaround:
When minimum delay mode is enabled and when sync source such as PLB, TSYNC configured as input, transmit synchronizer or transmit estore is used, the following routine can be used to ensure the sync is updated properly:

Wait for new sync source to be applied and stable. Disable the transmit data path via the transmit port Frame Enable config bit (FRM_EN Bit 7 in register TMMR) for 5µs. This will separate the old sync and the new sync by more than 2 bits and the new sync should now be detected properly.

7) RECEIVE ESTORE SLIP LATCHED STATUS BIT RSLIP

Description:
Receive Estore Slip Latched status bit RSLIP (located in Bit 5 in register RLS4) is not latched.

Workaround:
RSLIP bit is an 'OR' of RESEM (RLS4.6) and RESF (RLS4.7) bits, which are latched status bits. Clear RESEM and RESF to clear RSLIP.

8) TRANSMIT ESTORE SLIP LATCHED STATUS BIT TSLIP

Description:
Transmit Estore Slip Latched status bit TSLIP (located in bit 5 in register TLS1) is not latched.

Workaround:
TSLIP bit is an 'OR' of TESEM (TLS1.6) and TESF (TLS1.7) bits, which are latched status bits. Clear TESEM and TESF to clear TSLIP.

9) RRTS7 READ ISSUE

Description:
When switched from T1 to E1 without using hardware reset, RRTS7 reads an ‘OR’ed output of E1 RRTS7, T1 RFDL.

Work Around:
Use global soft reset when switching from T1 to E1.

10) E1 RECEIVE MULTIFRAME LATCHED STATUS CAS MODE

Description:
E1 Receive signaling registers (RS1–RS16) are updated 10µs after the RMF bit is set.

Work Around:
Wait at least 10µs after RMF bit detect before reading the RS1–RS16 registers.

11) E1 RECEIVE MULTIFRAME LATCHED STATUS CSS MODE

Description:
E1 RMF (RLS4.0) latched status bit in CCS mode is sometimes set on the multiframe boundary, and again one frame after the multiframe boundary. The RS1–RS16 registers in CCS mode are updated one frame after the multiframe boundary.

Work Around:
Wait at least 250µs after detecting RMF before clearing the latched status bit and reading RS1–RS16 registers.

12) RECEIVE DATA PATH INSERTION FUNCTIONS

Description:
Receive data path insertion functions (Idle code, Digital Milliwatt, Bit Inversion, Internal BERT direction reversed, Force Signaling all Ones) do not pass through RSER when Estore or IBO mode is enabled. Receive data path insertion functions do pass through RSER when Estore is disabled, and always pass through internal loopbacks (per-channel loopback, payload loopback).

Work Around:
None.

13) RECEIVE T1 COFA STATUS BIT

Description:
Receive T1 COFA status bit does not report multiframe change of frame alignment.

Work Around:
None.