

Revision B5 may be identified by the date/revision brand yywwB5, where yy and ww are the year and work-week of manufacture, respectively. This errata sheet is valid only when used in conjunction with the most current version of the data sheet available from Dallas Semiconductor on our website at www.maxim-ic.com.

ERRATA

1. Timer 0 will only clock at the divide-by-4 rate if it is being used in mode 3 with the TMOD.2 bit set. Timer 0 can be configured correctly in both the divide by four and divide-by-12 modes if the TMOD.2 bit is cleared.

Work Around: None. This erratum will be corrected in a future revision of the device.

2. Stop mode current, with the bandgap reference disabled, may be as high as 5 μ A on certain lots of the DS80C320. This erratum applies only to commercial temperature grade material with date codes between 9743B5 and 9802B5.

Work Around: None. This erratum applies only to the material listed above.

3. When a short reset stimulus occurs during the execution of an extended MOVX data memory access, the ALE signal may not be driven with the strong transition drivers (V_{OH2} test levels) on the first instruction fetch following reset. This reduced drive current may not allow the ALE signal to rise to a logic high level before the first instruction fetch at location 0000h, possibly latching an incorrect address. This situation will only occur during a watchdog timer reset (the timer generates a momentary pulse to the internal reset circuitry) or when an external reset pulse of less than 2 μ s is asserted. This errata does not affect a power-on reset as the internal crystal warmup period counter provides a reset pulse of greater than 2 μ s.

Work Around: If the watchdog timer reset function is employed, use the watchdog timer interrupt to ensure that the device will not be executing MOVX instructions when the watchdog timer reset occurs. If an external reset stimulus is used, be sure that it is at least 2 μ s in duration.