Revision A1 may be identified by the date/revision brand yywwA1, where yy and ww are the year and workweek of manufacture, respectively. This errata sheet is valid only when used in conjunction with the most current version of the data sheet available from Dallas Semiconductor via the Internet.

This document contains the following types of information:

Errata: These are design errors which deviate from published specifications. Errata are intended to be fixed in subsequent revisions of the device.

Specification Modifications: These are changes to the published specifications and will be reflected in the next update of the documentation and apply to all subsequent revisions of the device.

Documentation Changes: This information includes typographical mistakes, errors, omissions or clarifications of device operation. Items listed in this section will be reflected in the next update of the documentation.

ERRATA

1.   The broadcast address portion of the serial port's address recognition mode does not function. All other aspects of this mode work properly.

   Work Around: Use the "Given Address" (SADDR masked by SADEN) to create a group that may be addressed separately or as a unit.

2.   The SPTA0 and SPTA1 flags will not reflect the activity of the serial port if the corresponding TI bit is at a logic one prior to loading the corresponding SBUF register. In a traditional 8051 polling scheme, the SBUF is loaded with a character, and software loops until the TI bit is set. A similar scheme can be used with SPTA0 and SPTA1 bits, which will transition from 1 to 0 to indicate completion of the serial port transmission. Such a scheme usually ignores the TI bits, allowing them to remain set after the first transmission. This erratum means that for such a polling scheme to work with the SPTA0 and SPTA1 bits, software must clear the TI flag if set by a previous serial port transmission before loading SBUF.

   Work Around: Clear the corresponding TI bit before loading SBUF if a transmit bit polling scheme is used to sequence serial port transmission. It may be more convenient in software to clear the TI bit after the transmission has completed, rather than before. This will work also, as long as the TI bit is cleared before the next load of SBUF.

3.   Timer 0 will only clock at the divide by four rates if it is being used in mode 3 with the TMOD.2 bit set. Timer 0 can be configured correctly in both the divide by four and divide by 12 modes if the TMOD is cleared.

   Work Around: This errata will be corrected in a future revision of the device.

4.　　When a short reset stimulus occurs during the execution of an extended MOVX data memory access, the ALE signal may not be driven with the strong transition drivers (V_{OH2} test levels) on the first instruction fetch following reset. This reduced drive current may not allow the ALE signal to rise to a logic high level before the first instruction fetch at location 0000h, possibly latching an incorrect address. This situation will only occur during a watchdog timer reset (the timer generates a momentary pulse to the internal reset circuitry) or when an external reset pulse of less than 2 µs is asserted. This errata does not affect a power-on reset as the internal crystal warm-up period counter provides a reset pulse of greater than 2 µs.

Work Around: If the watchdog timer reset function is employed, use the watchdog timer interrupt to ensure that the device will not be executing MOVX instructions when the watchdog timer reset occurs. If an external reset stimulus is used, be sure that it is at least 2 µs in duration.

SPECIFICATION MODIFICATIONS

1. NONE

DOCUMENTATION CHANGES

1. NONE